THE REMOTE MEASUREMENT OF PHASE ANGLE

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DOCTOR OF PHILOSOPHY

by

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SUMMARY

In the distribution of electricity, it is necessary to link the outputs of substations, which may be many miles apart. In order to prevent an excessive surge of current in the connecting link, the connection between a pair of substations should not be made until the phase angle between their voltages is small. There has been, for many years, a need for the measurement of this phase angle, with the results displayed in the distribution Control Room. A direct measurement may be significantly in error, due to the time delay in transmission of the measurement signals from substation to Control Room. This error is avoided in the measurement system described. A test signal, superimposed on the phase measurement signal, repetitively measures the transmission path delay, and applies a suitable correction to the phase angle indication. The system may be used either with pilot lines or a radio link between substations and Control Room. An advantage is that the route of a pilot line may be changed without affecting the accuracy, thus allowing the use of public telephone lines, if necessary.

A pilot line system has been installed in the Birmingham Area of the Midlands Electricity Board: the maximum length of pilot line used is 12 miles, and the measurement error does not exceed a small fraction of one degree. The equipment has been designed to possess a high degree of reliability.

Although primarily designed for operation at 50 Hz, the system could readily be adapted for use at higher frequencies.

CONTENTS

1.1 INTRODUCTION

In the generation and distribution of electricity, the output of electrical energy from the generating stations is fed to a network of transmission lines which convey the power to the main areas of load. To achieve a high efficiency of transmission, these lines are operated at a potential of some hundreds of kilovolts, and this voltage is reduced, by successive stages of transformation, before being supplied to the consumer. The early stages of voltage transformation are carried out in substations : typically, in a primary substation the voltage may be reduced to 33kV, and this is supplied to several smaller substations giving a further reduction to 11kV. Each of these latter will feed a number of transformers, having the output voltage required by the consumer.

The substations are designed with a capacity sufficient to supply the load normally expected in the area they serve. There may be occasions, however, when an unusually heavy load falls on a particular substation : provision is made, therefore, to link the outputs of the substations at the 33kV or 11kV level, enabling the load to be redistributed between them. It may also be advantageous to link points at a lower voltage level in the distribution system. Before the link connection can safely be made, the phase relation between the voltages must be known : if the voltages differ in phase by too great an angle, an excessive transient current will flow when the link circuit breaker is closed. Ideally, the phase angle between every pair of circuits to be connected would be measured : this is not practicable, however, as there are a large number of points between which a link can be made, and a separate communication circuit would be required for each point. It is considered sufficient, therefore, to measure the relative phase between feeder points at the 33kV or 11kV level only. The current surge resulting from the connection of the link between two points in the distribution system will depend upon the impedance of the circuits

and the nature of the loads connected, as well as the phase angle between the points. Interpretation of the phase measurement in terms of surge current in a particular link will therefore depend upon accumulated experience of the distribution system.

The decision to make the link connection is made in the Area Control Centre, which may be many miles distant from either of the substations. This situation thus creates the need for a method of measuring the phase angle between two 50 Hz voltages, at two widely separated locations, with the results of the measurement displayed at a point distant from either of the voltages to be measured. The object of this research project has been to devise a system enabling the measurement to be made.

It is possible to imagine many systems for the solution of this measurement problem, and they may be divided into two groups. The first group contains those systems where the phase angle measurement is made within the substations: the line voltage of a substation is compared in phase with a reference voltage received by radio or pilot line, and the results telemetered to the Control Centre.[1] The reference voltage may be generated in the Control Centre or in another substation, or may be derived from a radio signal available to all substations, such as the long-wave transmissions used for broadcasting or for navigational aids. The phase difference between voltages at two substations is then obtained by subtracting, in the Control Centre, the results of the two separate measurements. The systems in this group have the advantage that transmission time delay in the telemetry channel between substations and Control Centre is unimportant, and the type of telemetry signal transmitted may be chosen to be best resistant to degradation by electrical noise induced in the circuits. However, they have the disadvantage of requiring accurate phase-measuring equipment in each substation: the equipment would probably be complex and expensive, and difficult to design to the standard of reliability required. It is likely that difficulties would also be encountered in deriving the reference voltage in

each substation. As far as the author is aware, no system in this group has so far been developed.

In the second group of systems, a voltage derived from the line voltage of each substation is transmitted to the Control Centre by pilot lines or radio, and the phase comparison is made in the Control Centre; thus, only one set of phase measuring equipment is required. The disadvantage of these systems lies in the transmission path delay : the finite velocity of propagation of the signal from the substation causes the voltage received at the Control Centre to be delayed with respect to the substation voltage. The phase angle measured in the Control Centre is thus in error by an amount proportional to the difference in the transmission delays from the two substations : the error may be several degrees at 50 Hz, with the substation distances at present in use by the Midlands Electricity Board.

This disadvantage of systems in the second group may be overcome if the transmission path delay from each substation to the Control Centre is known. Means can then be provided to compensate for the difference in delay. One method is to use, at the Control Centre, additional delay in series with the input from each substation, bringing the total delay to a standard value. Another method is to generate a signal proportional to the difference in delay from the two substations, and to use this signal to correct the phase indication. In the case where transmission is by radio, a knowledge of the geographical position of the substations is sufficient to enable the delay to be calculated.[2] Where pilot lines are used then, if the length and electrical characteristics of the line are known, the calculation of the delay is equally simple.[3] However, for some of the lines in use no specification exists, and transmission from substation to Control Centre may utilise several lengths of lines of differing characteristics connected end to end. Also, it may be necessary to re-route a pilot line, at short notice, as operational requirements demand. Under these conditions some method of measurement of transmission path delay is essential. In one system

considered, the delay would be measured, using appropriate test gear, when the equipment is installed, and the delay compensation circuits in the Control Centre set. The delays would then be periodically checked at times when the lines were not otherwise in use: this would be inconvenient and would give no protection against changes in line characteristics[9] that might have occurred since the previous check. In another system considered, the test gear would be permanently built in to the Control Centre equipment: by the operation of a switch, the line delay could be checked immediately before a phase measurement,[4, 5] and a warning indication given if there had been a change in the line delay from its original value. The disadvantage of this system is the need to rely on the operator to check the delays. In times of emergency, when the phase-measuring equipment is likely to be most useful, it is probable that the operator would be too busy with his other duties to carry out the checking procedure, simple though it may be.

The system finally developed for this project falls into the second group. The transmission path delay is measured repetitively, at intervals corresponding to two periods of the a.c. supply. The results of the measurements are used to correct the phase-angle indication. The operation is automatic, no preliminary setting-up being required. Should the delay alter, due, for example, to the re-routeing of a pilot line, then the new value of correction signal will be established within a time of approximately one second. The system has the advantage that public telephone lines may be used, without restrictions on the route the telephone operator may choose to select. The system is the subject of British Patent Application Nos. 30487/68 and 36604/68.

Although the research to be described was directed primarily toward the measurement of phase angle between 50 Hz voltages, as required by the sponsors of the project, it is clear

that the underlying principles have a much wider application. The measurement method developed can be used to determine the relative timing of any number of single or repetitive events occurring at points remote from the measurement location, and where the transmission delay times of the measurement signals are unknown, and perhaps varying.

The same principles can also be used to control the relative times of transmission of signals from a given location, so that they will be received at arbitrarily remote points with any temporal relation.

2.1 HISTORY AND ORGANISATION OF THE PROJECT

The project was initiated by the Midlands Electricity Board,[6] who have cooperated closely with the University throughout the work. Much of the construction and testing of the apparatus has been carried out by M. E. B. technicians working in the University laboratories, the number of technicians so employed varying between one and four. The M. E. B. have also made available a number of typical pilot lines with connections to the University laboratory : this has enabled long-term measurements to be made under conditions similar to those which will exist when the equipment is in service.

The total cost of the project exceeds £30, 000, which has been borne largely by the Electricity Council, through the Electricity Council Research Centre. This cost has included the development of the system of remote phase-angle measurement using pilot lines, and an alternative system using a U. H. F. radio link. There has simultaneously been developed a method of measurement of power system frequencies. Only the first two of these are hereinafter described; the third forms the subject of a separate report.[7]

The project has been carried out in four stages. In the first stage, the principles underlying the system of remote phase measurement were evolved : this led to the construction of a Feasibility Model (F. M.) to test these principles. This apparatus, although hastily constructed, gave results sufficiently conclusive to justify the continuation of work on the system.[8]

The second stage of the project was the construction of an improved version of the F. M. , using pilot lines, for temporary installation in the Birmingham Area. This was called the Field Trials Model (F. T. M.), and was in service for approximately six months. It was arranged to measure the phase difference between two test points located within the same substation. Using a series

of pilot lines, of various lengths, to transmit the signals to the Control Centre, the phase angle indicated in the Control Centre was compared with that measured by a conventional phase meter located in the substation. This check of the accuracy of the remote phase measurement was carried out over a extended period, and confirmed the results obtained in the laboratory. Much useful operational experience was gained from the F. T. M., which was invaluable in the design of the later equipment.

The third stage of the project was the design of a fully-engineered version of the pilot line equipment, suitable for quantity production, and arranged to permit measurement of the phase difference between voltages in any pair of a number of substations. This is called the Multi - Station Engineered Version (M. S. E. V.) of the equipment : one Control Centre and twelve substation units have so far been manufactured, and installed in the Birmingham Area.

The fourth stage of the project, which ran concurrently with stage three, was the development of a version of the equipment using signals transmitted over a radio link rather than by pilot line. This was feasibility study only : both radio link and pilot line equipment were installed in two substations, to measure the phase angle between common test points; the results of the separate measurements were then compared.

Most of this report is concerned with the design of the pilot line equipment, as it was found that this could be used, with little modification, for the radio link system.

Throughout the project, the resources of the University laboratories and workshops have been used. It has been necessary to design and construct certain items of test equipment which were not commercially available. In particular, an instrument for the generation of two voltages having an accurately - known phase difference has been developed : this must be regarded as a necessary piece of test gear for the maintenance of the remote phase angle equipment after installation.

3.1 SPECIFICATION OF PERFORMANCE

The performance required by the remote phase measurement system is given below. Most of this was specified by the M. E. B. at the start of the project; the remainder has been arrived at subsequently, when certain possibilities emerged as the system was developed.

Permissible error of measurement : not exceeding 1^{o}.

Accuracy to be unaffected by supply frequency over the range 46-51 Hz.

Range of measurement : $\pm 25^{o}$. It is expected that phase angles in the range -10^{o} to $+10^{o}$ will be of most importance.

Provision for continuous recording of phase angle to be made.

Number of substations : up to 25.

If phase angle measurement between two points within the same substation is required, two pilot lines to the Control Centre will be provided.

Maximum length of pilot line from substation to Control Centre : 12 miles.

Accuracy to be not significantly affected by type of pilot line, or by use of several lengths of pilot line of differing characteristics.

Voltage isolating transformers to be used at the Control Centre and at each substation, to give insulation of the pilot line up to 2kV r. m. s.

Performance of the system to be resistant to degradation by electrical noise induced in the pilot lines, or faults in the pilot lines such as low insulation resistance to earth or between lines.

A clear warning to be given, should the polarity of a pilot line be inadvertently reversed.

Measurement of phase angle between two voltages by measurement of the relative times when the voltages pass through zero value, is acceptable.

The measurement is not to depend on synchronization between 50 Hz voltages at Control Centre and substations.

Provision to be made for checking the electrical length of the pilot lines immediately prior to a measurement.

The Control Centre equipment to operate over an ambient temperature range of $10^{\circ}C$ to $40^{\circ}C$, from a supply voltage of 240V, +10%, - 15%, 46-51 Hz.

The substation equipments to operate over a range of ambient temperature of $0^{\circ}C$ to $50^{\circ}C$, with a supply voltage of 110V, +10%, -15%, 46-51 Hz.

The power consumption of the substation equipments, and the harmonic content of their supply current, to be sufficiently low to allow the equipments to be powered from the same source as the voltage whose phase angle is to be measured.

A high standard of reliability to be provided. In particular, the equipment should not give an erroneous indication; it should "fail safe".

The amount of routine maintenance required should be kept to a minimum.

In the interests of cost, reliability and maintenance, a preferred system would have most of the necessary complexity in the Control Centre equipment, the substation equipments being relatively simple.

The M. S. E. V. equipment satisfies all of these requirements : the accuracy achieved is higher than given in the specification above, and satisfactory operation has been obtained using pilot lines several miles longer than the maximum specified.

4.1 MEASUREMENT AND DISPLAY OF PHASE ANGLE

The design of the equipment is dominated by the choice of method for measurement and display of the phase angle. The system for the correction of transmission path delay will therefore be discussed in the next Section; here it will be assumed that there are available two trains of pulses at supply frequency f : the pulses in one train leading those in the other by a time t_ϕ, corresponding to the phase angle ϕ. The process of phase angle measurement is then one of measuring t_ϕ, and dividing this time by the supply period $\frac{1}{f}$. The minimum duration of a measurement is thus equal to one period of the supply, and successive measurements may be made at a frequency f. This rate of measurement information is far higher than is required, or can be interpreted, by the Control Engineer; he is unlikely to need phase angle readings updated as frequently as once per second. The large ratio of capability to requirement may be usefully employed to discriminate against random errors, such as might be caused by electrical noise induced in the system, or the error of $\pm$ 1 count which is an inevitable feature of many digital systems.

4.2 Display Methods

The choice of method of phase angle measurement is greatly influenced by the manner in which the results are to be displayed. In a Control Room, there are two suitable types of display: "digital", in which the readings are shown on numerical indicators, or "analogue", in which a meter is used. An advantage of the digital type of display is its great potential accuracy, since any number of numerical indicators can be used : another advantage is the brilliance and clarity of the display, enabling it to be understood from a distance.[10] The analogue display has an advantage that the meter, due to its inertia, has a built-in averaging action which smooths out fluctuations caused by noise. Perhaps a greater advantage is the ability to show trends in the phase indication; an operator already skilled in interpretation of meter readings should have little

difficulty in appreciating the significance of the meter needle variations, whereas the presentation of a succession of numerical indications is usually much less informative.

In view of the above considerations, and the fact that "lag" or "lead" indications can readily be given by the use of a centre-zero meter, the analogue type of display was chosen. This was a fortunate choice, as it led to the development of a simple method of line delay correction, as described in Sec. 6.3.

4.3 Measurement Methods

The methods of phase angle measurement also may be divided into "digital" or "analogue" types. In the digital type of measurement,[11] the duration of t_ϕ and $\frac{1}{f}$ are measured by counting the number of pulses from a constant-frequency oscillator which occur in the time being measured. The division of t_ϕ by $\frac{1}{f}$ is then performed digitally. The advantages of a long-duration measurement may be obtained by summing the pulse counts for t_ϕ and $\frac{1}{f}$ over many cycles of the supply. This system has a potentially high accuracy; it has the disadvantage of complexity, however, and if it is to be used with a meter display a digital-to-analogue converter is required.

In the analogue type of phase angle measurement,[12-19] a current of constant and accurately-known amplitude I is made to flow in the meter circuit for the time t_ϕ in each period of the supply: the average meter current is thus

$$I_{av} = fIt_\phi = \frac{I\phi}{360}, \qquad \text{------} \qquad (4.3.1)$$

where ϕ is the phase angle in degrees. It has been found possible to generate the current I with a long-term error not exceeding a small fraction of one per cent;[7] the accuracy of measurement using this system is thus limited mainly by errors in the meter. As a meter display had already been decided upon, a method of phase angle measurement of the analogue type was chosen.

In both the digital and the analogue systems described above a difficulty arises when it is required, as for this project, to provide a continuous display of phase angle from negative, through zero, to positive values.[20] For the analogue system, a method of overcoming the difficulty is to delay one of the input signals by a constant time T_Z, corresponding to the maximum phase angle to be measured. A side zero meter is used, but with a scale calibrated to have 0^o in the centre. The average meter current is thus

$$I_{av} = fI(t_\phi + T_Z) = \frac{I\phi}{360} + fIT_Z. \quad \text{----} \quad (4.3.2)$$

The arrangement thus has the disadvantage of being frequency sensitive, a change in frequency giving a constant error for all values of ϕ : another disadvantage is that the indications are critically dependent on the amplitude of the current I, and the time T_Z. This method was therefore rejected, as an inaccuracy in any of these quantities would cause an unnoticed error in the phase angle indications in a region, namely 0^o, where the accuracy is most important.

The problem was solved in the manner shown in Fig. 1;[21] Figs. 2 and 3 give the sequence of operation. Consider the case when the voltage at the input X leads that of the input Y, as shown in Fig. 2. The monostable element M is triggered from X before the bistable element B is triggered from Y. The gate G_p, which is connected to sense the condition $(M + \overline{B})$, opens, causing a defined current I_p to flow from the positive-current generator PCG into the meter : this continues until B is triggered from Y. The period T_M of M must be greater than the time corresponding to the maximum phase angle to be measured, but no great accuracy of T_M is otherwise required. At the end of this period B is then reset by M, and no further meter current flows. When Y leads X (Fig. 3), B is triggered before M, and the gate G_n, connected to sense the condition

($\bar{M}$ + B), opens, causing a defined current I_n to flow from the negative current generator NCG into the meter : this continues until M is triggered. Again, at the end of the period T_M, B is reset by M and no further meter current flows. By making $I_p = I_n = I$, the average meter current is then

$$I_{av} = fIt_{\phi} = \frac{I\phi}{360} \qquad \text{------} \qquad (4.3.3)$$

in magnitude, with a direction determined by the relative time sequence of the inputs X and Y. The meter indication of phase angle is thus independent of frequency. Vibration of the meter needle is avoided by the inertia of the movement, and by the use of a capacitative filter F to smooth out the pulses of current from PCG and NCG.

The accuracy of measurement of phase angle using the system of Fig. 1 is limited by time delay in the logic elements, inaccuracy of the current generators and errors in the meter. The logic elements were designed to have a delay of less than 10^{-7} second; this corresponds to an error of 0.0018 degree at 50 Hz, and is independent of the value of ϕ. The current generators were designed to maintain the current I within $\pm 1\%$ of nominal; this corresponds to an error of 0.25° at full-scale deflection of the meter, and proportionately less for smaller deflections. By a more elaborate design of current generator,[7] this error could be reduced to 0.1° at full scale. However, the extra complication was not thought justified, as the overall accuracy is limited by errors in the meter, which are of the same order as those of the current generators. The overall error will therefore not exceed 0.5° at full-scale deflection corresponding to $\pm 25^{\circ}$, and in the range $\pm 10^{\circ}$, which is of greatest interest, the errors will be less than 0.2°.

With this system, there is the possibility, should one or both of the input voltages fail, that current pulses of excessive duration will be generated, causing the meter to be overloaded. The current generators have therefore been designed with inherent overload protection, and damage to the meter is not possible under any normal conditions of use.

5.1 COMPENSATION FOR TRANSMISSION DELAY

The methods of measurement of phase angle described in the previous section assumed that the time difference between corresponding pulses in the two pulse trains was t_ϕ, i.e. equal to the time difference between the 50 Hz substation voltages. However, as discussed in section 1.1, the pulses received at the Control Centre will be delayed by transmission along the pilot lines, and the apparent phase angle between these pulses needs correcting by an amount equal to the difference between the transmission delay times.

There are two methods of making this correction. The first method is to add extra delay to each pilot line entering the Control Centre, to bring the total transmission delay in each line to a standard value[5] this requires a means of comparing the total delay of each line with the standard. One way in which this comparison could be accomplished would be to link a pair of substations at a time of light load, when the current in the interconnection was small : the substation voltages would then be assumed to be in phase. The delay elements would be adjusted to give synchronous pulse trains at the Control Centre : this procedure would be repeated with various pairs of substations, until the transmission delay of all pilot lines were equal. Another way of equalizing the transmission delays would be to measure the delay of each line separately, using a transponder system. A pulse generated at the Control Centre is received at a substation, and retransmitted back to the Control Centre : if the delay in both directions can be assumed equal, the time between transmission and reception of pulses at the Control Centre is then a direct measure of twice the transmission delay. Both of these ways of transmission delay measurement could be used to adjust the added delay to give equal total delay for all lines. As mentioned in Sec. 1.1, however, they are not "fail safe" methods; any change in the line characteristics[9] will give an undetected error in the phase angle indications.

It was to overcome this serious difficulty that the possibility of continuous repetitive transmission delay measurement was investigated. This uses the transponder system, with test pulses from the Control Centre synchronized with, and falling between, the phase angle measurement pulses generated at the substations. It was found possible to measure the two-way transmission path delay using test pulses at supply frequency at the same time as phase-angle measurement was proceeding, and to actuate an alarm when this delay deviated from a standard value by more than a chosen amount : this provided a solution to the "fail safe" problem. It was then realized that rather than use this delay measurement to check the accuracy of the extra delay added to each line, it could be used itself to provide the delay correction necessary. To do this, however, requires some means of storing the results of the measurement, for correction of the phase-angle measurement later in the cycle of supply voltage. This is satisfactorily accomplished in the system developed,[22] which has the advantage that as no added delay circuits are used, there is no initial setting-up to carry out, or periodic checking required.

6.1 SYSTEM OPERATION

In each substation, the 50 Hz voltage to be used for the measurement is applied to a voltage comparator, which gives an output pulse each time the voltage passes through zero, when changing from negative to positive values. The comparator output is used to initiate, with negligible delay, the generation of voltage pulses of accurately defined waveform, which are delivered to the pilot line. These pulses, which will henceforth be called "primary pulses", are transmitted via the pilot lines to the Control Centre, suffering a time delay and a change of waveform of amount depending upon the length and electrical characteristics of the lines. Upon arrival at the Control Centre, the primary pulses are applied to a voltage comparator, giving an output pulse each time the received voltage rises to a predetermined reference value V_{ref}. It is from these latter pulses that the phase measurement is made.

The sequence of events is shown in Fig. 4 : the 50 Hz voltages at the two substations A and B are shown in (a) and (b); they are assumed to differ in phase by an angle ϕ. The primary pulses delivered to the pilot lines are shown in (c) and (d); these are separated in time by t_ϕ, corresponding to the phase angle ϕ. The primary pulses arriving at the Control Centre are shown in (e) and (f) ; these will be delayed on the pulses in (c) and (d) by the transmission delay times t_A and t_B respectively, which will depend upon the pilot line characteristics. The output pulses from the voltage comparators in the Control Centre are shown at (g) and (h) : they are separated in time by $t_\phi + (t_B - t_A)$.

6.2 Measurement of $(t_B - t_A)$

This measurement is carried out by generating, in the Control Centre, pulses of voltage of accurately defined waveform similar to those delivered to the pilot lines at each substation, as described in the preceding Section. These pulses, which will henceforth be called "secondary pulses", are generated at a suitable time T_s after the arrival of the primary pulse from substation A, and are delivered simultaneously to the pilot lines connected to the substations A and B; during transmission to the substations, the pulses suffer delay and waveform distortion dependent upon the line characteristics. On arrival at a substation, the secondary pulses are applied to a voltage comparator, adjusted to give an output pulse when the line voltage reaches the same value V_{ref} to which the line voltage comparators in the Control Centre are set. Figure 5 illustrates the operation: the pulses generated at the Control Centre and fed to the pilot lines are shown at (a) and (b); the pulses received by substations A and B are shown at (c) and (d), and the output pulse from the voltage comparators at these substations are shown at (e) and (f). These latter pulses will be delayed on the pulses in (a) and (b) by the reverse transmission time delays t'_A and t'_B.

The output pulses from the voltage comparator in each substation are applied to a delay device, which gives an output pulse a known and constant time T_d after the receipt of each trigger pulse from the comparator. It is important that T_d be the same for all substations. The output pulses from the delay device are used to initiate the generation of voltage pulses of waveform similar to the primary pulses, and these are delivered to the pilot lines. These pulses will be called the "tertiary pulses", and are shown in (c) and (d) of Fig. 5. During transmission from the substations to the Control Centre, the tertiary pulses will be delayed and distorted in a similar manner to the primary pulses.

When they actuate the voltage comparators in the Control Centre, therefore, the time difference t_C between the output pulses from the comparators will be

$$t_C = (t'_B + t_B) - (t'_A + t_A), \qquad \text{----} \quad (6.2.1)$$

assuming that the time delays T_d in the substations are equal. This is shown in (a) and (b) of Fig. 5.

The measurement of $(t_B - t_A)$ is based on the equality of forward and reverse transmission time delays for a given line, even when that line is composed of several sections having differing electrical characteristics. It is important, therefore, to know that this is true for all lines likely to be used. Analysis of a discontinuous line is difficult, and although some attempts have been made [43, 44] they apply only to certain special configurations or characteristics of the lines. A general reciprocity theorem for linear circuits is, of course, well known; [45] however, it is perhaps useful to investigate the reciprocal delay properties of composite lines in particular. Consider the line shown in Fig. 5A. Here, the sections have characteristic impedances $Z_1, Z_2, \ldots\ldots Z_n$, attenuations $A_1, A_2, \ldots\ldots A_n$, and delay times $\tau_1, \tau_2, \ldots\ldots \tau_n$, respectively. Assume that $E_2 = 0$, and voltage pulse $E_1 = E$ is generated: a voltage v_0 will be delivered to the line, at node N_0, where

$$v_0 = \frac{Z_1 E}{(Z_0 + Z_1)} \qquad \text{----} \quad (6.2.2)$$

As it travels along the first section of the line this voltage will be delayed and attenuated, and there will be a reflection at the junction with the second section at node N_1. Let the voltage reflection coefficient at node N_j between any section j and the succeeding section k be ρ_{jk}, where

$$\rho_{jk} = \frac{Z_k - Z_j}{Z_k + Z_j} \quad , \qquad \text{---- (6.2.3)}$$

On arrival of the pulse, the voltage at node N_1 will be

$$v_1 = \frac{Z_1 E\ (1+\rho_{12})}{(Z_0 + Z_1)\ A_1} = \frac{(1+\rho_{01})\,(1+\rho_{12})E}{2A_1} \qquad \text{---- (6.2.4)}$$

and this will be the input voltage to section 2 of the line. However, there will be a further input to this section at a time $2\tau_1$ later, caused by the component of v_1 reflected from node N_0. Also, as the voltage pulse travels along the line, there will be additional multiple reflections from the subsequent nodes. The voltage v_n will therefore consist of two components:

(a) a primary component resulting from direct transmission along the line.

(b) a secondary component resulting from the sum of all reflections between nodes.

Considering, for the present, the primary component only, the Laplace transform equation for v_n is

$$v_n = \frac{(1+\rho_{01})(1+\rho_{12})(1+\rho_{23})\ldots(1+\rho_{(n-1)n})Z_0 E\ \varepsilon^{-s(\tau_1+\tau_2+\ldots\tau_n)}}{(A_1A_2A_3\ldots A_n)\,(Z_n+Z_0)}$$

$$= \frac{(1+\rho_{01})(1+\rho_{12})(1+\rho_{23})\ldots(1+\rho_{(n-1)n})(1+\rho_{n0})E\ \varepsilon^{-s(\tau_1+\tau_2+\ldots\tau_n)}}{2(A_1A_2A_3\ldots A_n)}$$

$$\text{---- (6.2.5)}$$

Consider now the case when $E_1 = O$, and the voltage pulse $E_2 = E$ is generated. The transform equation for v_0 is

$$v_0 = \frac{(1+\rho_{0n})(1+\rho_{n(n-1)})\ldots.(1+\rho_{32})(1+\rho_{21})(1+\rho_{10})E\,\varepsilon^{-s(\tau_n+\ldots\tau_2+\tau_1)}}{2(A_nA_{(n-1)}\ldots.A_3A_2A_1)} \qquad \text{---- (6.2.6)}$$

Noting that $\rho_{jk} = -\rho_{kj}$, then from (6.2.5) and (6.2.6)

$$\frac{v_n}{v_0} = \frac{(1+\rho_{01})(1+\rho_{12})(1+\rho_{23})\ldots.(1+\rho_{(n-1)n})(1+\rho_{n0})}{(1-\rho_{n0})(1-\rho_{(n-1)n})\ldots.(1-\rho_{23})(1-\rho_{12})(1-\rho_{01})} \qquad \text{---- (6.2.7)}$$

But from (6.2.3)

$$\frac{(1+\rho_{jk})}{(1-\rho_{jk})} = \frac{Z_k}{Z_j} \qquad \text{---- (6.2.8)}$$

Substituting this into (6.2.7) gives

$$\frac{v_n}{v_0} = \frac{Z_1Z_2Z_3\ldots.Z_{(n-1)}Z_nZ_0}{Z_0Z_1Z_2Z_3\ldots.Z_{(n-1)}Z_n} = 1 \qquad \text{---- (6.2.9)}$$

Thus, the primary component of the voltage received, for a given voltage delivered to the line, is unaffected by reversal of the direction of propagation of the voltage along the line.

The effect of the secondary component of the received voltage can be understood by considering the composite line of Fig. 5B, which may be regarded as the line of Fig. 5A to which the extra section x has been inserted between sections j and k. This extra section will cause an increase in the total attenuation and time delay of signals propagated along the line, and it will also cause additional reflections from the nodes j and x to which it is connected. Consider,

as before, the case when $E_2 = O$ and a voltage pulse $E_1 = E$ is generated. The transform equation for the voltage pulse developed at node j and arriving at node x is

$$v_j = \frac{(1+\rho_{01})(1+\rho_{12})(1+\rho_{23})\ldots(1+\rho_{ij})\, E\, \varepsilon^{-s(\tau_1+\tau_2+\ldots\tau_x)}}{2(A_1A_2A_3\ldots A_jA_x)} \qquad \text{---- (6.2.10)}$$

There will be a succession of reflections between nodes x and j, resulting in a series of reflected pulses being delivered to node x, the m^{th} such pulse being

$$v_{xm} = \left[\frac{\rho_{xk}\rho_{xj}\,\varepsilon^{-2s\tau_x}}{A_x^2}\right]^m v_j \qquad \text{---- (6.2.11)}$$

Thus, the secondary component of v_n corresponding to this m^{th} reflection will be

$$v_{nm} = \left[\frac{\rho_{xk}\rho_{xj}\,\varepsilon^{-2s\tau_x}}{A_x^2}\right]^m \frac{(1+\rho_{01})(1+\rho_{12})\ldots(1+\rho_{jx})(1+\rho_{xk})\ldots(1+\rho_{no})\,E\,\varepsilon^{-s(\tau_1+\tau_2\ldots\tau_n)}}{2(A_1A_2\ldots A_jA_xA_k\ldots A_n)} \qquad \text{.... (6.2.12)}$$

Now consider the case when $E_1 = 0$, $E_2 = E$. By similar reasoning to the above, the secondary component of v_0 corresponding to the m^{th} reflection between the nodes j and x will be

$$v_{om} = \left[\frac{\rho_{xj}\rho_{xk}\,\varepsilon^{-2s\tau_x}}{A_x^2}\right]^m \frac{(1+\rho_{on})(1+\rho_{n(n-1)})\ldots(1+\rho_{kx})(1+\rho_{xj})\ldots(1+\rho_{10})\,E\,\varepsilon^{-s(\tau_n+\ldots\tau_2+\tau_1)}}{2(A_nA_{(n-1)}\ldots A_kA_xA_j\ldots A_1)} \qquad \text{.... (6.2.13)}$$

Thus,

$$\frac{v_{nm}}{v_{0m}} = \frac{(1+\rho_{01})(1+\rho_{12})\ldots(1+\rho_{jx})(1+\rho_{xk})\ldots(1+\rho_{(n-1)n})(1+\rho_{n0})}{(1+\rho_{0n})(1+\rho_{n(n-1)})\ldots(1+\rho_{kx})(1+\rho_{xj})\ldots(1+\rho_{21})(1+\rho_{10})} \quad \text{---- (6.2.14)}$$

Making the same substitutions as were used in deriving equations (6.2.7) and (6.2.9), we again get

$$\frac{v_{nm}}{v_{0m}} = 1 \quad \text{---- (6.2.15)}$$

We see, therefore, that when the extra section of line is inserted, the additional secondary component of received voltage, caused by reflections between nodes to which the extra section of line is connected, is independent of the direction of propagation of the primary component along the line.

If we regard a composite line as being made by the successive addition of sections to a single uniform section of line, then each such addition will cause its own set of secondary components in the received voltage. Since it has been shown that both these and the primary component are independent of the direction of propagation, it follows that the total voltage received, when a given pulse is delivered to the line, is unaffected by reversal of the direction of transmission along the line. This implies that the forward and reverse transmission time delays are equal, since they are defined as the time between transmission of the pulse, and the instant the received voltage attains the value V_{ref}. This result is supported by the experiments on typical pilot lines described in Sec. 14.3.

Assuming the two transmission delays are equal, then

$$t_{A'} = t_{A'} \qquad t_{B'} = t_{B'}$$

and $$t_C = 2(t_B - t_A) \qquad \text{----} \quad (6.2.16)$$

This creates the need to divide the time difference t_C by two, and to store the result until the receipt of the next primary pulse at the Control Centre. It was found that attempts to develop a circuit to perform this operation directly did not lead to rapid progress. A solution to the problem was found in the use of the meter inertia (together with the filter F, Fig. 1) to perform the storage operation, and by making the line delay measurement on alternate cycles of the supply frequency only, as described in the next Section.

6.3 Correction for transmission delay error.

The method used to correct the phase angle indications for difference in transmission path delay is illustrated in Fig. 6, which gives the sequence of operation at the Control Centre over one cycle of the supply voltage. Primary pulses from the substations are received at the Control Centre as shown at (a) and (b); these are applied to the voltage comparators VCA and VCB, the output voltages of which are shown at (c) and (d). The current I flows in the meter circuit, as described in Sec. 4.3, for a duration $t_\phi + (t_B - t_A)$ in each cycle of the supply voltage. The secondary pulses generated at the control Centre are delayed by T_S on the

primary pulses received by VCA, as shown at (a) and (b) : these pulses inevitably actuate the comparators VCA and VCB, as shown by dotted lines in the Figure, but this action has no significant effect. The tertiary pulses from the substations are received at the Control Centre and the output from the voltage comparators are as shown at (d) and (e): these are arranged to operate a second set of positive and negative current generators, similar to those described in Sec. 4.3, which deliver an additional current pulse of amplitude I_X to the meter circuit. The average total current is thus

$$I_{av} = fI\left[t_\phi + (t_B - t_A)\right] + 2fI_X(t_B - t_A) \quad \text{---- (6.3.1)}$$

By choosing $I_X = \frac{-I}{2}$

then, $I_{av} = fIt_\phi$, ---------- (6.3.2)

i.e. the effect of the transmission delay on the meter indication is cancelled out.

The system described above, which was used in the F. T. M. version of the Control Centre equipment, requires two sets of positive- and negative - current generators : one set is used to measure $t_\phi + (t_B - t_A)$, and generates current of amplitude I, while the other set is used to measure $2(t_B - t_A)$ and generates current of amplitude I/2. An alternative to the use of separate half- and full - current generators is to choose $I_X = I$, and transmit secondary pulses on alternate cycles of the supply voltage only. This latter arrangement, which is used in the M. S. E. V. equipment, has the advantage that a common pair of current generators can be used for both phase angle measurement and transmission delay correction. There is also the advantage of a reduction by one - third in the total signalling power carried by the pilot line. The disadvantage is that with the half - supply frequency current pulse flowing in the meter circuit, there is a greater tendency for vibration of the needle; this effect has been eliminated by appropriate design of the low-pass filter F (Fig. 1).

7.1 SUBSTATION TIME DELAY

The secondary pulse transmitted from the Control Centre is received at the substation after a time equal to the transmission delay. Before the tertiary pulse is generated at the substation, it is necessary that sufficient time should elapse to allow the pilot line and its associated transformers to become discharged. A time-delay generator is therefore used to trigger the tertiary pulse generator at a time T_d after the receipt of the secondary pulse.

It is important that the period T_d of the time delay generators in all substations should be equal. Suppose there is an error ΔT_d in the period at one substation; this will cause an equal error in the duration of the transmission-delay-correction current pulse at the Control Centre, and there will therefore be an error in the phase angle indication of

$$\Delta\phi = 180 f \Delta T_d \quad \text{degrees} \qquad \text{------} \qquad (7.1.1)$$

As described in Sec. 12, a value of T_d of approximately 5 msec. is required : for a permissible error $\Delta\phi = 1/20$ degree, the allowable error in T_d, expressed as a fraction, is therefore

$$\frac{\Delta T_d}{T_d} = \frac{0.05}{180 \times 50 \times 0.005} = 0.0011 \qquad (7.1.2)$$

It is clear that a time-delay generator with period defined by combinations of inductance, capacitance and resistance is unlikely to give the required long-term accuracy, and in the equipment developed, a quartz crystal has been used as the timing standard.

7.2 Substation Time Delay Generator

A block diagram of the time delay generator is shown in Fig. 7. The crystal oscillator X generates a continuous train of short-duration pulses of frequency f_o, which are gated into a series of cascaded binary counters B_1 to B_n, to generate the required time period T_d. Each time that a secondary pulse is received at the substation, the bistable element B_0 is triggered to the "1" state, enabling the gate G to transmit the crystal-oscillator pulses to the element B_1, which is the first of the series of n cascaded binary counters. Assuming these counters to be initially all in the "0" state, they will be again in that state after 2^n pulses have been received by B_1. The change in the output of B_n, when returning to the "0" state, triggers B_0 to the "0" state also; the gate G then closes. The output of B_0 is the pulse of period T_d required.

There is a possibility of error in the period of pulses generated in this way. Since there will, in general, be no coherence between the crystal oscillator pulses and the time that B_0 is triggered by the voltage comparator, the gate G may open at any point between pulses 0 and 1 in Fig. 8, and will close at the 2^{nth} pulse : the period may therefore vary between the limits $2^n/f_o$ and $(2^n - 1)/f_o$, and there will be a corresponding variation in the timing of the secondary pulses. The effect of this on the phase angle indication will usually average out, but if a harmonic of f is sufficiently close to f_o for the difference frequency to be within the pass band of the meter and associated filter F in the Control Centre equipment, the varying error in T_d will cause a fluctuation in the meter indication. The fluctuations will be caused by variations in the duration of the transmission-delay-correction current pulse, which is affected by variations in T_d in both substations : there is therefore the possibility of a total error in the duration of this pulse of $\pm 1/f_o$, corresponding to an error in phase angle of

$$\delta\phi = \pm \frac{180f}{f_o} \text{ degrees} \qquad \text{-------} \qquad (7.2.1)$$

This error may thus be made as small as desired by the use of a sufficiently high oscillator frequency, and an appropriately large number of binary stages. Assuming that the error is to be no greater than $\pm$ 1/10 degree, the crystal oscillator frequency must be not less than

$$f_o = 1800f = 90,000 \text{ Hz} \qquad \text{-------} \qquad (7.2.2)$$

To obtain the required value of T_d, a frequency of 100 kHz was chosen, which, together with nine binary stages, gives a mean period of

$$T_d = \frac{(2^n - \frac{1}{2})}{f_o} = 5.115 \text{ msec.} \qquad (7.2.3)$$

The components associated with the time-delay generator are a substantial fraction of the total used in the substation equipment. It is tempting to replace the system of binary stages described above with a simpler arrangement : one possibility would be of a multivibrator - type circuit, with a natural period somewhat longer than that required; the crystal oscillator pulses would then be used to synchronize the multivibrator frequency to an appropriate submultiple of the crystal frequency.[23] Another possibility would be the use of a diode-pump type of frequency divider.[24] Of the many arrangements considered, most had the disadvantage that an incorrect division ratio was possible; as this could cause an undetected error in the phase angle indication, the "fail- safe" requirement precluded the use of circuits of this type. The apparent complexity of the nine binary stages could, of course, be reduced by a large-scale integration form of construction, all of the stages being diffused on one chip of silicon : at the time that the equipment was developed, however, integrated circuits of this type were not commercially available.

7.3 Repetitive Substation Time Delay Measurement

The desirability of a reduction in the complexity of the substation equipment led to a search for a system to remove the necessity for the accurately-known time delay described in the previous Sections. There are several systems possible which need delay devices of only moderate accuracy and stability : in these the value of the delay time is measured repetitively, and the results of the measurement are used to make an appropriate correction to the phase angle indication.

The operation of one such system is shown in Fig. 9, which shows the pilot line voltage waveforms of substations A and B at (a) and (b), and the voltage on pilot lines A and B in the Control Centre at (c) and (d), respectively. The current in the meter circuit is shown at (e). One cycle of operation requires two cycles of the supply voltage to complete : in the first cycle shown in Fig. 9, the secondary pulses are transmitted from the Control Centre, and the tertiary pulses are returned at times $(T_{dA} + 2t_A)$ and $(T_{dB} + 2t_B)$ later, where T_{dA} and T_{dB} are the periods of the substation time delay generators. These tertiary pulses are used to generate a current pulse in the meter circuit, as described in Section 6.3: the amplitude of these pulses, however, is twice the amplitude of the current pulse generated from the primary pulses. In the second cycle of the supply voltage, the secondary pulses are transmitted as in the previous cycle, but the time delay generators are triggered twice before the tertiary pulse is generated: the tertiary pulses are then used to generate a current pulse in the meter circuit of amplitude equal to the primary pulses. The average meter current, taken over two cycles of the supply voltage, is thus

$$I_{av} = \frac{2\left[t_\phi + t_B - t_A\right] I - \left[T_{dB} - T_{dA} + 2(t_B - t_A)\right] 2I}{2/f} +$$

$$\frac{\left[2(T_{dB} - T_{dA}) + 2(t_B - t_A)\right] I}{2/f} \quad \text{---} \quad (7.3.1)$$

giving

$$I_{av} = fIt_\phi \quad \text{----------} \quad (7.3.2)$$

i.e., an average meter current independent of transmission delay and period of the substation delay generators.

A serious disadvantage of this system is the long time occupied by the double delay $2T_{dA}$ and $2T_{dB}$ in the second cycle; it is difficult to design the system to ensure that when used with long pilot lines, the lines will be sufficiently discharged before a pulse is received. Also, although no crystal oscillator is needed, the benefits of eliminating the binary dividers are largely outweighed by the additional logic circuits necessary.

A better system is shown in Fig. 10. Again, two cycles of the supply voltage are required for one cycle of operation; in the first cycle the action is the same as in the previous system, except that the current pulses in the meter circuit controlled by the primary and secondary pulses are of equal amplitude. In the second cycle, pulses P_A and P_B are sent from the substations to the Control Centre, at times T_A and T_B after the primary pulses : these times do not need to be accurately defined, they are approximately equal to T_s, (Sec. 6.3). Coincident with the generation of the pulses P_A and P_B, the time delay generators are triggered, and on completion of their periods further pulses $P_{A'}$ and $P_{B'}$ are transmitted to the Control Centre. These are used to control the generation of current pulses in the meter circuit, as shown at (e) in Fig. 10. The meter current, averaged over two cycles, is then

$$I_{av} = \frac{2\left[t_\phi + t_B - t_A\right] I - \left[T_{dB} - T_{dA} + 2(t_B - t_A)\right] I}{2/f}$$

$$- \frac{\left[t_\phi + T_B - T_A + t_B - t_A\right] I}{2/f}$$

$$+ \frac{\left[t_\phi + T_B - T_A + t_B - t_A + T_{dB} - T_{dA}\right] I}{2/f} \quad -- (7.3.3)$$

giving

$I_{av} = fIt_\phi$, as in the previous system.

This system has the disadvantage that extra logic circuits are required in the Control Centre equipment to generate the current pulses in the second cycle. Also, the meter current pulses need to be defined with greater accuracy than in the previous systems, as the correction for the time difference $(T_{dB} - T_{dA})$ is achieved by subtraction of the currents controlled by the pulses P_A and P_B, and $P_{A'}$ and $P_{B'}$ in the second cycle. When the phase angle is large, the long duration of these current pulses demands that the positive and negative current amplitudes be closely matched, if an appreciable error in the phase indication is to be avoided. The advantage of the system is in the simplified substation circuits, and as there are many substations associated with each Control Centre, an overall improvement in cost and reliability might be expected.

It is a matter for some regret that the discovery of this system was not made at an earlier stage in the project. By the time that its possible advantages became apparent, the development and field trials of the crystal-controlled delay equipment were so well advanced that the time needed to explore the possibilities of the system could not be justified.

8.1 SUBSTATION EQUIPMENT LOGIC SYSTEM

A logic diagram of the substation equipment is shown in Fig. 11, and the sequence of essential operations in Fig. 12. The 50 Hz voltage of which phase measurement is to be made is applied to the voltage comparator FC, which gives an output voltage step each time the test voltage passes through zero value, with positive-going polarity, as shown in (b), Fig. 12. This voltage step is applied, via the OR gate G_3, to the monostable multivibrator M_{13}; the resulting output pulse from M_{13}, suitably amplified by A, is delivered to the pilot line by the transformer T, and is the primary pulse as defined in Sec. 6.1.

On receipt of a secondary pulse from the Control Centre, a step of output voltage from LC occurs when the voltage applied to it reaches the value V_{ref} (Sec. 6.1). This "sets" the bistable multivibrator B_0, allowing pulses from the crystal oscillator X to trigger the chain of binary counters B_1 - B_9, and resulting in B_0 being "reset" after a time T_d, as described in Sec. 7.2, and shown in Fig. 12e. The output voltage step from B_0 is used to trigger M_{13} via the gate G_3, resulting in the generation of the tertiary pulse (Sec. 6.1).

The pulses generated by M_{13} and A and delivered to the pilot line are inevitably delivered also to LC, as shown in Fig. 12d. The function of the time delays D_2 and D_1 is to prevent the triggering of B_0 from the primary and tertiary pulses, respectively: if this were to be permitted, there is a possibility that B_0 might become self-triggering, with the result that a continuous train of pulses of frequency $1/T_d$ would be sent to the Control Centre.

The system of operation described above was used in the F.T.M. substation units. However, when the M.S.E.V. version of the equipment was designed, the logic system was altered slightly, to exploit the capabilities of the integrated circuits used. This revised system is described in Section 22.

8.2 CONTROL CENTRE EQUIPMENT LOGIC SYSTEM

The arrangement of the logic in the Control Centre equipment is shown in Fig. 13, with the operating sequence in Fig. 14. The signals from the two substations are received on lines A and B, and are applied to the voltage comparators VCA and VCB via the transformers TA and TB. The voltage comparators and the transformers have identical characteristics to LC and T in the substation equipments.

Consider the case when the 50 Hz voltage at substation A leads that at substation B, and where the transmission delay t_B is greater than t_A; this condition is shown in Fig. 14. Before the arrival of the primary pulses from the substations, the output voltage of each element has the logic polarity shown in the square to which the output is connected.

When a primary pulse is received by the voltage comparator VCA, the output voltage pulse is applied to the AND gates G2A and G1A. As one of the inputs of G2A is at logical "0", the output of this gate remains at "0". All of the inputs of G1A are at "1", however, and the resulting output pulse from this gate triggers the monostable multivibrator M4, causing the current generator PCG to deliver a current pulse to the meter M, as described in Sec. 4.3 and Figs. 1 and 2, and as shown at (c) and (j) in Fig. 14. Upon the arrival of a primary pulse at the voltage comparator VCB, the output voltage pulse is applied to the AND gates G2B and G1B. The gate G2B is held closed by the "0" polarity of one of its inputs; the output of this gate therefore remains at "0". The gate G1B is, however, opened by the pulse from VCB, and the resulting output voltage pulse is applied to the bistable multivibrator B22, which is triggered to the "set" condition (Fig. 14d). As described in Sec. 4.3, this causes the termination of the meter current pulse (Fig. 14j).

The monostable multivibrator M4 has two functions. One of these is to provide a trigger pulse to reset B22; for this, the period T_4 of the multivibrator is unimportant so long as it is greater than the time corresponding to the maximum phase angle to be measured (see Sec. 4.3). This multivibrator has therefore been used also to define the instant at which the secondary pulse is transmitted. On completion of the period T_4, the monostable multivibrator M2 is triggered via B23 and M1, and the secondary pulse is generated : this is delivered to the lines A and B after amplification by AA and AB respectively. The element B23 is a binary divider, and M1 and M2 are thus triggered only on alternate pulses from M4 : the secondary pulses are thus transmitted at a frequency equal to one half of the supply frequency, as described in Sec. 6.3, and shown in Fig. 14g.

The element M1 is a monostable multivibrator, with a period sufficiently long that it is still in the triggered state when the tertiary pulses are received by VCA and VCB : the output pulses from these voltage comparators are thus diverted into M3 and MB21 respectively. The action of the latter elements is analogous to M4 and B22, in that they cause a meter current pulse to be generated by the current generator NCG: this pulse has a duration equal to the difference in time of arrival of the tertiary pulses at VCA and VCB, as required in the system of Sec. 6.3. The long-period monostable multivibrator MB21 may be regarded as a bistable device for this mode of operation : as is described in Sec. 9, the monostable property is provided only as a precaution against malfunction under certain fault conditions.

The logic delays D1 and D2 are provided to ensure that the gates G1A and G1B are not closed by the changing state of M4 and B22, until the triggering of these elements is complete. The delays D3 and D4 are necessary to prevent the unwanted triggering of M3 and MB21 by the secondary pulses. When M1 is triggered, there is sufficient delay in the amplifiers AA and AB, and the transformers TA and TB, to ensure that the gates G1A and G1B are

closed by the signal from M1 before the secondary pulse output from VCA and VCB is received by the gates. M4 and B22 are therefore not triggered by these pulses.

The logic elements shown in Fig. 13, but whose function is not described in detail above, are required to satisfy the "fail safe" conditions, as explained in the next Section.

9.1 "FAIL SAFE" PRECAUTIONS

As stated in the specification for the system, Sec. 3.1, it is important that malfunction should not allow an erroneous phase angle to be indicated. It will be appreciated that it is virtually impossible to make equipment of this type completely "fail-safe" : some contingency can always be envisaged which will nullify the precautions taken. The probability of a failure can, of course, always be reduced by the use of duplicate or triplicate sets of equipment : ultimately the limit is set by economic considerations. However, it has been possible to design this equipment so that the possibility of an undetected failure is remote, and almost certainly much less than the likelihood of failure in the pilot lines and other apparatus in conjunction with which the equipment is to be used. The duplication of the whole or part of the equipment in order still further to improve the reliability would therefore seem scarcely justifiable, and no provision for this redundancy has been made.

The system developed has been arranged so that most fault conditions result in the meter indicating off-scale. There are a few possible fault conditions, however, where this action is not obtainable; one such condition can occur when both pilot lines become disconnected. In these cases, some additional means of fault indication is necessary, and this is provided by a pair of warning lamps. During normal operation, only the green lamp glows; if a fault occurs, the red and green lamps glow alternately for a period of about one half second each.

This action is obtained by the elements A and D in Fig.13. The element A is an astable multivibrator, to which the indicating lamps are connected. The oscillations of A can be arrested by the clamp element D, which rectifies the voltage from the output of MB21 and applies this to the inhibiting input on A. Thus, the green lamp only will be energised when MB21 is operating repetitively; should the state of this element cease to alternate, the voltage

rectified by D will fall to zero and A will commence oscillations. Clearly, for the lamp indications to be meaningful, the reliability of D and A is of first importance, and the precautions taken to ensure this are described in Sec. 21.

9.2 Action under various fault conditions

(a) In the case of failure of all signals from substation A, but with B operating normally, M4 will not be triggered; secondary pulses will not be generated and there will thus be no tertiary pulses. MB21 will therefore be quiescent, and there will be no inhibiting output from D. The lamps will then glow alternately, indicating the fault condition. The pulses from substation B will cause the element B22 to be triggered, which will remain in the "set" state : NCG will then deliver a continuous current to the meter, which will normally read off-scale. If, however, the input from substation A fails at a time between the reception of the primary and tertiary pulses, M3 will not be triggered : MB21 will then be "set" by the tertiary pulse from substation B, causing the operation of PCG. Both NCG and PCG will then be simultaneously delivering current to the meter, and the sum of these currents will be zero, giving a false phase angle indication of zero degrees. Regarding MB21 as a bistable, or a monostable, multivibrator, the warning lamps will glow alternately, as the absence of secondary and tertiary pulses ensure that MB21 is quiescent. However, by the use of a long-period monostable multivibrator for this element, the current from PCG will cease on the termination of its period, and the meter will then indicate off-scale. This provides a double safeguard against misinterpretation by the operator of the equipment.

(b) In the case of failure of all signals from substation B, with A operating normally, M4 will be triggered, and secondary pulses will be transmitted. B22 will not be triggered; the current pulses generated by PCG will therefore have a duration equal to the period of M4, and the meter will indicate off-scale. MB21 will not be triggered either, and the signals from the warning lamps will alternate.

(c) If the tertiary pulse generator in substation A fails, M3 will not be triggered. If tertiary pulses are being received from substation B, MB21 will be triggered, and the green lamp will glow. The current pulses generated by PCG via G3 will then have a duration equal to that of the period of MB21 : this period must therefore be long enough to cause sufficient average meter current to give off-scale deflection, in the presence of the current that may be generated by NCG acting in its phase angle measurement role.

(d) Failure of the tertiary pulse generator in substation B will prevent the triggering of MB21: the warning lamps will then indicate the fault condition.

(e) Nearly all possible faults in the Control Centre equipment are equivalent to and covered by the previous cases. Other possible causes of failure are in the current-generator amplitude I and the voltage-comparator level V_{ref}. In view of the simplicity of these circuits, which are described in Sec. 20 and Sec. 18 respectively, it is likely that any significant changes in their characteristics will be slow, and easily identified in routine checking.

(f) No safeguard against errors in the meter has been included. Long-term changes in accuracy should be shown up by routine tests. Total failure of the meter, however, will cause a zero phase indication whatever the value of phase angle; the system is thus not "fail-safe" against this type of failure. The likelihood of total failure of the meter is small, and it was decided, therefore, that the provision of a duplicate meter was not justified. If zero phase angle is indicated, the operator will be instructed to switch momentarily to another pair of substations giving a non-zero phase indication.

9.3 Pilot line reversal indication

After the equipment has been installed and put into service, it may be necessary to replace or re-route the pilot lines, owing to failure of the lines or some operational requirement of the power distribution system. When this is done, there is the possibility that the new line will be connected with reversed polarity; the effect will then be to trigger the voltage comparators associated with that line by the overswing voltage caused by the transformer, rather than by the leading edge of the line voltage pulse. The operation of the logic circuits will thus be delayed by a time approximately equal to the line pulse duration; as the duration of this pulse corresponds to a phase angle of about 4^{o} at 50 Hz, there could be a serious error in the phase angle indication. Additional circuits have therefore been included to give warning should this line polarity reversal occur, and these are shown in Fig. 13. Considering line A, the line voltage, after transformation by TA, is applied to the voltage comparators VCA and VCA'. VCA is arranged to have the reference voltage $+V_{ref}$, as described in Sec. 6.1 : VCA' has a reference voltage of approximately the same magnitude but of opposite polarity.

In normal operation, when the incoming pulse from the substation is received, its positive - going leading edge causes an output voltage step from VCA, which is applied to G1A. VCA' is in the "0" state, and the output from the inverter IA therefore enables M4 to be triggered from the VCA signal. On termination of the input pulse, the resulting voltage overswing causes an output voltage step from VCA', but this has no effect on the operation of the circuits. With the pilot line reversed, the leading edge of the incoming voltage pulse is negative - going, with the result that VCA' is actuated first, causing the output of IA to be "0". On termination of the pulse, the overswing then actuates VCA. However, the resulting step in output voltage cannot trigger M4, as, owing to the delay D5, the gate G1A is still closed by the previous action of VCA'. The effect is thus equivalent to a cessation of signals from

line A, and a warning is given as in Sec. 9.2 (a) above. A similar action occurs when line B is reversed.

10.1 TRANSMITTED PULSE WAVEFORM

The accuracy of phase angle measurement, and the compensation for transmission path delay, depend upon the generation of primary, secondary and tertiary pulses of similar waveform, as discussed in Sec. 6.1. Not all parts of the transmitted waveform need to be closely controlled, however. When the received voltage reaches the comparator reference level V_{ref}, the logic circuits are triggered and the subsequent waveform of the received signal is of little consequence. The leading edge of the transmitted pulse must therefore be accurately defined, and sufficient of the remainder of the pulse as is required to develop the value V_{ref} in the received voltage on the "worst-case" pilot line.

For the lines in use by the M. E. B., there are no mandatory restrictions on the bandwidth of the transmitted signal, and there is therefore no objection to the leading edge of the pulse approximating to a step waveform. An advantage of this type of signal is the ease and precision with which it may be generated : it also has the advantage of using the whole of the bandwidth of the line and associated transformers; this results in the maximum rate of rise of the received voltage, and consequently the least error in timing, should the comparator reference voltage vary from the nominal value V_{ref}. However, the design requirements of the line transformers, as described in Sec. 11, cause a restriction of the bandwidth of frequencies transmitted to those in the audio range. The rate of rise of received voltage is then still sufficient to ensure that only a low value of timing error is possible. The restriction in bandwidth has the merit of reducing the possibility of crosstalk from the pilot line to adjacent lines which are being used perhaps for other services. With the bandwidth transmitted, the problem of crosstalk would appear to be little more serious than that existing between circuits carrying speech signals of equivalent power level.

10.2 Transmitted Pulse Duration

The duration t_p of the transmitted pulse must be sufficient to allow the received pulse, after transformation, to reach an amplitude equal to V_{ref}. To permit the use of the equipment on long lines, it is undesirable that the pulse duration should be so short that the received pulse does not achieve its full amplitude. On the other hand, too great a pulse duration will result in the build-up of excessive magnetic energy in the line transformers, with a resulting extended overshoot of the line voltage, as discussed in the next Section. Assuming that the lowest upper cutoff frequency f_o of the line and transformer combination corresponds to the present specification for many speech circuits, namely, 3400 Hz, and assuming further that the frequency response has a shape similar to that given by a single RC circuit, we have

$$CR = 1/2\pi f_o = 1/2\pi . 3400 = 46.8\ \mu\text{sec.} \quad \text{---} \quad (10.2.1)$$

This will be the time constant of the exponential rise in received voltage when a voltage step is transmitted, when the above assumptions are true. For the received voltage to rise to within 2% of its final value, the duration of the pulse must therefore be

$$t_p = 4CR = 4 \times 46.8 = 187.2\ \mu\text{sec.} \quad \text{----} \quad (10.2.2)$$

A pulse duration of nominally 200 μsec. has therefore been chosen, and the suitability of this choice has been confirmed by tests on the many pilot lines provided by the M. E. B.

10.3 Transmitted Pulse Amplitude

The amplitude of the transmitted pulse will affect the maximum permissible length of pilot line for satisfactory operation of the equipment: a large amplitude is therefore desirable if long lines are to be used. The upper limit of amplitude allowable is, however, limited by the possibility of cross-talk with adjacent lines, which may be in use for purposes other than phase angle measurement. It is somewhat difficult to decide what the maximum pulse amplitude should be, as no regulations exist for the pilot line to be

used, when a pulse signal is to be transmitted. If the amplitude of the pulses transmitted from substation and Control Centre is V_p, then the mean power P_{av} delivered to the pilot line of characteristic impedance Z_o is

$$P_{av} = \frac{V_p^2}{Z_o} (N_{cc} + N_{ss}) \frac{t_p}{2/f} \qquad \text{--------} \qquad (10.3.1)$$

where N_{cc} and N_{ss} are the number of pulses transmitted from the Control Centre and substation respectively, during two cycles of the supply voltage. For 200 μsec. pulses of 10V amplitude, the mean power delivered to a line of 1000 ohms characteristic impedance will be

$$P_{av} = \frac{10^2}{1000} (1 + 3) \frac{200}{40,000} = 2 \cdot \text{mW} \quad \text{---} \quad (10.3.2)$$

This is considered a satisfactorily low value for the pilot lines to be used, and a nominal value of transmitted pulse amplitude of 10 volts has therefore been used.

10.4 Possible use of bidirectional pulse

As discussed in Sec. 7.1, it is necessary to provide a time delay in each substation to allow the pilot line and transformer to discharge before the tertiary pulses are generated. A reduction in this time delay might be possible by the use of a transmitted pulse voltage waveform consisting of the 10 volt 200 μsec. positive pulse, followed immediately by a similar negative pulse. This would reduce the time required by the transformer overswing voltage, (see Sec. 11). It was decided not to use this type of waveform, however, as the possible reduction in the number of binary elements in the time delay generator was outweighed by the increased complexity of the transmitted pulse generator. A further disadvantage is that should a fault occur, resulting in the non-transmission of the negative pulse, the resulting extended transformer overswing voltage could cause and error in the phase angle indication which might well remain undetected.

10.5 Relative merits of pulse and sinusoidal waveforms

It is useful to compare the merits of pulse and sinusoidal waveforms for conveying the measurement information between substation and Control Centre. In an early scheme considered, it was proposed to apply the 50 Hz sinusoidal test voltage, after a suitable phase advance, to the pilot line at the substation, and to detect the zero crossover of the voltage received at the Control Centre. Let us compare this system with the present one. For an equal amount of power delivered to the line considered in Sec. 10.3, the voltage applied to the line would be

$$V_s = \sqrt{P_{av} Z_o} = \sqrt{2 \times 1000/1000} = 1.41V \text{ r.m.s.} \quad \text{-------} \quad (10.5.1)$$

This low value of voltage, compared with the 10V pulse amplitude, is even less favourable than the ratio of amplitudes would suggest. While both systems are prone to errors caused by pulse interference signals induced in the pilot line, the sinusoidal voltage system is much more susceptible to errors caused by interference voltages having a sinusoidal waveform. With a sinusoidal interference voltage V_q induced in a line carrying a test signal voltage V_s, the error in the zero crossover point will be greatest when the two voltages are in quadrature. Then, assuming $V_q << V_s$, the error $\delta\phi$ in the phase angle will be

$$\delta\phi = \frac{V_q}{V_s} \text{ radians} \quad \text{--------} \quad (10.5.2)$$

Thus, for a test signal voltage of 1.41V r.m.s., a 1^o error will be caused by an interference signal of magnitude

$$V_q = V_s/57.3 = 24.6 \text{ mV r.m.s.} \quad \text{---} \quad (10.5.3)$$

If an interference voltage of this magnitude were present in the voltage applied to the comparator of the pulse system, the resulting error, from equation (13.1.3), would be approximately $(24.6 \times \sqrt{2})/425 = 0.0818$ degrees of phase angle. Furthermore, the

action of the high-pass filter formed by the line transformer inductance L, in conjunction with the series resistance R_1, (Fig. 21), is still more to discriminate in favour of the pulse voltage.

The pulse system is thus superior, by a factor exceeding 10, in its resistance to errors caused by sinusoidal interference voltages induced in the pilot line.

11.1 PILOT LINE TRANSFORMER COUPLING

It has already been mentioned in Sec. 3.1 that voltage-isolating transformers are necessary at each end of the pilot line, as a precaution against an excessive voltage being transmitted along the line, should a fault condition in a substation result in an elevated "earth" potential there. The specification calls for insulation to withstand 2 kV r.m.s., and the present transformers have been designed to this : it is believed, however, that in future installations this requirement may be raised to 5 kV r.m.s., in which case a redesign of the transformers will be necessary.

An important benefit given by the transformers is to minimize the transmission to the voltage comparators of common-mode electrical noise voltages induced in the line. This type of signal, applied to the primary of a transformer, can cause a voltage in the secondary in two ways : the first is caused by capacitance between the primary and secondary windings : signals transmitted by this means can be reduced to a satisfactorily low level by thorough screening between the two windings. The common-mode primary signals can also cause a secondary voltage by the action of the capacitance of the primary winding to earth: this capacitance is distributed along the winding, and as it becomes charged by the common-mode voltage, the charging current from the line causes an m.m.f. to be developed in the winding. If, however, this winding is of symmetrical construction, the effect of the current flowing to earth from one line is balanced by that from the other, and the nett m.m.f., and hence the secondary voltage induced, is very small.

A further requirement of the transformers is that they shall be free from non-linearity between input and output voltages. The pulse voltages applied are such that the resulting magnetization of the transformer is unidirectional, and an air gap in the magnetic core is essential if saturation effects are to be avoided.

The above requirements for a balanced and screened pulse transformer, with linear characteristics, and made to specified tolerances on primary inductance, leakage inductance and self-capacitance, make this a component upon which the proper operation of the system critically depends. The design of the transformer is complicated by the wide variety of pilot lines in conjunction with which it may have to work. As mentioned in Sec. 1.1, the characteristics of these lines are unknown; this excludes the use of any line/transformer matching or equalization networks which rely on a knowledge of the properties of the line for their correct operation.

11.2 Line/transformer coupling network

With the transformer directly connected to the pilot line, there is an interchange of energy between line and transformer following the transmission of a pulse. This causes line voltage oscillations, which may persist for some considerable time after the cessation of the pulse. If an error in timing is to be avoided, the line should be fully discharged before a pulse is transmitted; it is therefore important that these oscillations are minimized, and this has been accomplished by the line coupling network shown in Fig. 15. A low resistance path for the rapid discharge of the line is provided by R_2, while the higher resistance of R_1 ensures a rapid decay of the magnetic flux in the transformer T.

To assist in the design of the transformer and this line coupling network, a pilot line having a length greater than that required by the specification for the system was made available to the University. This will be referred to as "line X". The effect of R_2 on the discharge time of this line was investigated in a series of tests using the circuit shown in Fig. 16. A positive voltage pulse was applied to A and, simultaneously, a negative pulse was applied to B: the saturation of the transistors TR1 and TR2 caused the line to be charged to a potential difference of approximately 24 volts, symmetrical with respect to earth. On

termination of the pulses, the line discharged through the resistors, and the waveform of the voltage v was measured on an oscilloscope having a "differential input" facility. Typical waveforms are shown in Fig. 17; the positive-going waveforms show the charging of the line, when TR1 and TR2 are conducting, and the negative-going waveforms show the discharge of the line through the resistors. The tests were repeated, using a series of values of R_2, and the time for v to fall to one-half of its initial amplitude during discharge of the line was measured: the results are shown in Fig. 18, and indicate the great effect of R_2 on the discharge time of the line. This would suggest that the value of R_2 should be the minimum permissible consistent with a satisfactorily low attenuation of the signal voltage. The d.c. loop resistance of line X was 728 ohms: taking a value of 1000 ohms as being the maximum resistance of a line likely to be used, then if R_2 = 220 ohms, a 10-volt transmitted pulse will give a received pulse amplitude of 1.8 volts. This was considered an adequate received signal level compared with the electrical noise it was expected might be induced in the line. The value of R_2 was thus tentatively fixed at 220 ohms.

11.3 Effects of transformer inductance

The inductance L of the transformer T in Fig. 15 has two deleterious effects. One effect is to cause oscillations, as mentioned in the previous Section. The other effect is a distortion of the received pulse : when a signal voltage is received from the pilot line, the "differentiating" effect of L and R_1 is to cause the voltage pulse developed across the windings of T to differ from the pulse voltage across R_2.

Considering the latter effect, suppose the received voltage across R_2 is

$$V_r = V(1 - e^{-\frac{t}{T_r}}) \qquad \text{-------} \qquad (11.3.1)$$

where T_r is the time constant of the assumed exponential rise of v_r. Then the Laplace transform of the voltage v_L across

the inductance L is

$$\overline{v_L} = \frac{Ls}{(R_1 + Ls)} \cdot \overline{v_r} \qquad \text{-------} \qquad (11.3.2)$$

$$= \frac{s}{(s + \frac{R_1}{L})} \left[\frac{1}{s} - \frac{1}{(s + \frac{1}{T_r})} \right] V$$

$$= \left[\frac{1}{(s + \frac{R_1}{L})} + \frac{\frac{1}{T_r}}{(\frac{R_1}{L} - \frac{1}{T_r})} \cdot \frac{1}{(s + \frac{1}{T_r})} - \frac{\frac{R_1}{L}}{(\frac{R_1}{L} - \frac{1}{T_r})} \cdot \frac{1}{(s + \frac{R_1}{L})} \right] V$$

$$\text{-------} \qquad (11.3.3)$$

The voltage v_L is therefore

$$v_L = \frac{\frac{L}{R_1}}{(\frac{L}{R_1} - T_r)} \left[\varepsilon^{-\frac{R_1 t}{L}} - \varepsilon^{-\frac{t}{T_r}} \right] V \qquad \text{-------} \qquad (11.3.4)$$

A graph of this is plotted in Fig. 19, for various values of $\frac{L}{R_1 T_r}$, and shows the increasing distortion of the waveform of v_L as the ratio $\frac{L}{R_1 T_r}$ is reduced.

As described in Sec. 6.1, the timing of the received voltage is measured from the instant that v_L reaches a predetermined value V_{ref}, to which the voltage comparator is set. It is clear from Fig. 19 that this will be delayed on the instant that v_r attains a similar value, and this delay will depend upon the ratio of the time constants L/R_1 and T_r. Any variation in the values of L or R_1 can

therefore cause a timing error in the system. The variation in delay caused by a given variation in L/R_1 may be calculated as follows : if we put $\alpha = 1/T_r$, and $\beta = R_1/L$, then equation (11.3.4) may be rewritten

$$v_L = \frac{\alpha}{\alpha - \beta} \left[\varepsilon^{-\beta t} - \varepsilon^{-\alpha t} \right] V \quad \text{-------} \quad (11.3.5)$$

Now, if α and β are constant,

$$\frac{\partial v_L}{\partial t} = \frac{\alpha}{(\alpha - \beta)} \left[\alpha \varepsilon^{-\alpha t} - \beta \varepsilon^{-\beta t} \right] V \quad \text{--} \quad (11.3.6)$$

And, if α and t are constant,

$$\frac{\partial v_L}{\partial \beta} = \frac{V \alpha}{(\alpha - \beta)^2} \left| \varepsilon^{-\beta t} - \varepsilon^{-\alpha t} \right| - \frac{V \alpha t}{(\alpha - \beta)} \varepsilon^{-\beta t} \quad \text{-- (11.3.7)}$$

If both t and β vary by dt and $d\beta$ respectively, the total variation dv_L in v_L will be

$$dv_L = \frac{\partial v_L}{\partial t} \cdot dt + \frac{\partial v_L}{\partial \beta} \cdot d\beta \quad \text{------} \quad (11.3.8)$$

Therefore, the variation dt which will be caused by a variation $d\beta$, for a constant comparator voltage V_{ref} will be given by equating (11.3.8) to zero, i.e.,

$$\frac{\partial v_L}{\partial t} \cdot dt + \frac{\partial v_L}{\partial \beta} \cdot d\beta = 0 \quad \text{------} \quad (11.3.9)$$

giving

$$\frac{dt}{d\beta} = - \frac{\partial v_L}{\partial \beta} \cdot \frac{\partial t}{\partial v_L} \quad \text{------} \quad (11.3.10)$$

substituting from (11.3.6) and (11.3.7),

$$\frac{dt}{d\beta} = \frac{\frac{1}{(\alpha-\beta)}\left[\varepsilon^{-\beta t} - \varepsilon^{-\alpha t}\right] - t\,\varepsilon^{-\beta t}}{\alpha\varepsilon^{-\alpha t} - \beta\varepsilon^{-\beta t}} \qquad \text{--------} \qquad (11.3.11)$$

The variation Δt in delay caused by a variation $\Delta\beta$ will thus be

$$\Delta t = \frac{dt}{d\beta} \cdot \Delta\beta \qquad \text{--------} \qquad (11.3.12)$$

The value of β may now be calculated which, for a given tolerance on β, will ensure that the timing error is within the allowable limits. The largest variation in β is likely to be caused by variations in inductance L of the transformer. By the use of a magnetic core having an air gap which is adjustable after the coils are wound, a tolerance of $\pm$ 5% on L is readily achievable,[25] but if the tolerance is reduced much below this value, the manufacture of the transformer becomes increasingly difficult and expensive, the leakage inductance becomes excessive, and the susceptibility of the magnetic material to variations in temperature and mechanical stress become important. Tolerances of $\pm$ 5% on L, and $\pm$ 3% on R_1 have therefore been accepted, giving a total tolerance on β of $\pm$ 8%. To calculate the required value of β, the signal voltage time constant must be known. For line X, Fig. 18 shows that when R_2 = 220 ohms, the voltage across R_2 falls to half amplitude in approximately 100 μsec: if this fall is assumed to be exponential the time constant will be 100/log. 2 = 144 μsec. Using this value for T_r, Fig. 20 shows the timing error Δt plotted against β, using equation (11.3.12), and assuming that $V_{ref} = \frac{V}{2}$. For a value of $\Delta t = \pm$ 1.4 μsec., corresponding to a total error of 2.8 μsec. or 1/20 degree at 50 Hz, the value

of β required is approximately 1870, i.e.,

$$L/R_1 = 534\ \mu\text{sec.} \qquad \text{-------} \qquad (11.3.13)$$

This value was used as a basis for the specification of the transformer. It represents the minimum value of L/R_1 which, using the longest line likely to be used, and with the voltage comparator level V_{ref} set to operate when the received pulse attains one-half of its final amplitude, will give a timing error of $\pm$ 1/40 degree for a $\pm$ 8% variation in L/R_1. For most of the lines likely to be used with this equipment, the received voltage will be so large that V_{ref} will be only a small fraction of V, and the timing error will be correspondingly reduced.

11.4 Transformer inductance calculation

Having arrived at a suitable value of L/R_1 to avoid excessive distortion of the received signal, the effect of L and R_1 on the conditions for oscillation following a transmitted pulse may be examined. There are many possible criteria for optimizing the performance of the line/network/transformer combination, and a great number of equivalent circuits, of varying degrees of complexity, may be drawn to represent the system. The equivalent circuit finally adopted was the simplest, and is shown in Fig. 21; the pilot line is represented by the capacitance 2C. Taking a value of 2C equal to the maximum distributed capacitance of any line likely to be used with the equipment, the value of R_1 required to just prevent oscillations in v_c can then be calculated. It is assumed that with a value of R_1 so obtained, the use of a line of capacitance lower than 2C will give a satisfactorily short discharge time.

Taking a mid-shunt division of the line, as shown in Fig. 22, the mesh equations are :

$$-L\frac{di_1}{dt} - (R_1 + R_2)\, i_1 + R_2 i_2 = 0 \quad \text{---} \quad (11.4.1)$$

$$R_2 i_1 - R_2 i_2 - \frac{1}{C}\int i_2\, dt = 0 \quad \text{---} \quad (11.4.2)$$

from (11.4.2)

$$i_1 = i_2 + \frac{1}{R_2 C}\int i_2\, dt \quad \text{---} \quad (11.4.3)$$

hence

$$\frac{di_1}{dt} = \frac{di_2}{dt} + \frac{i_2}{R_2 C} \quad \text{---} \quad (11.4.4)$$

Substituting (11.4.3) and (11.4.4) in (11.4.1)

$$L\frac{di_2}{dt} + \left(\frac{L}{R_2 C} + R_1\right) i_2 + \frac{(R_1 + R_2)}{R_2 C}\int i_2\, dt = 0 \quad \text{---} \quad (11.4.5)$$

hence

$$L\frac{d^2 i_2}{dt^2} + \left(\frac{L}{R_2 C} + R_1\right)\frac{di_2}{dt} + \frac{(R_1 + R_2)}{R_2 C} i_2 = 0 \quad \text{---} \quad (11.4.6)$$

A non-oscillatory solution to this equation is obtained when

$$\left(\frac{L}{R_2 C} + R_1\right)^2 \geqslant \frac{4L(R_1 + R_2)}{R_2 C} \quad \text{---} \quad (11.4.7)$$

which, for a given L, C and R_2, requires a value of R_1 given by

$$R_1^2 - \frac{2L}{R_2 C} \cdot R_1 + \left(\frac{L^2}{R_2^2 C^2} - \frac{4L}{C}\right) \geqslant 0 \quad \text{--} \quad (11.4.8)$$

But the value of $R_1/L = \beta$ has already been determined in equation (11.3.13). Putting $L = R_1/\beta$, equation (11.4.8) becomes

$$R_1 \left[R_1 \left(1 - \frac{2}{\beta R_2 C} + \frac{1}{\beta^2 R_2^2 C^2} \right) - \frac{4}{\beta C} \right] \geqslant 0 \qquad \text{---- (11.4.9)}$$

Rejecting the trivial solution $R_1 = 0$ (corresponding to $L = 0$), the smallest value of R_1 for a non-oscillatory solution is then

$$R_{1(\min)} \left(1 - \frac{2}{\beta R_2 C} + \frac{1}{\beta^2 R_2^2 C^2} \right) = \frac{4}{\beta C} \qquad \text{---- (11.4.10)}$$

giving

$$R_{1(\min)} = \frac{4\beta R_2^2 C}{(1 - \beta R_2 C)^2} \qquad \text{---- (11.4.11)}$$

A value of $R_1 = 940$ ohms was chosen, which satisfies (11.3.13) and the above equation for a value of C of 0.96 μF. It is not expected that this value of capacitance will be exceeded in any line to be used with the equipment. The required transformer inductance is thus

$$L = R_1/\beta = 940/1870 = 0.5 \text{ H} \qquad \text{---- (11.4.12)}$$

Using these values of R_1 and L, the results of experiments on typical pilot lines of various lengths and characteristics are given in Section 14. They show that the required short discharge time for the line and transformer have been achieved, justifying the use of the eqivalent circuit of Fig. 21 as a basis for the design of the transformer and coupling network.

It is a matter for some satisfaction that such a simple equivalent circuit can describe the operation with enough accuracy to allow so straightforward a design procedure. The success of

the representation of the line by the capacitor 2C may be understood by noting that the effect of the pilot line inductance is swamped by the presence of the inductance L, while the effect of line resistance can only increase the damping of the network, and thus reduce still further the possibility of line voltage oscillations.

11.5 Active coupling network

Consider now the network of Fig. 15 when a pulse is being transmitted. The pulse from the transformer is delivered to the pilot line through the resistance R_1. The high value of this resistance compared with the combined impedance of R_2 and Z_o in parallel causes a large attenuation in the network, and to develop the 10-volt pulse as specified in Sec. 10.3, an inconveniently large amplitude of pulse voltage would be required from the transformer. The fact that the transmitted pulse is unidirectional suggests that this attenuation could be avoided by the use of a polarity - sensitive switch to shunt R_1 in the transmit condition, this switch opening with the reverse - polarity overswing of the transformer voltage. The attenuation of the network to transmitted signals would then be low, but the discharge of the line and transformer unaffected. This action can be achieved by shunting each resistor $R_1/2$ with a diode, connected so that the diodes conduct when a pulse is transmitted; unfortunately, diodes connected in this way largely nullify the advantages of the balanced transformer, as whatever the polarity of common-mode noise voltages induced on the line, one diode will be reverse-biassed while the other is biassed in the conducting direction causing an m.m.f. in the transformer winding as described in Sec. 11.1.

The balance of the line/transformer system can be preserved by the use of the active network shown in Fig. 23,[26] which also shows the transistor TR used to generate the pulse. When a pulse is transmitted, terminal A of the transformer T has a potential positive to that of terminal B. The transistors TR1 and TR2 are then saturated by base current flowing through the resistors R_3 and the diodes D1 and D2. When the transmitted pulse terminates, the transformer voltage overswing causes A to become negative to B, and the transistors cease conduction. The diodes ensure that excessive reverse voltage cannot be applied between base and emitter of the transistors: they have a further function; when a pulse is being received, conduction in the transistors is prevented until the

received voltage has an amplitude greater than the value of the reference voltage V_{ref}. The attenuation of the network to received signals up to the time of the voltage comparator output pulse is thus known and constant, and the calculations of Sec. 11.3 may be used. The network, being on the line side of the transformer, has to be insulated to withstand a potential to earth of 2 kV r.m.s.; this is facilitated by the fact that no d.c. supplies to the transistors are necessary.

11.6 Effect of transformer leakage inductance

The calculations given in Sec. 11.3 assumed that the received voltage v_r developed across R_2 was exponential, with a time constant T_r. Continuing that assumption, the value of T_r will depend upon the waveform of the voltage delivered to the pilot line from the transmitter, and also upon the bandwidth of the line. Assuming further that the frequency response of the line corresponds to that of a single RC circuit of time constant T_L, then if the voltage v_t delivered to the line is exponential, with a time constant T_t, the voltage v_r will have a time constant

$$T_r = \sqrt{T_t^2 + T_L^2} \qquad \text{-------} \qquad (11.6.1)$$

Thus, any variation in T_t will cause a variation in T_r, and a corresponding change in the timing of the received voltage, as described in Sec. 11.3. It is therefore necessary that the tolerance on the value of the components affecting T_t should be controlled, in order that possible timing errors from this cause are within acceptable limits.

The circuit diagram of the transmitter is shown in Fig. 23, and the equivalent circuit which applies during the period of the transmitted pulse is given in Fig. 24. The inductance L_1 represents the leakage inductance of the transformer, measured between transmitter and line windings. In series with this inductance should be the resistance of the transformer windings, and also the saturation resistance of the transistors TR, TR1 and TR2 in Fig. 23 : these

resistances have been omitted, as they are small in comparison with the combined resistance R_{eq} of R_2 and Z_o in parallel. Using this equivalent circuit, the time constant of the pulse of voltage v_t transmitted to the line is

$$T_t = L_1/R_{eq} \qquad \text{------} \qquad (11.6.2)$$

Now suppose that T_t changes by a small increment ΔT_t; the corresponding change ΔT_r in T_r will be

$$\Delta T_r = \frac{dT_r}{dT_t} \Delta T_t \qquad \text{------} \qquad (11.6.3)$$

Differentiating equation (11.6.1) and substituting in (11.6.3) gives

$$\Delta T_r = \frac{T_t}{\sqrt{T_t^2 + T_L^2}} \Delta T_t \qquad \text{------} \qquad (11.6.4)$$

For a given increment ΔT_t, the change ΔT_r will thus be greatest when $T_L << T_t$, and in this case

$$T_r = T_t \qquad \text{------} \qquad (11.6.5)$$

The effect of a variation in T_t on the timing can now be calculated. From Sec. 11.3,

$$v_L = \frac{\alpha}{(\alpha - \beta)} \begin{bmatrix} -\beta t & -\alpha t \\ \varepsilon & -\varepsilon \end{bmatrix} V \qquad \text{------} \qquad (11.3.5)$$

Now, if α and β are constant,

$$\frac{\partial v_L}{\partial t} = \frac{\alpha}{(\alpha - \beta)} \begin{bmatrix} -\alpha t & -\beta t \\ \alpha\varepsilon & -\beta\varepsilon \end{bmatrix} V \qquad \text{------} \qquad (11.3.6)$$

and if β and t are constant,

$$\frac{\partial V_L}{\partial \alpha} = \frac{V\beta}{(\alpha-\beta)^2}\left[\varepsilon^{-\alpha t} - \varepsilon^{-\beta t}\right] + \frac{V\alpha t}{(\alpha-\beta)}\varepsilon^{-\alpha t} \qquad \text{--- (11.6.6)}$$

For a constant value of v_L, the change dt corresponding to a change $d\alpha$ will therefore be given by

$$\frac{\partial V_L}{\partial t} \cdot dt + \frac{\partial V_L}{\partial \alpha} \cdot d\alpha = 0 \qquad \text{------ (11.6.7)}$$

hence,

$$\frac{dt}{d\alpha} = -\frac{\partial t}{\partial V_L} \cdot \frac{\partial V_L}{\partial \alpha} \qquad \text{----- (11.6.8)}$$

Substituting from (11.3.6) and (11.6.6),

$$\frac{dt}{d\alpha} = \frac{\frac{\beta}{\alpha(\alpha-\beta)}\left[\varepsilon^{-\beta t} - \varepsilon^{-\alpha t}\right] - t\varepsilon^{-\alpha t}}{\alpha\varepsilon^{-\alpha t} - \beta\varepsilon^{-\beta t}} \qquad \text{------ (11.6.9)}$$

For a small change $\Delta\alpha$ in α, the change Δt in the timing of the voltage comparator output will then be

$$\Delta t = \frac{dt}{d\alpha} \cdot \Delta\alpha \qquad \text{------ (11.6.10)}$$

The greatest variation in α is likely to be caused by variations in L_1 between one transformer and another. While, as described in Sec. 11.3, it is readily possible to adjust the primary inductance of a transformer by variation of an air gap in the magnetic core, it is much more difficult to adjust the leakage inductance also.

It is therefore important that all transformers required to work in a set of phase angle measurement equipments are made by the same manufacturer, and preferably wound in the same batch. The transformers used for the development work were made some years before those used in the production version of the equipment; the measured values of the leakage inductance of the transformers were all within the range 4±1 mH, and are given in Sec. 12.3

The timing error caused by a variation of 1 mH in leakage inductance is calculated below. The following values are used:

$$L_1 = 4 \text{ mH.} \quad \Delta L_1 = 1 \text{ mH.}$$

From Sec. 11.3: $\beta = 1870$; $V_{ref} = V/2$; $\therefore \alpha t = 0.693$.

$$R_{eq} = R_2 Z_o/(R_2 + Z_o) = 100 \text{ ohms.}$$

$$\alpha = R_{eq}/L_1 = 25,000.$$

$$\frac{\Delta\alpha}{\alpha} = \frac{\Delta L_1}{L_1} = \frac{1}{4}, \quad \therefore \Delta\alpha = 6250.$$

Substituting these values in equation (11.6.10),

$$\Delta t = \left[\frac{\frac{1870}{25,000(25,000-1870)} \left[\varepsilon^{-0.0518} - \varepsilon^{-0.693} \right] - \frac{0.693}{25,000} \varepsilon^{-0.693}}{25,000\,\varepsilon^{-0.693} - 1870\,\varepsilon^{-0.0518}} \right] 6250$$

$$\Delta t = -7.23 \ \mu\text{sec.} \qquad \text{------} \qquad (11.6.11)$$

This is equivalent to a phase angle error of approximately 1/8 degree at 50 Hz. On all but the longest lines, the error will be less than this value, as the assumption that $V_{ref} = \frac{V}{2}$, made in deriving (11.6.11), implies a line having the maximum allowable attenuation. The results of experiments to measure the variation in error for a change in leakage inductance, using various pilot lines, are given in Sec. 14.4: they show that for most of the lines likely to be used, the error is substantially below that given by (11.6.11). The calculations leading to (11.6.11) do, however, allow

the leakage inductance for the transformer to be specified as 4 ± 1 mH, with the confidence that the timing error due to variations within this range will then be acceptably small. They also indicate that some improvement in overall accuracy might be made by seeking a reduction in ΔL_1, probably by reducing L_1, even if this resulted in the necessity for widening the tolerance on the primary inductance L.[27]

11.7 Effect of transformer self-capacitance

The distributed capacitance of the transformer windings can be represented approximately by a capacitance connected across L in Fig. 15. The main effect of this capacitance will be to modify slightly the waveform of the voltage across the transformer windings when a voltage pulse is received from the pilot line. To expect the transformer manufacturer to be able to control the distributed capacitance to a close tolerance, in addition to L and L_1, is clearly unrealistic: tests were therefore made to determine the value of capacitance which, when connected across L, would cause a specified error in the timing of the received voltage. These tests were carried out using a succession of pilot lines of different characteristics, and are described in Sec. 14.6; they indicate that a substantial value of capacitance must be added to cause an appreciable error. It would appear, therefore, that particular attention to a close tolerance on distributed capacitance in the transformer is unnecessary, and external capacitance connected across L to bring the total capacitance to a standard value is not required.

12.1 TRANSFORMER TEST RESULTS

The line transformers were manufactured in three batches. Initially, two transformers were made, having values of L differing by the 5% tolerance specified : after the effects of this tolerance predicted by calculation had been experimentally confirmed, (see Sec. 14.3), a further seven transformers were made. These latter were used in the Field Trials equipments, and have serial numbers 3 - 9. Some two years later, a further batch of transformers were made for permanent installation in the M.S.E.V. equipments; these have serial numbers 10 - 22.

The transformer windings are as shown in Fig. 25. The winding joining terminals 5 and 6 is connected, via the network described in Sec. 11.2, to the pilot line : this winding is completely surrounded by a screen connected to pin 11. The transmitter is connected to terminals 1 and 4: the tapping points, intended for a possible increase in transmitted voltage, are not used. The windings terminating at 7 and 10 supply the voltage comparator : an external link is required between terminals 8 and 9. All of the windings shown in Fig. 15 have an equal number of turns.

12.2 Primary inductance tests

The inductance measured between terminals 1 and 4, with no connection to the other terminals, is given in Table 1. The measurements were made using a Marconi Bridge type TF 1313A, at a frequency of 1 kHz.

TABLE 1

Ser. No.	L	Ser. No.	L	Ser. No.	L
3	0.505 H.	10	0.517 H.	17	0.516 H.
4	0.496	11	0.516	18	0.512
5	0.494	12	0.513	19	0.522
6	0.503	13	0.517	20	0.498
7	0.476	14	0.540	21	0.528
8	0.496	15	0.503	22	0.527
9	0.499	16	0.490		

Considerable care is normally required to interpret the results of a measurement of primary inductance of a transformer, unless the measurement conditions are closely similar to those under which the transformer is to operate. With these transformers, however, the air gap is sufficiently large that the variation of permeability of the iron with varying magnetic excitation has only a small effect on the primary inductance, and the requirement of linearity mentioned in Sec. 11.1 appears to have been met.

Although the tolerance on the value of inductance of the transformers measured was somewhat greater than that specified in Sec. 11.3, the test results were considered to be acceptable.

12.3 Leakage inductance tests

The inductance measured between terminals 1 and 4, with 5 and 6 short-circuited, but with no connection to the other terminals, was measured as in Sec. 12.2. Table 2 gives the results.

TABLE 2

Ser. No.	L_1	Ser. No.	L_1	Ser. No.	L_1
3	3.44 mH	10	4.02 mH	17	3.25 mH
4	3.14	11	3.55	18	3.89
5	3.29	12	4.00	19	4.16
6	3.50	13	3.70	20	3.74
7	3.09	14	3.96	21	4.85
8	3.18	15	3.84	22	4.85
9	3.08	16	3.84		

The effect of these variations in L_1 has already been discussed in Sec. 11.6. Since the path of the leakage flux in the transformer is largely in air, the leakage inductance is virtually unaffected by the magnetic excitation level, and there is less need for caution in interpretation of the results of the measurements, than was the case in the tests described in Sec. 12.2.

12.4 Common-mode rejection tests

To simulate common-mode noise voltages induced in the pilot line, the arrangement shown in Fig. 26 was used. Pulses of variable frequency and duration were generated in the pulse generator PG; the rise time of the pulses being less than 10^{-7} sec. The resistance of the line was simulated by the 220 ohm resistors, and these were connected to the networks N, which are as shown in Fig. 23. The voltage across the comparator winding (Sec. 12.1) of each transformer was measured: with a pulse from PG of amplitude 50 volts, the voltage "spikes" induced in the comparator winding did not exceed 0.2 volts amplitude. It is considered that a very satisfactory degree of screening and balance within the line transformer has been achieved.

13.1 OPTIMUM COMPARATOR REFERENCE VOLTAGE

To determine an optimum value for the reference voltage V_{ref} to which the voltage comparator should be set is difficult, unless the properties of the pilot lines, and their electrical noise level, are known. An unsuitable choice of V_{ref} can affect the accuracy of timing in the system in several ways. As mentioned in Sec. 11.3, the timing error caused by a given variation in L/R_1 will become greater as V_{ref} is increased: the timing error caused by variations in transformer leakage inductance (Sec. 11.6) will be similarly affected by the value of V_{ref}.

A further cause of timing error will be the variation ΔV_{ref} in the reference voltage that will occur with variations in the values of the comparator circuit elements with age, temperature and supply voltage variations; this will cause an error of magnitude dependent upon the rate of rise of the voltage received by the comparator. The received voltage developed across the transformer winding has already been calculated:

$$v_L = \frac{\frac{L}{R_1}}{\left(\frac{L}{R_1} - T_r\right)} \left[\varepsilon^{\frac{-R_1 t}{L}} - \varepsilon^{\frac{-t}{T_r}} \right] V \quad \text{-----(11.3.4)}$$

The rate of rise of this voltage is thus

$$\frac{dv_L}{dt} = \frac{1}{\left[\frac{L}{R_1} - T_r\right]} \left[\frac{L}{R_1 T_r} \varepsilon^{\frac{-t}{T_r}} - \varepsilon^{\frac{-R_1 t}{L}} \right] V \quad \text{--- (13.1.1)}$$

Taking values of T_r = 144 μsec; L/R_1 = 534 μsec. (from Sec. 11.3) the ratio $L/R_1 T_r$ = 534/144 = 3.7. From Fig. 19, the peak value of v_L will then be approximately 0.6V. Using the value V = 1.8 volts mentioned in Sec. 11.2, the amplitude of v_L will be 0.6 x 1.8 = 1.08 volts.

Now assume that V_{ref} is set to one-half of the amplitude of v_L. From Fig. 19, v_L will reach this value at a time given approximately by $t/T_r = 0.37$, i.e., $t = 0.37 \times 144 = 53$ μsec. Substituting the above values for T_r, L/R_1 and t in equation (13.1.1) gives

$$\frac{dv_L}{dt} = \frac{10^6}{(534-144)} \left[\frac{534}{144} \varepsilon^{-\frac{53}{144}} - \varepsilon^{\frac{-53}{534}} \right] 1.8$$

$$= 7660 \text{ volts/sec.} \qquad \text{-----(13.1.2)}$$

For a timing error Δt not exceeding 1/10 degree at 50 Hz, i.e. 5.55 μsec., the permissible error ΔV_{ref} will thus be

$$\Delta V_{ref} = \frac{dv_L}{dt} \Delta t$$

$$= 7660 \times 5.55/10^6 = 42.5 \text{ mV} \text{ --- (13.1.3)}$$

By the series connection of the two comparator windings of the transformer (Fig. 25), the amplitude of the received voltage is doubled : the reference voltage has been set to the value V_{ref} = 1volt, and the permissible error ΔV_{ref} for a 1/10 degree timing error is then approximately 85 mV. It is confidently expected that the voltage comparator error will remain well within this tolerance over a period of many years : the results of life tests over a period of approximately two years on the M.S.E.V. substation comparators are given in Sec. 22.2: they show a variation in V_{ref} of a few millivolts only.

The timing errors can all be reduced by the choice of a low value of the reference voltage : this choice will also allow the use of lines of high attenuation, and will therefore extend the maximum usable range of the equipment. However, as V_{ref} is reduced, the probability of false triggering by electrical noise

induced in the lines is increased. The best compromise then depends upon a knowledge of the noise level expected, and this is not usually known. The lines tested in Sections 14 and 25 include some longer than those with which the equipment will be used: with none of the lines was there observed a received noise level high enough to interfere in any way with the proper operation of the system.

14.1 TESTS ON PILOT LINE/TRANSFORMER COMBINATION

The tests described in this Section were made to confirm experimentally the assumptions made in previous Sections, and to measure the effect of transformer manufacturing tolerances, under conditions simulating those which exist when phase angle measurement is proceeding. The test circuit is shown in Fig. 27; the transformers T_1 and T_2 and their associated circuits were part of complete substation and Control Centre equipments, respectively. Many of the tests used the pilot line "X" mentioned in Sec. 11.2. This had a loop resistance of 728 ohms, and consisted of a short length (<1 mile) of 3 core 12 pair 0.044" cable, in which one pair was used, and a similar length of 3 core 4 pair 0.044" cable, in which also one pair was used. The remainder of the circuit consisted of one pair in a Pirelli 15 pair telephone cable, "40 lbs/1000 yds Dry Cored Air Spaced Paper Insulated Lead Covered Steel Taped Armoured", of length 23,160 yards, and laid in 1928. Both ends of this composite cable were brought in to the University laboratory. The waveforms were recorded using a Tektronix type 547 oscilloscope, and where a great accuracy of time measurement was required this was obtained by the use of a quartz-crystal controlled time-mark generator, using the oscilloscope to interpolate between the 1 μsecond timing pulses. It is expected that the error of time measurement using this system is less than 0.2 μsec.

14.2 Optimum coupling network - tests

Tests were made to confirm the suitability of resistances R_1 and R_2 calculated for the coupling network in Sec. 11. The tests were carried out using the arrangement of Fig. 27, which shows the pilot line, transformers and coupling networks for one substation equipment and for the corresponding input to the Control Centre equipment. The transmitter was as shown in Fig. 23.

The first test was to investigate the effect of varying R_2, with $R_1/2$ set to a constant value of 470 ohms. This test complements the measurements made in Sec. 11.2 on the discharge of the pilot line without transformers. The test was in two parts : referring to Fig. 27, the first part was to measure the amplitude $\hat{v}_{EF}$ of the transmitted pulse and the time t_{EF} for it to reach one-half of its amplitude, for a succession of values of R_2. The results are shown in Fig. 28, and a typical waveform of v_{EF}, for R_2 = 200 ohms, is given in Fig. 30. As R_2 is reduced, the amplitude of the transmitted pulse falls, due to the effective resistance of the pulse source constituted by the resistance of the transformer windings, and the saturation resistance of the transistors TR1 and TR2 in Fig. 27, and TR in Fig. 23. Let this effective resistance be r. Then if Z_o is the characteristic impedance of the line, assumed resistive, then

$$v_{EF} = \frac{R_2 Z_o/(R_2 + Z_o)}{r + R_2 Z_o/(R_2 + Z_o)} E_p \qquad \text{-----} (14.2.1)$$

where E_p is the amplitude of the pulse of e.m.f. across terminals E and F with R_2 and the pilot line disconnected: the measured value of E_p was 11.8 volts. From (14.2.1),

$$\frac{1}{\hat{v}_{EF}} = \left[1 + \frac{r}{Z_o} + \frac{r}{R_2} \right] \frac{1}{E_p} \qquad \text{-----} (14.2.2)$$

By plotting $1/\hat{v}_{EF}$ against $1/R_2$ as in Fig. 28, the effective pulse source resistance may be obtained, viz :

$$\text{Slope of graph} = r/E_p = 2.2 \text{ ohm.volt}^{-1}.$$

$$\therefore \quad r = 2.2 \times 11.8 = 26 \text{ ohms} \qquad \text{-----} (14.2.3)$$

This low value of r indicates that the transmitted pulse amplitude is unlikely to be greatly affected by connection of the different types of pilot lines likely to be used with the equipment.

The other effect on the transmitted pulse voltage of a reduction in R_2 is an increase in the time t_{EF} for the voltage v_{EF} to reach half-amplitude, as shown in Fig. 28. This is caused mainly by the leakage inductance of the transformer, as predicted in equation (11.6.2).

The second part of the first test was the measurement of the amplitude $\hat{v}_{GH}$ of the received voltage, and the time t_{GH} for it to rise from zero to half-amplitude, as R_2 was varied. The results are given in Fig. 29, and a typical waveform of v_{GH}, for R_2 = 200 ohm, is shown in Fig. 31. The attenuation of the line, $\hat{v}_{EF}/\hat{v}_{GH}$ is also plotted. The accuracy of measurement of t_{GH} was below that of the other quantities measured in this test; as the received voltage had suffered distortion caused by the pilot line, the initial rise of the voltage was slow, and it was difficult to determine accurately the starting point of the voltage rise. However, there was a clear minimum in the value of t_{GH} as R_2 was varied : for high values of R_2, the charge/discharge of the line is slow, as indicated by the measurements described in Sec. 11.2; when R_2 is low, the rate of rise of the transmitted waveform is slow, as shown in Fig. 28. The minimum t_{GH} therefore occurs at an intermediate value of R_2, which Fig. 29 shows to be approximately 400 ohms for this particular pilot line : the time t_{GH} for the chosen value of R_2 = 220 ohms is thus only slightly above this minimum value.

The waveforms for both parts of this first test were recorded using an oscilloscope having a "differential input" pre-amplifier, eliminating the need to earth any point on the line, and thus maintaining the electrical balance of the system. The pulse duration was extended to 500 μsec., when necessary, to ensure that with all values of R_1 and R_2 the full amplitude of received pulse was attained.

The second test was to investigate the effect of varying $R_1/2$, with R_2 set to a constant value of 200 ohms. This test also was in two parts. In the first part, the waveform of the voltage pulses v_{JK}, (Fig. 27), received from the substation and developed across one comparator winding of the transformer at the Control Centre was measured. Typical waveforms of v_{JK} and the line voltage v_{GH} are shown in Fig. 32, for $R_1/2$ = 600 ohms. As the value of $R_1/2$ was raised, the differentiating action of the transformer inductance L became more pronounced, and the difference in the waveforms of v_{GH} and v_{JK} increased, as explained in Sec. 11.3. The difference t in the times for v_{GH} and v_{JK} to reach a given reference value was measured, and for comparison with the calculations in Sec. 11.3, this reference value was made equal to one-half of the amplitude of v_{GH}. The results are shown in Fig. 33, which is a graph of t plotted against $R_1/2$. This may be used to verify the calculations leading to equation (11.3.13) as follows: the 8% total tolerance on L/R_1 specified in Sec. 11.3 can be represented by an 8% variation in $R_1/2$, as L is constant throughout the tests; for a nominal value of $R_1/2$ = 470 ohms, this is a variation of 37.6 ohms. Referring to Fig. 33, the corresponding variation in t is 0.92 μsec. Now the time for v_{GH} to rise to half-amplitude is only 70 μsec., compared with 100 μsec. in Sec. 11.3. Thus the value of t derived above, compared with the value of 1.4 μsec. taken in Sec. 11.3, gives a satisfactory support to the assumptions made in obtaining equation (11.3.13).

The second part of this second test was to determine the effect of the value of R1/2 on the overswing of transformer voltage that occurs after a pulse has been transmitted. Sufficient time must be allowed for this overswing to die away before a pulse is received, if an error in received pulse timing is to be avoided. The waveform of voltage v_{MK}, (Fig. 27), developed across the double comparator winding of the transformer was recorded, and Fig. 34 shows the negative-going overswing following the transmitted pulse, the positive portion of which is out of the photograph. The smaller pulse

at the right-hand side of the photograph is a received pulse, and is not significant in this test. The time t_o from the start of the transmitted pulse to the point where the negative overswing voltage rose to -20 mV was measured; this value is sufficiently small that if a pulse were received at time t_o after the transmitted pulse, or later, the timing error would be less than 1/20 degree at 50 Hz (from equation (13.1.3)).

The results are plotted in Fig. 35. It will be seen that with the value of R1/2 = 470 ohms chosen in Sec. 11.4, a minimum time of 3.4 msec. must be allowed between transmission and reception of a pulse. This requirement is easily satisfied using the timing cycle described in Sec. 15.1.

14.3 Line delay reciprocity tests

As described in Sec. 6.2, the accuracy of compensation for transmission delay in the pilot line depends on the equality of time delay for pulses transmitted in opposite directions along the line. If these are not equal, there will be an error in the phase angle indication equivalent to one-half of the difference in the delay times. A number of typical pilot lines were provided by the M.E.B., both ends of each line being available in the University laboratory. Using the arrangement of Fig. 27, pulses were transmitted via T_1 to the line under test, and an accurate measurement made of the time delay between generation of the pulse at terminals 1, 4 of T_1, and the instant when the voltage received at terminals 7, 10 of T_2 attained the 1 volt reference value. The measurement was then repeated after the line connections had been reversed, end to end. The results are given in Table 3. Most of these lines have been laid for many years, and their physical length is not known. A rough estimate can be made of their length from the values of time delay measured. Assuming a cable of 12 miles length (the maximum distance specified) with a velocity factor of 0.5, the time delay will be $12 \times 10^6/186,000 \times 0.5 = 129$ μsec. It would appear, therefore, that cable J in the table is considerably longer than the maximum specified, even after allowance has been made for the equivalent

delay caused by the distortion of the waveform by the line and line transformers. Taking the remaining cables, the greatest difference in the "forward" and "reverse" time delays is for cable H, and this time difference would result in an error of 3.5/2 x 55.5 = 0.032 degree in the phase angle indication.

Line	d.c. loop resistance ohms	delay time μsec. forward	reverse	difference μsec.
A	206	51.0	51.0	0
B	307	71.0	71.0	0
C	375	75.0	75.0	0
D	375	104.5	104.5	0
E	570	103.5	104.0	0.5
F	600	172.0	170.5	1.5
G	620	118.5	118.0	0.5
H	708	140.5	137.0	3.5
I	784	161.0	158.5	2.5
J	979	235.5	240.5	5.0

TABLE 3. Comparison of transmission delay times for pulses propagated in opposite directions along pilot lines.

The assumption made in Sec. 6.2, that $t_A' = t_A$, and $t_B' = t_B$, depends upon these results. It would have been reassuring if the tests could have been extended to include a larger number of different types of pilot lines. However, the provision of even this number of lines represented a considerable effort on the part of the M.E.B. staff, and some operational inconvenience to them. There was also a limit to the number of different pilot lines available. An attempt to provide more lines would probably have necessitated the use of a line already measured to form part of a longer line, with possibly misleading test results.

14.4. Effect of variations in L_1 - tests

The object of this test was to determine experimentally the effect on the transmission delay of variations in the leakage inductance L_1 of the line transformers. The arrangement described in Sec. 14.3 (Fig. 27) was used, but in series with the winding 5, 6 on transformer T_1 an inductor was connected, the value L_x of which could be varied. As L_x was increased, the transmission delay increased, due to the reduction in bandwidth of the transmitted pulse. Measurements of this increase in delay were made on each of the pilot lines provided by the M. E. B., for four values of L_x, and the results are given in Table 4.

	L_x, mH				
Line	0.135	0.582	1.313	2.313	1.00
A	0.5	1.5	3.0	4.5	2.4
B	0.5	2.0	3.5	6.5	2.9
C	0.3	2.0	3.5	6.5	2.9
D	1.0	3.0	5.5	9.0	4.4
E	0.5	2.0	4.5	9.0	3.4
F	1.0	4.0	8.5	14.0	6.6
G	1.0	3.0	6.0	10.5	4.7
H	1.0	3.0	7.0	12.0	5.3
I	1.0	3.0	9.5	14.5	6.2
J	0.5	4.0	10.5	18.5	7.7
K	2.5	5.0	12.0	19.0	9.0

TABLE 4. Increase in transmission delay (μsec.) with simulated increase L_x in transformer leakage inductance.

The values of delay for L_x = 1 mH were obtained by interpolation, enabling a comparison to be made with the calculations in Sec. 11.6.

It will be seen that the results of the test give good support to the tolerance of $\pm$ 1 mH specified by the calculations.

14.5 Effect of variations in L - tests

These tests were made to confirm experimentally the correctness of the assumptions and calculations made in Sec. 11.3, concerning the effect of variations in transformer inductance L on the pulse timing. As mentioned in Sec. 12.1, two line transformers were made having inductance L (Fig. 15) adjusted to 0.5 H (serial no. 1) and 0.525 H (serial no. 2), representing the 5% tolerance specified. The tests were carried out using the arrangement of Fig. 27, with line "X" (Sec. 11.2) as the pilot line.

With $R_1/2$ and R_2 of values 470 and 200 ohms respectively, the time delay between the generation of the transmitter pulse at terminals 1, 4 of T_1, and the instant when the voltage received at terminals 7, 10 of T_2 attained the value V_{ref}, was accurately measured for various values of V_{ref}. These measurements were made using first the 0.5 H transformer, and then the 0.525 H transformer in position T_2, a third transformer being used at T_1 throughout the tests. The amplitude of the received pulse voltage across the terminals 7, 10 was 3.4V, for both transformers.

The results are given in Fig. 36. For the value of V_{ref} = 1 volt chosen in Sec. 13.1, the timing error caused by the 5% change in primary inductance L is 2.2 μsec., corresponding to an error of 1/25 degree at 50 Hz. In view of the assumptions made, this is considered in satisfactory agreement with the value obtained by calculation in Sec. 11.3.

14.6 Effect of variations in transformer self-capacitance - tests

The difficulty of achieving a close tolerance on values of primary inductance, leakage inductance and self-capacitance simultaneously in a transformer has already been stressed in Sec. 11.3.

14.7 Variations of delay between transformer samples

The effect of the manufacturing tolerances on the line transformers was determined experimentally, by measurement of the transmission delay using the arrangement of Fig. 27. The 0.525 H transformer (ser. no. 2) was used for T_1, while at T_2 the remaining transformers were connected, in turn, and the delay accurately measured. The transformers were made in two batches, separated by an interval of some two years : the pilot line "X" used to test the first batch was not available when the subsequent transformers were tested, and the difference in transmission delay between the two groups is therefore of no significance.

The propagation delay T_{12} between a pulse generated at terminals 1, 4 of T_1 and subsequently attaining the 1 volt reference level at terminals 7, 10 of T_2 was measured. The corresponding delay T_{21} for pulses travelling in the reverse direction, i.e., generated at terminals 1, 4 of T_2 and received at terminals 7, 10 of T_1, was also measured. These two tests were repeated for each sample of transformer at T_2. The variation of T_{12} between samples of T_2 will be caused mainly by variations in L, as given in equation (11.3.12), while the variation in T_{21} is due chiefly to variations in transmitted bandwidth caused by the tolerance on L_1, as indicated in equation (11.6.10). The results in Table 6 show the consistency of propagation delay with the different transformers: bearing in mind that the error in phase angle indication will correspond to one-half of the delay difference between transformers shown in the Table, these results are considered entirely satisfactory.

15.1 SYSTEM TIMING CYCLE

For proper operation of the system, it is essential that the primary, secondary and tertiary pulses are generated only when the pilot line and associated transformers are fully discharged. If this condition is not satisfied, then any charge remaining from previous transmitted pulses may cause a residual voltage to exist at the voltage comparator terminals when a pulse is received, with a consequent error in the timing of this pulse, and in the phase angle indication. The relative timing of primary, secondary and tertiary pulses is therefore important, and is controlled by the time delays T_s and T_d (Sec. 6.2). Fig. 37 shows the timing sequence for one complete cycle of operation, using the system described in Sec. 6.3; the pilot line voltages at the two substations are given at (a) and (b), while the voltage on the corresponding pilot lines at the Control Centre is given at (c) and (d). The primary, secondary and tertiary pulses are transmitted on "odd" cycles; "even" cycles contain primary pulses only.

The values of T_s and T_d must be chosen to allow a minimum time interval T_m to elapse after the generation of a given pulse at either end of the line, before another pulse is received or generated. The critical intervals are lettered A to F in Fig. 37, and may be expressed in terms of the system time delays as follows:

$$A = 2t_A + T_s \quad \text{---} \quad (15.1.1)$$

$$B = t_A + t_B + T_s - t_\phi' \quad \text{---} \quad (15.1.2)$$

$$C = 2t_A + T_d \quad \text{---} \quad (15.1.3)$$

$$D = 2t_B + T_d \quad \text{---} \quad (15.1.4)$$

$$E = \frac{1}{f} - 2t_A - T_s - T_d \quad \text{---} \quad (15.1.5)$$

$$F = \frac{1}{f} - t_A - t_B - T_s - T_d + t_\phi' \quad \text{---} \quad (15.1.6)$$

The smallest (i.e., most critical) values of A, B, C, and D will exist when t_A and t_B are zero, and t_ϕ' is a maximum positive.

The smallest values of E and F will occur with the maximum values of t_A and t_B, and with the largest negative value of t_ϕ. Applying these conditions to the equations given above,

$$A_{min} = T_s \qquad \text{---} \qquad (15.1.7)$$

$$B_{min} = T_s - t_{\phi max.} \qquad \text{---} \qquad (15.1.8)$$

$$C_{min} = D_{min} = T_d \qquad \text{---} \qquad (15.1.9)$$

$$E_{min} = \frac{1}{f} - 2t_{Amax.} - T_s - T_d \qquad \text{---} \qquad (15.1.10)$$

$$F_{min} = \frac{1}{f} - t_{Amax.} - t_{Bmax.} - T_s - T_d - t_{\phi max.} \qquad \text{---} \qquad (15.1.11)$$

Assuming that the available time is to be distributed, as far as is possible, equally between the critical intervals given above, the best values of T_s and T_d may now be calculated. Clearly, B_{min} is smaller than A_{min}; equation (15.1.8) therefore represents a more onerous condition for T_s than does (15.1.7). Similarly, F_{min} is smaller than E_{min}. We may therefore discard (15.1.7) and (15.1.10). Equating the remaining critical intervals B_{min}, $C_{min} = D_{min}$, and F_{min}, in turn, to T_m we have :

from (15.1.8) $$T_s = T_m + t_{\phi max.} \qquad \text{---} \qquad (15.1.12)$$

from (15.1.9) $$T_d = T_m \qquad \text{---} \qquad (15.1.13)$$

from (15.1.11)

$$T_m = \frac{1}{f} - t_{Amax.} - t_{Bmax.} - T_s - T_d - t_{\phi max.} \qquad \text{---} \qquad (15.1.14)$$

Substituting, in the above equation, T_d and T_m from (15.1.12) and (15.1.13),

$$T_s = \frac{1}{3}\left[\frac{1}{f} - t_{Amax.} - t_{Bmax.} + t_{\phi max.}\right] \qquad (15.1.15)$$

Hence, from (15.1.12) and (15.1.13),

$$T_d = T_m = \frac{1}{3}\left[\frac{1}{f} - t_{Amax.} - t_{Bmax.} - 2t_{\phi max.}\right] \quad \text{---} \quad (15.1.16)$$

Taking the maximum pilot line transmission delay $t_{Amax.}$ and $t_{Bmax.}$ as 0.2 msec. (Sec. 14.3), and $t_{\phi max.}$ as 1.39 msec. (corresponding to the maximum phase angle of 25^{o}), then

$$T_s = \frac{1}{3}\left[\frac{20}{1000} - \frac{0.4}{1000} + \frac{1.39}{1000}\right] = 7 \text{ msec.} \quad (15.1.17)$$

$$T_d = \frac{1}{3}\left[\frac{20}{1000} - \frac{0.4}{1000} - \frac{2.78}{1000}\right] = 5.6 \text{ msec.} \quad (15.1.18)$$

$$T_m = T_d = 5.6 \text{ msec.} \quad \text{---} \quad (15.1.19)$$

This value of T_m easily satisfies the requirement of 3.4 msec. obtained in Sec. 14.2. There is therefore no need for great accuracy in the value of T_s, and a simple multivibrator is adequate for the generation of this time interval. Also, a precise value of T_d is not required, although it is essential that the values of T_d generated in the various substation equipments shall be closely similar, as described in Sec. 7.1. Therefore, although a quartz crystal oscillator is required to define the period T_d, an oscillator frequency of 100 kHz has been chosen, allowing the use of readily available crystals. When used with a nine-stage binary frequency divider, the period is then 5.115 msec.

The required values of period of the multivibrators M1 - M4, Fig. 13, may now be calculated. The multivibrator M4 acts as the element M in Sec. 4.3 and Fig. 1, and is triggered by the

primary pulses received from line A. As described in Sec. 4.3, no great accuracy of period is required for this action : M4 is therefore used also to define the time T_s, and thus has a period T_{M4} = 7 msec., from equation (15.1.17).

The multivibrator M3 also acts as the element M in Fig. 1, and is triggered by the tertiary pulses received from line A. Again, great accuracy of period T_{M3} is not important, so long as it is greater than the maximum time difference between a tertiary pulse received from line A, and a subsequent and corresponding pulse received from line B. Since this time difference is equal to twice the difference in transmission delay of the lines, a value of T_{M3} = 1.2 msec. is adequate.

M2 generates the secondary pulses; it therefore has a period T_{M2} = 200 μsec.

The action of multivibrator M1, in conjunction with the gates G1A, G2A, G1B and G2B, (Fig. 13), is to steer the primary and tertiary pulses into M4-B22, and M3-MB21, respectively. It is triggered, on alternate cycles, when M4 returns to the "0" state. Again, great accuracy of period T_{M1} is unnecessary,so long as it is sufficient to ensure that the tertiary pulses are directed always into M3 and MB21. Since M1 is triggered simultaneously with M2, (Fig. 13), the period must be not less than the interval between the generation of secondary pulses, and the receipt of the corresponding tertiary pulses. Thus, from Fig. 37, T_{M1} must exceed the sum of T_d and twice the maximum transmission delay. A value of T_{M1} = 8 msec. was therefore chosen.

16.1 RELIABILITY

A high degree of reliability is required of this equipment, ie., it must continue to function within specification for long periods of time. As mentioned in Sec. 9.1, the existence of a fault condition should be immediately obvious from the operation of the equipment, and some of the methods of ensuring this are described in that Section. The amount of development time which can justifiably be devoted to reliability considerations in a project is ultimately a matter of economics, and this is influenced by the cost of damage to associated apparatus consequent upon a failure. The result of a total loss of the phase angle information might possibly preclude the linking together of two substations, with attendant difficulties in operation of the power distribution system. An incorrect indication of phase angle could, however, lead to the interconnection of substations at a time of excessive phase difference, thus possibly resulting in extensive damage to the switchgear. For this reason a substantial fraction of the development time has been spent on reliability aspects of the design.

The design methods to be used to ensure high reliability must be related to the conditions under which the equipment has to work, to the methods of maintenance to be used, and to the knowledge and skill of the maintenance staff. For example, protection has had to be provided against high voltages delivered from the pilot lines into the substation and Control Centre units, by inadvertent "routine" insulation testing of the lines. A decision was made at an early stage in the project, that no attempt should be made to repair a unit in the field : the unit should be replaced as a whole, and the repair carried out in the base repair workshop. Routine maintenance should be unnecessary, although periodic overall functional checking of the units will be undertaken. It is

strongly felt that unnecessary disturbance to the inside of the equipment should be avoided, as past experience has most clearly shown the reduction in reliability that can be brought about by excessive maintenance procedures.

The design procedures and philosophy outlined in MIL HDBK 217A[28] were, as far as possible, followed throughout the project.

16.2 Design methods for reliability

There are three levels of design at which reliability must be considered. The first level is at the "block diagram" stage in the design; the choice of a system of operation to minimize the number of circuits required, and to reduce the consequences of a failure. Much of this has been described in the preceding Sections, but a further simple example will be given. In the F. T. M. substation unit, two a. c. inputs were used. One input was used to supply the d. c. voltages required to operate the unit, while the other input supplied the test voltage from which the phase measurement was to be made. A fuse was provided in each of these inputs to the unit. This arrangement did not satisfy the "fail-safe" requirement of the system. In the event of the fuse in the test voltage input blowing, the input impedance and sensitivity of the zero-crossover voltage comparator are so high that the comparator could continue to function, being actuated by current flowing in a leakage path, or via the capacitance between the terminals of the ruptured fuse. The phase angle then indicated would probably be greatly in error from the true value. Such a false mode of operation was avoided by the connection of a resistor across the test voltage terminals; of value low enough to prevent an appreciable voltage being developed when the fuse was blown : this is not a complete solution to the

problem, however, as an open-circuit failure of this resistor would, if undetected, leave the system liable to error as before. In the M. S. E. V. unit, the d. c. supplies are derived from the source of test voltage, and only one fuse is fitted : reliability is thus improved in that operation of the unit is impossible if the fuse blows, and also by the elimination of a plug, socket and fuse, as only one a. c. input is required.

The second level of design is concerned with the design of the circuits to be used. Some of these will be described in detail in following Sections, but certain general rules have been followed throughout the project :

1. the use only of circuits which are, as far as possible, inherently "fail safe". For example, the avoidance of a synchronized oscillator type of frequency divider, as mentioned in Sec. 7. 2.

2. the use only of circuits whose significant performance is completely calculable.

3. the use of "worst-case" design procedures throughout, i. e., calculations to ensure that circuit performance meets the required specification with components and supply voltages having any value within the tolerance range expected during the life of the equipment.

4. the avoidance of any preset variable components. For situations where initial adjustment is required as, for example, to accommodate the voltage tolerance of a Zener reference diode, a fixed-value component of value selected by test has been used.

5. the avoidance, or reduction to a minimum, of variable components, switches, relays, plugs and sockets, blower motors or other components known to have a poor reliability record, taking into account the expected life of the equipment.

6. adequate derating of electrical and thermal stresses on components.

7. the avoidance, so far as is possible, of a situation where an unknown stress is applied to a component. For example, adequate precautions to ensure that transient mains-borne supply voltages are not transmitted to the circuits.

8. the use only of circuits allowing the electrical stresses on components to be calculated. This is equivalent to the statement that it must be possible to calculate the voltage and current in any part of the circuits, at all times in the cycle of operation. When all the transient conditions of operation of a circuit are considered, this is a stringent requirement, and leads to the rejection of many circuits in common use.

9. the use of circuits in which voltage and current levels are arranged, wherever possible, to coincide with the component manufacturer's guaranteed test conditions. If this is not possible, (due, for instance, to derating of stress) then the possible change in characteristics of the component should with confidence be known.

10. recognition of the most likely failure mode of the components. For example, when using a Zener diode to provide an accurate voltage reference, a resistance potential divider is used, the ratio of which is adjusted on test by selection of the value of one resistance. This usually requires the use of a pair of resistors to obtain an accurate total value of resistance. In this case, the most likely failure mode of a resistor is open - rather than short-circuit. With the resistor pair connected in parallel, the failure of one resistor could result in an undetected error in the reference voltage : the series connection is therefore used, in spite of a slight increase in the probability of catastrophic failure.

The design of circuits using the rules given above requires, above all, that the design methods shall be simple. This has been achieved by dividing the complete circuit for the equipment into elementary sub-circuits. By the use, in many cases, of a deliberate mismatch between sub-circuits, the operation of each is little affected by the others to which it is connected. A straightforward design method for each of the subcircuits can then be devised, avoiding the need for elaborate analysis and computation : a further advantage is the ease with which the test procedures can be carried out.

The third level of design relates to selection of the components. Here the rule was to use components well established and in widespread use. It is a great temptation to a designer to exploit the improved performance of a new type of component; this was firmly resisted. Also avoided was the choice of components with values at the limits of the range manufactured. With resistors, for example, values at the upper limit for a given physical size will require a resistive film so tenuous that it may be prone to failure. Similarly, a capacitor having the maximum value for a given size will often have reduced clearances, or thickness of the protective covering. In addition to the possible reduction in reliability, it is not uncommon to find that characteristics such as temperature coefficient and stability with time suffer degradation at extreme values in a given range. Since there was no restriction on the physical size of the equipment for this project, components of generous size and rating were used.

There are two ways in which failure can occur : breakdown (catastrophic failure) of a component, or degradation of its characteristics to the point where operation within specification no longer occurs. It is often possible to reduce the effect of one of these failure modes, at the expense of the other. For example, degradation failures can often be reduced by the addition of extra

components, with a consequent increase in the total number of components, and hence possibly the likelihood of catastrophic failure. One of the tasks of the circuit designer, therefore, is to arrange the circuit configuration to achieve a balance between the two types of failure, to obtain a minimum overall failure rate. To carry out such a design it is essential that reliability data be available, and considerable weight was therefore given, in the choice of components for this project, to the availability of this reliability data.

16.3 Environmental testing of circuits

In addition to environmental tests on the completed equipments, the basic circuits used were separately tested. In some cases, a single sample of a circuit which had been developed was tested over a range of temperature and supply voltages; in other cases a number of similar circuits were constructed and operated for an extended period, to detect any possible long-term deterioration in performance. The results of these tests are given in the Section in which the design of the particular circuit is described.

Much of the detailed design of the circuits was carried out during development of the F. T. M. (Sec. 2.1). Although a high long-term reliability was not required in these units, the decision was taken to develop reliable circuits at this stage, to save later partial duplication of development effort, and also to obtain some experience of the circuit behaviour under typical operational conditions. This decision was fortunate, as by the time the F. T. M. tests were complete, insufficient time remained to allow the redesign of the Control Centre unit : a complete redesign of the substation unit, to use integrated circuits, was, however, accomplished.

16.4 Prediction of equipment reliability

At an early stage in the project, a quantitative estimate of the reliability required of the equipment had to be made. No small difficulty was experienced in deciding upon an acceptable failure rate. While the importance of high reliability has been much stressed, it would appear pointless to specify a degree of reliability vastly in excess of that relating to the other parts of the power distribution system with which the phase measurement system is to work. Ultimately it was agreed that for the complete system a Mean Time Between Failures (M. T. B. F.) of "several years" would be acceptable.

To achieve a given system reliability, the M. T. B. F. required in each unit will, of course, depend on the number of substations to be equipped. It was assumed that the ratio of substation to Control Centre units would be at least 12. The attainment of a high M. T. B. F. in each substation unit was therefore particularly important. Throughout the design, a constant endeavour to simplify the substation unit was made, while concentrating any necessary complexity in the Control Centre unit.

The degree to which the required reliability has been achieved will be known only after many years operation of the equipment. However, a reliability forecast can be made, based on past experience of the failure rate of the component parts. The greatest caution should, of course, be observed in interpretation of such a forecast, as there are many parts of a system for which no failure rate can be known; for example, there is no way of forecasting the failures which may arise from accidents or faulty maintenance. Also, for many of the components used, the only reliability data available were obtained under conditions differing from those actually used : when this occurred, however, the effect of derating ensured that the actual conditions were always of lower stress than those at which the data were obtained;

this lowering of stress can, with some exceptions, be expected to improve the reliability performance above that obtained from the data. In addition to the above, the circuits were designed generally to tolerate, without malfunction, a greater variation in component value than was defined as a "degradation failure": for example, with the resistors used, an excursion of $\pm$ 2% from the initial value is deemed to be a "failure"; many of the circuits used will accept values outside these limits, and still function correctly. The successful outcome of the reliability prediction should therefore be regarded as a necessary, but not sufficient, indication that a satisfactory M. T. B. F. has been achieved. Only time will show the true reliability of the system.

Tables 7 and 8 give the failure rate data for the reliability forecast for substation and Control Centre units respectively, and the notes given below relate to these Tables.

NOTE 1 Extract of letter from SGS-Fairchild Ltd., dated 16th January 1968 : - - - "There is considerable data on microcircuit reliability. I am giving here summation of results of several test programmes.

> 33, 129 Units > 105, 652, 704 Operating Hours

Failure Rate 0. 0042 %/1000 hours at 99% Confidence,

or, 0. 0022 %/1000 hours at 90% Confidence,

or, 0. 00088 %/1000 hours at 60% Confidence."

NOTE 2 Extracts of letters from SGS-Fairchild Ltd., dated 26th August and 23rd September, 1968: - - - "We have, as the cumulative result of many thousands of hours of testing, the following 90 % confidence results for the devices you are considering using :

2N 914	λ	=	9×10^{-6}
BFY 56A	λ	=	0.4×10^{-6}
BFY 64	λ	=	8×10^{-6}
2N 2484	λ	=	1.0×10^{-5}
1N 914	λ	=	0.2×10^{-6}

These figures are based on our own life test measurements."

- - - - "With regard to the definition of failures, we include both catastrophic failures and drift failures in the figures sent to you. The drift limits are outlined in the SURE programme - - - The symbol λ is the Failure Rate and is the L. T. P. D. per 1000 hours."

Extract from SURE manual, p. 6:

"Lot Tolerance Percent Defective (LTPD). This parameter of a sampling plan is the maximum percent defective which will be accepted by the sampling plan at a 90% confidence level."

NOTE 3 As Mullard were unable to supply reliability data, the value of λ was obtained from MIL-HDBK-217A, Fig. 7.4.3A, using normalised junction temperatures of 0.224 and zero for the diode types BZY 78 and BZY 88 respectively. The resulting failure rates appear very high when compared with the diodes type 1N914.

NOTE 4 Extract of letter from Electrosil Ltd., dated 12th November 1968 : - - - - "To date we have accumulated approximatedly 104 million unit hours with one failure giving a failure rate of 0.0019%/1,000 hours with a 60% confidence level. Also of outstanding significance are the failure rate figures obtained with the help of B. O. A. C. The TR style resistor which is used on their VC10 aircraft has accumulated 1,000 million unit hours with zero failures which represents a failure rate of 0.000092 %/1000 hours with a 60% confidence."

The more pessimistic value of λ has been taken, in spite of the derating used.

NOTE 5 Extract of letter from Salford Electrical Instruments Ltd., reference KBT/AH, dated 17th December 1969 : - - - -
"It is believed that the failure rate for crystals of low frequency in a low stress environment may be better than 0.1% per 1000 hours."

NOTE 6 Extract from Mullard booklet, "Electrolytic and Polyester Capacitors, Quality and Reliability" :
p. 8, " --- if L_1 and L_2 are the average service lives, at applied voltages V_1 and V_2 respectively, then

$$\frac{L_1}{L_2} = \left[\frac{V_2}{V_1}\right]^x$$

where x is a factor which generally has a value between 4 and 6."
p. 9, referring to extended foil capacitors "for 160V types, the failure rate at the nominal voltage will be less than 0.02% per 1000 hours"
p. 9, referring to metallised film capacitors, (the type used in the equipment) " - - - the failure rates of the metallised film capacitors must be appreciably better than those for the foil capacitors."

Since the maximum voltage applied to any of these capacitors does not exceed 12, and 250V capacitors have been specified, the voltage stress ratio is 12/250 = 0.048. However, in accordance with MIL-HDBK-217A, para. 7.2.1, this has been limited to 0.1, resulting in a value of $\lambda = 0.02 \times 1/10^4 = 2 \times 10^{-6}$ %/1000 hours.

NOTE 7 Extract of letter from Salford Electrical Instruments Ltd., reference KBT/AH, dated 17th November 1969: "We have supplied Polystyrene Capacitors to Messrs. G. E. C. Telephone Works, Coventry, who have reported a failure rate of better than 0.01% per 1000 hours. The Type RPF is manufactured under more stringent conditions of Quality Control than the ordinary Polystyrene Capacitors. The reduction in voltage and temperature stress in your proposed application will improve the reliability and therefore the failure rate will be considerably better than the 0.01% per 1000 hours quoted."

NOTE 8 Dummer, G. W. A., "Electronic-circuit connections. Part 2 - Plugs and sockets and permanent joints". Electronics and Power, vol. 12, July 1966. p. 260, "The total of soldered joints - - - on which satisfactory information is available is 3,390,880. With total component hours of 99,822,497,000 and total failures of 134, the overall failure rate is approximately 0.00014% per 1000 h."

NOTE 9 For the Control Centre unit, no numerical value of reliability data was available for the meter or the rotary switches for substation selection. For the substation unit no data existed for the 110V/110V isolating transformer from which the 50 Hz test voltage is obtained. For both units, no reliability data was available for the pilot line transformers, or connectors. It is not expected that the reliability of the system will be much affected by these components, as the meter and the transformers were specially made for the project, with high reliability a feature of the specification.

Item	Quantity	Component type	λ, per component	% confidence	Source		λ, per component type.
1	14	Integrated circuits	2.2×10^{-2}	90	SGS-Fairchild.	Note 1.	0.308
2	1	Transistor 2N914	9×10^{-5}	90	SGS-Fairchild.	Note 2.	0.00009
3	1	Transistor BFY64	8×10^{-5}	90	SGS-Fairchild.	Note 2.	0.00008
4	2	Transistors BFY56A	4×10^{-6}	90	SGS-Fairchild.	Note 2.	0.000008
5	8	Diodes IN914	2×10^{-6}	90	SGS-Fairchild.	Note 2.	0.000016
6	1	Zener diode BZY78	0.6		MIL-HDBK-217A	Note 3.	0.6
7	1	Zener diode BZY88	0.3		MIL-HDBK-217A	Note 3.	0.3
8	31	Resistors, metal oxide	1.9×10^{-2}	60	Electrosil	Note 4.	0.589
9	1	Quartz crystal	<1.0		S.E.I.	Note 5.	<1.0
10	6	Capacitors, polyester	2×10^{-5}		Mullard	Note 6.	0.00012
11	3	Capacitors, polystyrene	<0.1		S.E.I.	Note 7.	<0.3
12	200	Soldered joints	1.4×10^{-3}		Dummer	Note 8.	0.28
						Total	<3.38

TABLE 7. Failure rate forecast for substation unit, excluding power supply, and isolating and line transformers.

The failure rate, λ, is given in failures per million component hours.

Item	Quantity	Component type	λ, per component	% confidence	Source		λ, per component type.
1	10	Transistors 2N2484	1×10^{-4}	90	SGS-Fairchild.	Note 2.	0.001
2	32	Transistors 2N914	9×10^{-5}	90	SGS-Fairchild.	Note 2.	0.000288
3	4	Transistors BFY56A	4×10^{-6}	90	SGS-Fairchild.	Note 2.	0.000016
4	2	Transistors BFY64	8×10^{-5}	90	SGS-Fairchild.	Note 2.	0.00016
5	75	Diodes IN914	2×10^{-6}	90	SGS-Fairchild.	Note 2.	0.00015
6	3	Zener diodes BZY78	0.6		MIL-HDBK-217A.	Note 3.	1.8
7	2	Zener diodes BZY88	0.3		MIL-HDBK-217A.	Note 3.	0.6
8	191	Resistors, metal oxide	1.9×10^{-2}	60	Electrosil.	Note 4.	3.6
9	12	Capacitors, polyester	2×10^{-5}		Mullard.	Note 6.	0.00024
10	15	Capacitors, polystyrene	< 0.1		S.E.I.	Note 7.	< 1.5
11	4	Capacitors, tantalum				Note 9.	
12	1000	Soldered joints	1.4×10^{-3}		Dummer.	Note 8.	1.4
						Total	<8.91

TABLE 8. Failure rate forecast for Control Centre unit, excluding power supply, meter, selector switches and line transformers.

The failure rate, λ, is given in failures per million component hours.

The difficulty of making a satisfactory and meaningful reliability forecast can be appreciated by a study of the last column in Tables 7 and 8. There is little doubt that the wide variations in failure rate between different types of components reflects the source of reliability data rather than the inherent reliability of the components : this is evident in the comparison of the failure rates of item 5 with items 6 or 7, or the polyester and polystyrene capacitors. However, the total failure rates are so low that the M. T. B. F. is likely to be controlled mainly by other types of failure in the system.

The most important causes of possible failure in the system appear to be the power supplies, and the pilot lines. The stabilised supplies use transistors operating in the linear mode with appreciable power dissipation, and it can perhaps be expected that their life will be shorter than that of transistors in the rest of the equipment, most of which operate in the switching mode, with a very small power dissipation. The specification for the power units places great emphasis on reliability, and the manufacturers have quoted "we will aim, in design, for an extended M. T. B. F. of 5 years, remembering that component selection and derating will be such as to see an extended minimum long-term reliability of 10 years." An M. T. B. F. of 5 years is equivalent to a failure rate of 22. 8 per million hours, and is thus many times the failure rate for the remainder of a unit. The overall failure rate of the equipment is thus dominated by that of the power supplies, and an approximation to the M. T. B. F. of the whole system in years thus becomes 5/(1 + no. of substation units). For a system having a large number of substation units this gives an M. T. B. F. for the whole system below that envisaged as necessary. A large improvement in the reliability of the power supplies seems hardly possible: it wouldbe a courageous (or foolhardy) manufacturer who would guarantee an M. T. B. F. greatly in exess of 5 years, even if he thought that such an extended time might be achieved. Redundancy in the power units could, of course, be employed to reduce the

probability of failure, but new reliability problems might then well be encountered.

The other important cause of possible failure is the pilot lines. No reliability data on these is available, but it is not expected that their failure rate will be any less than that of the power supplies. Here, again, redundancy might be used, but it is unlikely that duplicate pilot lines would be available for many of the substations.

It appears that a reconsideration of the required "several years" M. T. B. F. for the whole system may be necessary, in the light of the pilot lines available and what is technically feasible in the equipment at reasonable cost. If a higher degree of reliability than that provided by the present equipment is ever found to be required, then perhaps it would be best to use complete duplication of the units and the pilot lines.

17.1 DESIGN OF THE CONTROL CENTRE UNIT

Unlike the substation units, there has been only one major design of the Control Centre unit. This was carried out for the Field Trials Model of the equipment, and discrete components were used throughout. By the time the F. T. M. was installed and operating, insufficient development time remained to allow the redesign of both substation and Control Centre units for the Multi-Station Engineered Version of the equipment. The substation unit was therefore redesigned, to exploit the reputed high reliability of integrated circuits, but only detail modifications could be made to the Control Centre unit. However, it is not expected that any great improvement in performance or reliability would accrue from a complete redesign of the unit, although some simplification of the circuits could probably be made.

One of the first decisions was the value of the d. c. supply voltages to be used. Generally, a low supply voltage favours high reliability operation by minimizing the temperature rise of the components, and by allowing them to be run at a low voltage stress. On the other hand, an advantage of a higher supply voltage is the large resistance to degradation of performance by electrical noise that it is possible to design into the circuits. A further advantage is that the variation in semiconductor saturation voltages that occurs with age and operating conditions may be "swamped out" by the use of a high supply voltage : circuits may then be designed more effectively to operate over long periods of time with predictable performance. This is particularly valuable in the design of the voltage comparators, the monostable multivibrators and the current switch. Another factor that applied to the F. T. M. was the possibility that the equipment might be required to operate using a lead-acid battery as a power supply. These considerations lead to the choice of d. c. supply voltages of +12 and -12, relative to earth.

No attempt to give a detailed design of all circuits used in the equipment will be made. However, in the following Sections the design of the major circuits will be discussed, and this should enable the remainder of the circuit design to be readily understood.

The circuit diagram of the complete Control Centre unit is shown in Fig. 38, which should be read in conjunction with the logic diagram, Fig. 13. A list of components used is given in Appendix A. Pilot lines from the substations are connected, via the coupling networks, to the line transformer windings A3 and B3. The comparator windings A1 and B1 on these transformers deliver the line pulses to the voltage comparators VCA and VCB, which are protected from excessive voltage input by the diodes D4, D5 and D51, D52 for inputs A and B respectively. The 1 volt reference for the comparators is obtained from the Zener diodes D1 and D 3, via the potential dividers, the resistance values of which are adjusted on test to accommodate the spread in diode voltage.

The output from the voltage comparators is applied to the gating diodes D11 and D16, corresponding to G1A and G2A (Fig. 13), and D58 and D63, corresponding to G1B and G2B, respectively. The capacitors C1, C2, C15 and C16, together with the associated resistors, function as the logical delays D6, D5, D7, and D8 respectively. An input to these gates is taken, via the diodes D9, D10 and D56, D57, from the transistors TR1 and TR6, whose action gives a warning indication should a pilot line be inadvertently connected with reversed polarity.

The voltage output from the diode gates causes the multivibrators M4, M3, B22 and MB21 to be triggered, as described in Section 8 : the multivibrator output voltages control the positive and negative current generators PCG and NCG, by the action of the gates G3 - G8, (Fig. 13). For the positive current generator, the diodes D20 and D21 correspond to G5, while D22 and D23 correspond to G3. The transistors TR20 and TR21 form the gate G7.

The diodes D27, D28, D25, D26 and transistors TR18, TR19 act in similar fashion for the negative current generator. The amplitude of the current pulse in the meter circuit is controlled by the Zener reference diode D2 , and the resistors R53-4 and R62-3, which are adjusted on test to suit the particular Zener diode used. The current pulses are smoothed by the capacitors C5 and C6 before being applied to the meter.

The secondary pulses are generated by the multivibrator M2, and amplified by the transistor pairs AA and AB before application to the transmitter windings A2 and B2 on the line transformers. The diodes D29-D34 protect the output transistors from excessive voltage that may be generated within the transformers, or received from the pilot lines.

The red and green warning lamps are supplied with current from the multivibrator A. This is basically an astable multivibrator, but the oscillations may be inhibited by the saturation of transistor TR41; this can occur only when base current for TR41 is being supplied from the diode pump, which is driven by the multivibrator M5.

18.1 VOLTAGE COMPARATOR DESIGN

The voltage comparator (VCA and VCB in Fig. 13) should give an output voltage pulse when the input voltage received from a substation rises to the standard value V_{ref}. It is obviously important that the value of input voltage to operate the comparator should be maintained close to V_{ref} throughout the life of the equipment. Equation (13.1.3) and the following paragraph shows that an error ΔV_{ref} of 85 mV can result in an error of 0.1^{o} in the phase angle indication. The design of the comparator should therefore aim to achieve an error preferably much less than this value.

In designing the comparator, a decision to be made concerns the possible use of regeneration. The advantage of the use of regeneration is that the output voltage waveform is then not significantly dependent on the rate of rise of the input voltage. If regeneration is not used, the comparator then may be regarded as a saturating amplifier, and the rates of rise of output and input voltage will be related. Now the rate of rise of the line voltage calculated in equation (13.1.2) is 7660 v/sec: the input voltage to the comparator from the double winding on the line transformer will thus rise at 15320 v/sec; signals received from actual pilot lines tested have shown rates of rise always exceeding this value. If a non-regenerative comparator of voltage gain 250 or more, and having an adequate high-frequency response, is used, then the rate of rise of output voltage should always be greater than 3.83 v/μsec; this value should be ample to ensure the triggering of subsequent circuits with negligible time error.

Because of the simplicity of design method possible, and the lack of necessity for control of the hysteresis characteristic of regenerative comparators, it was decided to use the non-regenerative type, and to aim for a voltage gain not less than 500. To obtain this value of voltage gain, an amplifier having at least two stages

is required. The circuit developed is as shown essentially in Fig. 39, and completely in Fig. 38.

Referring to Fig. 39, the transistors TR1 and TR2, connected in the "long-tailed pair" configuration, form the first stage, and transistors TR3 and TR4, in a similar configuration, the second stage of the amplifier. By adopting this balanced arrangement throughout the amplifier, compensation is obtained for several possible sources of error voltage ΔV_{ref} [32]. The output voltage v_o must be sufficient to trigger the multivibrators M3, M4, MB21 and B22 (Fig. 13) : a negative-going pulse of nominal amplitude 6 volts, having a source resistance of 1.2 kohm, is suitable. In the input circuit the resistor R_1 is used, in conjunction with diodes connected from the base of TR1 to suitable d.c. potentials, to protect the transistors TR1 and TR2 from excessive values of the input voltage v_i : the minimum permissible value of this resistor is used, determined by the allowable loading of the line transformer.

A complete formal analysis of this circuit results in cumbersome algebraic expressions, from which it is difficult to derive meaningful conclusions: following the philosophy mentioned in Sec. 16.2, the design method described below has therefore been used. In discussion of this and subsequent circuits, the currents in the base, collector and emitter of a transistor will be denoted by i_b, i_c and i_e respectively, with a further suffix applying to that of the transistor concerned. A similar system v_b, v_c and v_e for voltages will also be used, these voltages being measured with respect to earth : in other cases, the terminals between which a voltage is measured are indicated in the suffix.

There are several possible modes in which the comparator can be operated. For the mode chosen, saturation of the transistors TR3 and TR4 does not occur; also, saturation of TR1 and TR2 will not occur while both TR3 and TR4 are simultaneously conducting. To obtain the greatest benefit from the balanced configuration, the

values of corresponding resistors should be equal : we will thus put $R_1 = R_2 = R_A$, $R_3 = R_4 = R_B$, $R_5 = R_6 = R_C$. The transistors used (type 2N2484) are guaranteed by the manufacturers to have a minimum common-emitter d.c. current gain $\bar{\beta}$ of 250, with I_c = 1mA and ambient temperature 25°C. Allowing a reduction of 15% for operation at 10°C, and a further 15% for ageing, the lowest value $\bar{\beta}_{min}$ will be 175. A common-base current gain α of unity will therefore be used in the calculations which follow.

The transistor pair TR3-TR4 may be regarded as a commutator, in which the current flowing in R_7 is switched from TR3 to TR4 to generate the output voltage pulse. The commutation occurs with a change in relative base voltage $(v_{b3} - v_{b4})$ of approximately $\pm$ 0.4 volt. For an output pulse of 6V amplitude from a source resistance R_4 = 1.2 kohm, a current i_{c4} = 5 mA is required. Since TR3 is "off" when the pulse is being generated, the required current in R_7 will thus be 5 mA. The maximum base current of TR4 will be $i_{b4max} = i_{c4}/\bar{\beta}_{min} = 5/175 = 0.029$ mA; this current will fall as the ambient temperature rises, due to the increase in $\bar{\beta}_{min}$ with temperature. The effect of variations in i_{b4} can, however, be swamped out by the choice of a value of i_{c2} substantially larger than i_{b4}. An upper limit is set to the allowable i_{c2} by self-heating in the transistors TR1 and TR2, and also by the excessive voltage drop $i_{b1}R_1$ and $i_{b2}R_2$ in the base circuit resistors of these transistors. By the use of an iterative design process, the value of i_{c2} was chosen to be that corresponding to a value of resistor R_8 = 27 kohm: the suitability of this value will be apparent from the calculations given below.

Consider the conditions in the comparator when the transistors TR3 and TR4 are conducting equally; the output voltage v_o will then be near the midpoint of its dynamic range, and the base potentials of these transistors will be approximately

equal. Putting $v_{b3} = v_{b4} = v_b$, then

$$v_b = E_b - (i_{c2} + i_{b4})R_B$$

$$= E_b - \left[\frac{(E_c + V_{ref} - v_{be1})}{2R_8} + i_{b4} \right] R_B$$

---- (18.1.1)

Choice of a suitable value of v_b is important; it must lie within a range having an upper limit set by saturation in TR3 or TR4, and a lower limit set by saturation in TR1 or TR2. As the voltage gain of the transistor pair TR1-TR2 increases as v_b is reduced, a value near the lower limit is preferable.

The value of R_B will now be calculated. As given in Sec. 23.1, the d.c. supply voltages are $\pm$ 12V $\pm$ 1V, with the difference between the values of the positive and negative voltages not exceeding 0.6V. A total variation in resistor values of $\pm$ 2% has been assumed. By inspection of Fig. 39, the worst-case condition for near-saturation of the transistors TR1 and TR2 will be when $E_b = 11V$, $E_c = 11.6V$, $R_8 = 27 - 2\%$ kohm and $i_{b4} = i_{b4max} = 0.014$ mA (for equal conduction in TR3 and TR4). Putting $v_{be1} = 0.7V$, $V_{ref} = 1V$ and $v_b = 1V$ (corresponding to zero collector-base voltage of TR1 and TR2), and substituting these values in equation (18.1.1) gives

$$R_{bmax} = \frac{11 - 1}{\frac{(11.6 + 1 - 0.7)}{52.9} - 0.014} = 41.8 \text{ kohm}$$

---- (18.1.2)

This is the maximum permissible value of R_B to avoid possible saturation of TR1 or TR2, and the nominal value of R_B is therefore 41.8 - 2% = 41 kohm.

With the resistors and supply voltages at their nominal values, and taking a nominal value of i_{b4} equal to one half of its maximum, then, from equation (18.1.1) the nominal value of v_b is

$$v_{bnom} = 12 - \left[\frac{12 + 1 - 0.7}{54} + 0.007 \right] 41$$

$$= 2.36V \qquad ---- \qquad (18.1.3)$$

To obtain the required nominal output current of 5 mA, the nominal value of R_7 is thus

$$R_{7nom} = \frac{E_{cnom} + v_{bnom} - v_{be4}}{i_{c4}} = \frac{12 + 2.36 - 0.7}{5}$$

$$= 2.73 \text{ kohm} \qquad ---- \qquad (18.1.4)$$

A value R_7 = 2.7 kohm is therefore specified.

The maximum value of v_b will occur when E_b = 13V, E_c = 12.4V and i_{b4} = 0, and with R_8 and R_C at their highest and lowest values, respectively. Substitution for this condition in equation (18.1.1) gives

$$v_{bmax} = 13 - \left[\frac{12.4 + 1 - 0.7}{55} \right] 40.2 = 3.7V$$

--- (18.1.5)

Thereis thus no possibility of saturation of the transistors TR3 and TR4.

The output voltage amplitude is

$$v_o = i_{c4} R_6 = \left[\frac{E_c + v_b - v_{be4}}{R_7} \right] R_6 \quad \text{----} \quad (18.1.6)$$

The lowest value of output voltage amplitude will occur under conditions similar to those for v_{bmin}, and with R_7 at its highest, and R_6 its lowest, value. From (18.1.6) the amplitude will then be

$$v_{omin} = \frac{11.6 + 1 - 0.7}{2.75} 1.18 = 5.11V \quad -- \quad (18.1.7)$$

The multivibrators which are triggered by the comparator have therefore been designed to operate from this minimum value of output voltage.

18.2 Voltage Comparator Gain

Having chosen the resistor values to obtain satisfactory d.c. conditions in the comparator, an estimate must be made of the voltage gain. As it is necessary only to ensure that the gain exceeds the value of 500 arrived at in Sec. 18.1, an accurate calculation is not required, and a simple method of determining the gain will suffice; a detailed equivalent-circuit analysis of the comparator will not be attempted.

As in Sec. 18.1, the condition of equal currents in transistors TR3 and TR4 will be assumed. Then, since the base potentials of the transistors are nearly equal, it will also be assumed that the currents in TR1 and TR2 are equal. This is the condition of maximum small-signal voltage gain of the comparator.

Consider the transistor pair TR3-TR4. The application of a small change in input voltage v_i will cause changes in v_{b3} and v_{b4}, which may be assumed equal and opposite: this assumption will be justified later in this Section. Since the transistors are operating in the linear mode, there will be no change in the total current $(i_{e3} + i_{e4})$, and the potential of the emitters will thus

remain constant. Each of these transistors may, therefore, be regarded as a simple common-emitter amplifier. Considering TR4 in this way, the common-emitter input resistance r_{be4}, as given in the manufacturer's data, is within the range 1.8 kohm to 12 kohm, when the d.c. emitter current I_e = 2.5 mA. Taking the 1.8 kohm value as "worst case", the effective collector load R_L of TR2 is then

$$R_L = \frac{R_B r_{be4}}{R_B + r_{be4}} = \frac{1.8 \times 41}{1.8 + 41} = 1.73 \text{ kohm} \quad \text{-(18.2.1)}$$

A change Δi_{c2} in collector current of TR2 will therefore result in a change Δi_{b4} of

$$\Delta i_{b4} = \frac{R_B}{R_B + R_L} \Delta i_{c2} \quad \text{----} \quad (18.2.2)$$

causing a change in output current from TR4 of

$$\Delta i_{c4} = \beta \Delta i_{b4} = \frac{\beta R_B}{R_B + R_L} \Delta i_{c2} \text{ ---} \quad (18.2.3)$$

Where β is the small-signal current gain of TR4. After a reduction for ambient temperature and ageing, as described in Sec. 18.1, a worst-case value of 100 will be taken. Substituting values in equation (18.2.3),

$$\frac{\Delta i_{c4}}{\Delta i_{c2}} = \frac{100 \times 41}{41 + 1.73} = 95.9 \text{ ----} \quad (18.2.4)$$

In the case of the transistor pair TR1-TR2, a change in input voltage Δv_i will cause a corresponding change Δv_{b1} in base voltage of TR1, v_{b2} remaining constant. These unbalanced base voltages may be regarded as the superposition of two components. The first "differential" component consists of equal and opposite voltages, of magnitude $\Delta v_{b1/2}$, applied to TR1 and TR2 base terminals: the second "common mode" component consists of

equal voltages of magnitude $\Delta v_{b1}/2$, and of similar polarity, applied to both base terminals. As linear operation has been assumed, the effect of these components of input voltage on i_{c1} and i_{c2} may be determined separately, and the results added, to obtain the total effect of the input voltage change Δv_i.

The "differential" component of base input voltages will cause equal and opposite changes in collector currents i_{c1} and i_{c2} : i_{R8} will therefore remain constant and, by the reasoning used for TR3-TR4, each of the transistors TR1 and TR2 may be regarded as a common-emitter amplifier. Considering TR1 in this way, the change $\Delta v_{b1}/2$ in base-emitter voltage will cause a change in base current of

$$\Delta i_{b1} = \Delta v_{b1}/2r_{be1} \qquad \text{-----} \qquad (18.2.5)$$

where r_{be1} is the common-emitter input resistance.

Now, the change in input voltage will be

$$\Delta v_1 = \Delta v_{b1} + \Delta i_{b1} R_1 \qquad \text{-----} \qquad (18.2.6)$$

Substituting (18.2.5) in (18.2.6),

$$\Delta v_i = (2r_{be1} + R_1)\Delta i_{b1} \qquad \text{-----} \qquad (18.2.7)$$

Thus the voltage gain is

$$\frac{\Delta v_o}{\Delta v_i} = \frac{\Delta i_{c4} R_C}{\Delta v_i} = \frac{\beta \Delta i_{b1}}{\Delta v_i} \cdot \frac{\Delta i_{c4}}{\Delta i_{c2}} \cdot R_C = \frac{\beta R_C}{(2r_{be1} + R_1)} \cdot \frac{\Delta i_{c4}}{\Delta i_{c2}}$$

$$\text{-----} \qquad (18.2.8)$$

From the manufacturer's data, r_{be1}, for a d.c. emitter current of 0.23 mA, is within the range 7-48 kohm. Taking the lowest value as "worst-cast", and using equation (18.2.4), substitution of numerical values in (18.2.8) gives

$$\frac{\Delta v_o}{\Delta v_1} = \frac{100 \times 1.2}{(14 + 10)} 95.9 = 480 \quad \text{---} \quad (18.2.9)$$

The "common-mode" component of base voltages will cause a rise in the potential of the common emitters of TR1-TR2 of approximately $\Delta v_{b1}/2$. The resulting increase $\Delta i_{R8} = \Delta v_{b1}/2R_8$ in current in R_8 will divide equally between TR1 and TR2, as equal conduction in these transistors has been assumed. There will thus be an equal reduction Δv_b in both v_{b3} and v_{b4}, with a corresponding reduction in v_{e4} : the change in output voltage will then be

$$\Delta v_o = R_C \Delta i_{c4} = \frac{R_C \Delta v_{e4}}{2R_7} = \frac{R_C \Delta v_b}{2R_7} = \frac{R_L R_C \Delta i_{R8}}{4R_7}$$

$$= \frac{R_L R_C}{8R_7 R_8} \Delta v_{b1} \quad \text{-----} \quad (18.2.10)$$

Substituting values from (18.2.1) and Sec. 18.1, the "common-mode" voltage gain is

$$\frac{\Delta v_o}{\Delta v_{b1}} = \frac{1.73 \times 1.2}{8 \times 2.7 \times 27} = 0.0036 \quad \text{---} \quad (18.2.11)$$

This component of the voltage gain is so small that it will be neglected : thus the only significant component of base voltages of the transistors TR3 and TR4 is that causing equal and opposite voltage increments, and this justifies the assumption to that effect made earlier in this Section.

The voltage gain of the comparator is therefore as given by equation (18.2.9). The value of 480 calculated for "worst-case" conditions is almost twice the minimum value specified in Sec. 18.1, and would thus appear to be adequate.

18.3 Voltage comparator error

The d.c. voltage V_2 (Fig. 39) is selected, during manufacture of the equipment, to cause operation of the comparator when the input voltage v_i reaches the value V_{ref}. Subsequent variations in this value may occur, due to variations in ambient temperature, supply voltages, or due to ageing of the components. A primary cause of variations in V_{ref} will, of course, be variations in the voltage V_2 : this is derived from a Zener reference diode, the choice of which is dictated mainly by economics. It is possible to obtain Zener diodes having a stability reputed to equal that of a Standard Cell; however, a less expensive type has been used, for which the makers guarantee a voltage stability of $\pm$ 1% over a temperature range -50^{o} to $+100^{o}$ C. This is equivalent to a tolerance of $\pm$ 10 mV in V_{ref}, corresponding to 0.012 degree in phase angle (Equation 13.1.3). For the remainder of the components, the effect of possible variations in the characteristics of the transistors far outweighs that of the other components, which latter will therefore be neglected. Silicon transistors having negligible leakage currents are used; the effect of variation of leakage current with temperature will therefore not be considered.

Consider the comparator operating in the condition described in the previous Sections, when the transistors TR3 and TR4 are equally conducting. From Fig. 39, for the transistor pair TR1-TR2 we have

$$v_i - V_2 = i_{b1}R_1 - i_{b2}R_2 + v_{be1} - v_{be2} \text{ ----- (18.3.1)}$$

Putting $R_1 = R_2 = R_A$, this becomes

$$v_1 - V_2 = (i_{b1} - i_{b2})R_A + (v_{be1} - v_{be2}) \text{ -- (18.3.2)}$$

For a constant value of V_2, the variations in the value of v_i required to maintain this condition have two main causes, as shown by the two terms on the right-hand side of (18.3.2). The first cause is the variation in base-emitter voltage of the transistors, affecting the term $(v_{be1} - v_{be2})$. For a given emitter current, the base-emitter voltage of a transistor with constant emitter current varies with junction temperature at approximately 2 mV/deg. C.[33] It is important, therefore, to ensure that a large differential change in junction temperature between the transistors of a pair does not occur. One of the causes of such a change is the operation of the transistors at a temperature considerably above ambient : variations in ventilation can then unequally affect their temperatures; this is one of the reasons for the low values of current and voltage chosen for TR1 and TR2. The differential change in temperature between the transistors in a pair can be reduced by mounting them on a common block of material having a high thermal conductivity; a still greater improvement may be obtained by fabrication of the transistors on a common silicon chip. None of these methods was found to be necessary, however, as, with negligible power dissipation in TR1 and TR2, and by mounting the transistors close together on the circuit board, a differential temperature variation exceeding 4 deg. C was thought to be most unlikely : this variation would cause an error in V_{ref} of $\pm$ 8 mV, giving a phase angle error less than 0.01 degree at 50 Hz. Differential variations in the junction temperature of the transistors TR3 and TR4 will cause a change in $(v_{b3} - v_{be4})$, which will also cause a change in v_i : however, the magnitude of this change in v_i will be negligible, due to the effect of the voltage gain of the transistor pair TR1-TR2.

The second cause of variation in the value of v_i is shown in the term $(i_{b1} - i_{b2})R_A$ in (18.3.2). With TR1 and TR2 conducting equally, the base current of each transistor will be approximately $(V_2 + E_c - v_{be})/2\bar{\beta}R_8$. A minimum value of current gain $\bar{\beta} = 175$, at 25°C and collector current 0.1 mA, is guaranteed in the manufacturer's data for the transistor; applying a reduction of 30% for the effects of ambient temperature and ageing, as described in Sec. 18.1, this falls to $\bar{\beta}_{min} = 122$. The maximum value of voltage drop across R_1 or R_2 will thus be

$$\frac{R_1(V_2 + E_c - v_{be})}{2\beta_{min}R_8} = \frac{10(1 + 12 - 0.7}{2 \times 122 \times 27} = 0.0187 \text{ volts} \quad (18.3.3)$$

Assuming a "worst-case" condition where TR1 and TR2 have current gains of $\bar{\beta}_{min}$ and infinity, respectively, and taking a variation in $\bar{\beta}$ of 30% for ambient temperature and ageing effects, then the maximum change in v_i will be $0.3 \times 18.7 = 5.6$ mV.

Adding together the possible changes in v_i due to both causes described above, the total change is $(2 \times 8) + 5.6 = 21.6$ mV, i.e., a possible error of $\pm$ 10.8 mV from the nominal value of V_{ref}. Comparing this with the 85 mV given by equation (13.1.3) as required to cause a 0.1° error in phase angle indication, it would appear that the comparator designed has an adequate performance.

18.4 Voltage comparator tests

Both long-term and short-term tests were carried out on the voltage comparator, connected as VCA in Fig. 38. The transformer winding A_1 was replaced by a d.c. voltage source v_i the magnitude of which was variable, and accurately measured using a digital voltmeter. This input voltage v_i was varied until the output voltage across R_9 was in the centre of its dynamic range.

The value of v_i was then noted.

The long-term test consisted of measuring v_i, under the above conditions, for both comparators VCA and VCB in the F. T. M. Control Centre unit, after it had been in service for a period exceeding 12 months. No significant variation from the value of v_i to which the comparators had been initially adjusted was found.

The short-term tests consisted in measurement of v_i under the conditions given above, for a comparator similar in mechanical construction to those used in the Control Centre unit, and mounted in an environmental test chamber. The ambient temperature was varied in 10 degree steps from $0^{\circ}C$ to $50^{\circ}C$, i.e. over a range 10 degrees hotter and 10 degrees cooler than the specification demanded. At each temperature the value of v_i was measured, for supply voltages of nominal and extreme tolerance values. The results are given in Table 9, which also shows the voltage V_z across the Zener diode D1 for each of the test conditions. It will be seen that over the prescribed temperature range of 10° to $40^{\circ}C$, the maximum variation in v_i for worst-case extremes of supply voltage is 1.0021 - 0.9878 = 0.0143 volt, most of which is accounted for by changes in Zener diode voltage.

A further test was made to determine the voltage gain. With the supply voltages at their nominal values of 12V, and with an ambient temperature of $20^{\circ}C$, the input voltage was varied in steps, and the corresponding output voltage between TR3 collector (Fig. 38) and earth measured for each value of input voltage. The results are shown in Fig. 40. The voltage gain is given by the slope of the graph, which, evaluated at its mid-point, is 1233.

It is concluded that these results give satisfactory support to the calculations given in the previous Sections, and confirm the adequacy of the voltage comparator performance.

19.1 MULTIVIBRATOR DESIGN

Multivibrators operating in astable, monostable and bistable modes are used in the equipment. The monostable multivibrator is the most general of the three types, and its design contains virtually all of the considerations required for the astable and bistable multivibrators. A detailed design of only the monostable type will therefore be given.

The circuit is shown in Fig. 41, and waveforms of voltage, measured with respect to earth, in Fig. 42. The input triggering voltage is shown at (a), while base and collector voltages for the transistors TR2 and TR1 are shown at (b) and (d), and (e) and (f), respectively. The purpose of the components D4, R_4 and R_6 is to make the multivibrator resistant to false triggering by noise voltages : their action is explained in Sec. 19.3.

In the quiescent state of the multivibrator, base current flowing via R and D2 causes TR2 to saturate : by suitable choice of the values of R_1 and R_2, the resulting low collector voltage of TR2 causes the base-emitter junction of TR1 to be reverse-biassed, and this transistor is therefore held in the "off" state. On receipt of a negative-going step of input trigger voltage v_t, the base of transistor TR2 is driven negative; this transistor is then in the "off" state, and the resulting rise in collector voltage v_{c2} causes a flow of base current in TR1 sufficient to cause saturation. The multivibrator is then in its "quasi-stable" state. The fall in collector voltage v_{c1} which accompanies the conduction of TR1 is transmitted via the capacitor C to the point P, Fig. 41, and (c) in Fig. 42. Since this voltage fall has an amplitude greater than the permissible reverse base-emitter voltage rating of the transistors, it is applied to the base of TR2 via the diode D2, which becomes reverse-biassed; the maximum negative value of v_{b2} is then limited

by the diode D3. The potential at the point P now rises at a rate determined by the values of R and C, due to current flowing in R, into C, and thence into the collector terminal of TR1. After a time T, the "period" of the multivibrator, the potential of P has risen to the point where sufficient conduction in TR2 occurs to cause regenerative action between the transistors. TR1 then turns "off" and TR2 becomes heavily saturated, due to the current recharging C via R_L, added to the current in R, flowing into the base of TR2. After a "recovery" time t_r, during which C becomes fully recharged, the multivibrator returns to its quiescent state, in readiness for the next trigger pulse. Pulses of output voltage, of duration T, may be taken from the collector terminals of either of the transistors TR1 or TR2, giving negative-going and positive-going pulses, respectively.

In the design of this multivibrator, the main choice to be made is in the type of transistors, and the saturation collector current $I_{c(sat)}$ at which they will operate. On grounds of reliability, silicon planar transistors were chosen. The optimum value of $I_{c(sat)}$ is not critical; it lies within a range having a lower limit determined by the maximum load to be imposed on the output of the multivibrator, and an upper limit beyond which excessive heating and power consumption will occur. A further factor affects the choice : as the current $I_{c(sat)}$ is increased, the value of R (Fig. 41) must be reduced; thus for a given period T, the required value of capacitor C will increase, and this may result in an inconveniently large capacitor in multivibrators designed to generate long-duration pulses. On the other hand, in multivibrators for short-pulse operation, the use of a large $I_{c(sat)}$ may avoid the necessity of an inconveniently small value of C. Based on these considerations, the transistor type 2N914 was chosen, operating at a saturation collector current of approximately 10 mA.

The nearest preferred value of collector load resistor is thus R_L = 1.2 kohm, giving a nominal collector current of

$$I_{c(sat)} = \frac{E_b - V_{ce(sat)}}{R_L} = \frac{12 - 0.25}{1.2} = 9.8 \text{ mA nominal} \qquad \text{-----} \quad (19.1.1)$$

The value of R_3 is not critical. Its function is merely to cause sufficient current to flow in D3, during the quasi-stable state of the multivibrator, to ensure that TR2 remains "off". A value R_3 = 100 kohm was therefore chosen, giving a current in D3 of

$$i_{D3} = \frac{E_c - V_{D3}}{R_3} = \frac{12 - 0.6}{100} = 0.114 \text{ mA nominal} \qquad \text{-----} \quad (19.1.2)$$

The value of R must be such that under worst-case conditions, TR2 is aways saturated when the multivibrator is in the quiescent state. Now as the current in R_7 is zero,

$$i_R = i_{b2} + i_{R3} \qquad \text{-----} \quad (19.1.3)$$

i.e.,

$$\frac{E_b - V_{D2} - V_{be(sat)}}{R} = \frac{I_{c(sat)}}{\bar{\beta}} + \frac{E_c + V_{be(sat)}}{R_3} \qquad \text{-----} \quad (19.1.4)$$

For the transistor type 2N914, the manufacturer's data gives a minimum common-emitter d.c. current gain of 30, at 25°C and with I_c = 10 mA. Applying the 30% reduction for lower temperature operation and ageing, as described in Sec. 18.1, gives $\bar{\beta}_{min}$ = 21. The resistors will be assumed to be within 5% of their nominal values. Then, taking the worst-case values as

$E_b = 11V$, $E_c = 11.6V$, $v_{D2} = V_{be(sat)} = 0.8V$,

$V_{ce(sat)} = 0V$, $I_{c(sat)} = E_b/R_{Lmin} = 11/1.14 = 9.65$ mA,

$R_3 = 95$ kohm,

and substituting these in (19.1.4), we get

$$\frac{11 - 0.8 - 0.8}{R} = \frac{9.65}{21} + \frac{11.6 + 0.8}{95}$$

giving

$$R_{max} = 15.9 \text{ kohm} \qquad \text{-----} \qquad (19.1.5)$$

Thus the nominal value of R is 15.9 - 5% = 15.1 kohm. A 15 kohm resistor has therefore been specified.

The period of the multivibrator is the time T during which TR2 is "off". Referring to Fig. 42, after the application of the negative-going step of v_t the collector voltage v_{c1} falls by an amount $E_b - v_{D4} - I_{coo}R_L - V_{ce(sat)}$, where I_{coo} is the collector leakage current of TR1 in the "off" state: using silicon transistors, $I_{coo}R_L << E_b$, and the former term will henceforth be neglected. The fall in v_{c1} causes the potential at the point P to fall to $-v_x$, where

$$v_x = E_b - v_{D4} - V_{ce(sat)} - V_{be(sat)} - v_{D2} \qquad \text{---} \quad (19.1.6)$$

Neglecting the leakage current of the reverse-biassed silicon diode D2, the rise of v_P occurs in two stages. The first stage, of duration (1 - k)T, where k is a constant, is an exponential rise towards an aiming potential E_b. The time constant is $C(R + r_{o1})$, where r_{o1} is the collector-emitter saturation resistance of TR1: as $r_{o1} << R$, this time constant will be taken as CR. The rise in v_P continues until it has reached a value such that v_{b2} is approximately zero; the diode D3 then no longer conducts, and the current in R_3 is supplied, via D2, from i_R. As v_P will then be approxi-

mately v_{D2}, we can write

$$(E_b - v_{D2}) = (E_b + v_x)\varepsilon^{-(1 - k)T/CR} \quad \text{----} \quad (19.1.7)$$

which, on substituting (19.1.6) and rearranging terms, gives

$$(1 - k)T = CR\log \frac{2E_b - v_{D4} - V_{ce(sat)} - V_{be(sat)} - v_{D2}}{E_b - v_{D2}} \quad \text{----} \quad (19.1.8)$$

The second stage of the rise in v_P now commences; the rise is exponential, with a time constant CR', where

$$R' = \frac{RR_3}{R + R_3} , \quad \text{----} \quad (19.1.9)$$

towards an aiming potential E', where

$$E' = \frac{E_b R_3 - (E_c - v_{D2})R}{R + R_3} \quad \text{----} \quad (19.1.10)$$

After a time kT in the second stage, v_P rises to a value v_{PR} sufficient to cause TR2 to conduct and initiate the regenerative action between the transistors. This value v_{PR} is less than $V_{be(sat)} + v_{D2}$ by a small fraction of a volt; for the purpose of determining the period of the multivibrator they may be assumed equal, with negligible error in the period calculated. We may then write

$$E' - V_{be(sat)} - v_{D2} = (E' - v_{D2})\varepsilon^{-kT/CR'} \quad \text{--} \quad (19.1.11)$$

giving

$$kT = CR'\log \frac{(E' - v_{D2})}{\left[E' - V_{be(sat)} - v_{D2}\right]} \quad \text{----} \quad (19.1.12)$$

Taking the nominal values $E_b = E_c = 12V$, $V_{ce(sat)} = 0.25V$ $V_{be(sat)} = v_{D2} = v_{D4} = 0.7V$, $R = 15$ kohm, $R_3 = 100$ kohm, and substituting these values in (19.1.8) we have

$$(1 - k)T = 15000C\log\left[\frac{(2x12) - 0.7 - 0.25 - 0.7 - 0.7}{12 - 0.7}\right]$$

$$(1 - k)T = 9750C \qquad \text{-----} \qquad (19.1.13)$$

Substituting the nominal values in (19.1.10) gives

$$E' = \frac{(12x100) - (12 - 0.7)15}{15 + 100} = 8.95V \text{ ---} \qquad (19.1.14)$$

$$R' = \frac{(15 \times 100)}{(15 + 100)} \cdot 10^3 = 13130 \qquad \text{-----} \qquad (19.1.15)$$

Substituting (19.1.14) and (19.1.15) in (19.1.12) gives

$$kT = 13130C\log\frac{(8.95 - 0.7)}{(8.95 - 0.7 - 0.7)} = 1160C$$

$$\text{-----} \qquad (19.1.16)$$

From (19.1.13) and (19.1.16), the total period is therefore

$$T = (9750 + 1160)C = 10910C \qquad \text{-----} \qquad (19.1.17)$$

This expression has been used to calculate the values of C used in the multivibrators M1-M4 in Fig. 38, to give the periods specified in Sec. 15.1.

The values of R_1 and R_2 will now be determined. They have to satisfy two conditions : the first condition is that when TR2 is saturated, the base voltage of TR1 shall be negative, thus ensuring the "off" condition of that transistor. The amplitude of this negative voltage should lie within a range having an upper value limited by the base-emitter reverse voltage breakdown rating of the transistor : the lower limit value must be large enough to ensure collector-current cut-off in the transistor under worst-case conditions of ambient temperature and supply voltages. Limit values of 2V and 0.5V, respectively, were taken. The second condition is that when TR2 is "off", sufficient base current shall

flow in TR1 to ensure saturation; too high a base current will, however, cause excessive charge storage in the transistor. There are an infinite number of pairs of values of R_1 and R_2 which will satisfy the above conditions; they are not, however, all of equal merit. There is a pair of values which, while satisfying the required conditions, will also permit the maximum variation from the nominal value of each resistor. A method of determining such a pair of values is described below.

In Fig. 41, consider TR2 to be saturated : TR1 will then be "off". A small reverse base current will flow in TR1; for the present this will be neglected. The base of TR1 will be at a potential $-V_{br}$ to earth, where

$$V_{br} = \frac{R_1 E_c - R_2 V_{ce(sat)}}{R_1 + R_2} \qquad \text{-----} \qquad (19.1.18)$$

Rearranging terms, in (19.1.18), then for any given value of R_2, the value of R_1 required to provide a given V_{br} will be

$$R_1 = \frac{(V_{ce(sat)} + V_{br})R_2}{E_c - V_{br}} \qquad \text{-----} \qquad (19.1.19)$$

Now consider the conditions when TR2 is "off". A forward base current I_{bf} will flow in TR1, resulting in a base voltage $v_{b1} = V_{be(sat)}$. Then

$$I_{bf} = \frac{E_b - I_{coo} R_L - V_{be(sat)}}{R_1 + R_L} - \frac{E_c + V_{be(sat)}}{R_2}$$

$$\text{-----} \qquad (19.1.20)$$

Thus, from (19.1.20), for a given value of R_2, the value of R_1 required to provide a given I_{bf} will be

$$R_1 = \frac{(E_b - I_{coo}R_L - V_{be(sat)})R_2}{E_c + V_{be(sat)} + I_{bf}R_2} - R_L \quad \text{---- (19.1.21)}$$

Fig. 43 shows the value of R_1, calculated from (19.1.19), plotted against R_2; the two graphs (a) and (b) are drawn for the limit conditions V_{br} = 0.5V and 2V respectively. Graphs of R_1 plotted against R_2, calculated from (19.1.21), are also shown, for the limit conditions $I_{bfmin} = I_{c(sat)max}/\bar{\beta}_{min} = E_b/R_{Lmin}\bar{\beta}_{min}$ = 12/1.14 x 21 = 0.5 mA, (graph c) and I_{bf} = 1 mA, (graph d). The following values were used in the calculations from which the graphs were plotted : $V_{ce(sat)}$ = 0.25V, $V_{be(sat)}$ = 0.7V, $E_b = E_c$ = 12V, R_L = 1.26 kohm. The term $I_{coo}R_L$ has been neglected, as $I_{coo}R_L << E_b$.

To satisfy the "off" condition of TR1, R_1 and R_2 must have values corresponding to a point lying between the lines (a) and (b) in Fig. 43. To simultaneously satisfy the "on" condition, this point must also lie between the curves (c) and (d). Hence, it is a simple matter to select, by inspection, a point such as Q, representing preferred resistance values, and to inscribe a rectangle representing a given tolerance on the resistance values. The dotted rectangle shown in Fig. 43 is drawn for a tolerance of $\pm$ 20% on the values of R_1 and R_2. The multivibrators in the equipment were designed with values for R_1 and R_2 represented by the point Q, i.e., R_1 = 12 kohm, R_2 = 100 kohm.

In the preceding analysis, the reverse base current of TR1 in the "off" condition has been neglected. The effect of this current will be to raise the base potential by an amount $I_{br}R_1R_2/(R_1 + R_2)$, where I_{br} is the reverse base current,

Using silicon transistors, this represents a negligible increase in the base potential.

19.2 Multivibrator Triggering

Consider the multivibrator shown in Fig. 41, when triggered by a step voltage v_t of amplitude E_t. Before the trigger pulse is applied, $v_{b2} = V_{be(sat)}$, and the voltage across R_5 is $V_{R5} = E_b R_5/(R_5 + R_6)$. When v_t falls by E_t, the diodes D_1 and D_3 conduct, and the voltage across R_7 is then

$$V_{R7} = E_t - V_{R5} - v_{D1} - V_{be(sat)} - v_{D3} \qquad \text{-----} \qquad (19.2.1)$$

causing a current in R_7 of $i_{R7} = v_{R7}/R_7$. Part of this current flows in D2, and the remainder in D3. Assuming the diode voltages v_{D1} and v_{D3} to be constant, the current i_{R7} will then decay exponentially with a time constant $C_t R_7$. For proper triggering, it is essential that the base current i_{b2} be reduced to zero for the time t_t required for the multivibrator to establish its regenerative action, i.e., $i_{R7} \geq i_{D2}$ during this time. Here, t_t is defined as the time between the application of v_t and the instant when the diode D2 becomes reverse-biassed, due to the fall in potential at point P. (Fig. 41). It is to prolong the triggering current that the resistor R_7 is used. With R_7 of zero value, the capacitor C_t is charged by v_t so quickly that i_{R7} is a large-amplitude pulse with a duration that may be less than t_t, and experiments have amply confirmed the resulting unreliability of triggering of the multivibrator under these conditions. With R_7 at too high a value, insufficient current i_{R7} flows, and triggering is again uncertain. There is therefore an optimum value of R_7, and an evaluation of this will now be made.

At a time t_t after the negative-going step in v_t then, for the present, neglecting the effect of R_5 and R_6, the current i_{R7} will be

$$i_{R7} = \frac{V_{R7}}{R_7} \varepsilon^{\frac{-t_t}{C_t R_7}} \qquad \text{-----} \qquad (19.2.2)$$

where V_{R7} is defined in equation (19.2.1). If R_7 is varied, while V_{R7} and C are kept constant, this current will be a maximum when

$$\frac{di_{R7}}{dR_7} = \frac{v_{R7}}{R_7^2} \varepsilon^{\frac{-t_t}{C_t R_7}} \left[\frac{t_t}{C_t R_7} - 1 \right] = 0$$

$$\text{-----} \qquad (19.2.3)$$

corresponding to the condition

$$C_t R_7 = t_t \qquad \text{-----} \qquad (19.2.4)$$

When this condition is satisfied, then after a time t_t from the application of the trigger pulse, the amplitude of i_{R7} will have fallen to $1/\varepsilon$ of its initial value. A necessary condition is therefore

$$\frac{V_{R7}}{R_7} = \varepsilon i_{D2} \qquad \text{-----} \qquad (19.2.5)$$

or, substituting from equation (19.2.1)

$$R_7 = \frac{E_t - V_{R5} - v_{D1} - V_{be(sat)} - v_{D3}}{\varepsilon i_{D2}}$$

$$\text{-----} \qquad (19.2.6)$$

The required value of C_t is thus, from (19.2.4),

$$C_t = \frac{t_t}{R_7} \qquad \text{-----} \qquad (19.2.7)$$

using the value of R_7 calculated from (19.2.6).

This indicates the design procedure for calculating the optimum values of R_7 and C_t. Taking $v_{D1} = v_{D3} = V_{be(sat)} = 0.7V$, $V_{R5} = 2.16V$ (see later), $i_{D2} = E_b/R = 12/15 = 0.8$ mA, and assuming minimum amplitude of trigger pulses of $E_t = 9V$, then, on substituting these values in (19.2.6), we have

$$R_7 = \frac{9 - 2.16 - 0.7 - 0.7 - 0.7}{0.8} = 2.17 \text{ kohm} \qquad \text{-----} \qquad (19.2.8)$$

The value of t_t is difficult to determine accurately. A generous estimate of $t_t = 0.5$ μsec. will therefore be made, in the confidence that this value will be large enough for this type of multivibrator, using silicon planar transistors. Then, from (19.2.7),

$$C_t = \frac{0.5}{10^6 \times 2170} 10^{12} = 230 \text{ pF} \qquad \text{-----} \qquad (19.2.9)$$

Components having values $R_7 = 2.2$ kohm, and $C_t = 270$ pF have therefore been specified.

So far, the effects of R_5 and R_6 have been ignored. The purpose of these resistors is to provide a path for the recharge of C_t after the trigger pulse has terminated; another purpose is to provide, in the quiescent state of the multivibrator, a reverse bias voltage across D1 to avoid false triggering by noise voltages (see Sec. 19.3). The capacitor C_t will be virtually fully recharged in a time $5C_tR_5R_6/(R_5 + R_6)$ after the termination of the trigger pulse. Since there is no requirement for rapid retriggering of any of the multivibrators used in this equipment, the absolute values of these resistors is not critical, so long as their ratio satisfies the noise immunity requirements: values of $R_5 = 33$ kohm and $R_6 = 100$ kohm have been chosen, giving $V_{R5} = 33 \times 12/(33 + 100) = 2.16V$, the value used in (19.2.8). By the use of these high

values of resistance, their effect on the calculations made earlier in this Section is negligible.

In the case of the bistable multivibrator, e.g., B22 in Fig. 38, the diodes D60 and D61 are included to prevent excessive reverse base-emitter voltage being applied to the transistors TR35 and TR36 by the trigger pulses. Although the duration of these pulses is so short that they cannot cause appreciable heating in the transistor, the existence of even momentary repetitive reverse-voltage breakdown of the base-emitter junction is known (34, 35) to reduce the life of a transistor.

19.3 Multivibrator Noise Immunity

A problem in the design of multivibrators is to prevent their being falsely triggered by noise voltages. There are two main points of entry for the noise voltage : the first is via the normal triggering circuit C_t, D1 and R_7 in Fig. 41, the noise voltage being induced in the connections to the source of trigger pulses. The second point of entry is from the supply voltage E_b; even with the generous use of decoupling capacitors connected between E_b and earth, it is difficult to prevent voltage transients generated by neighbouring circuits, or transmitted by the power supply, reaching the multivibrator. By careful physical layout of the various circuits relative to each other, the amplitude of the noise voltages can be minimized;[39] however, it is also desirable that the multivibrator should, as far as is possible, be designed to be insensitive to the noise.

The sensitivity to false triggering by noise voltages induced in the trigger pulse circuit can be reduced very simply, by arranging that in the quiescent state, the diode D1 (Fig. 41) is reversed-biassed. The bias voltage is obtained from the direct current flowing in R_6. An increase in the bias improves the resistance of the multivibrator to noise, but also increases the amplitude of trigger pulses required. As all of the multi-vibrators used in this equipment are triggered from circuits

giving a substantial trigger-pulse amplitude, a bias of approximately 2V has been used, providing adequate protection against noise induced in this way.

For noise voltages superimposed on the supply voltage E_b, the bistable multivibrator is inherently insensitive. Consider B22, Fig. 38, and assume that the transistor TR35 is "off", and TR36 "on". The base current of TR36 is

$$i_{b36} = \frac{E_b - V_{be(sat)}}{R_{134} + R_{138}} - \frac{E_c + V_{be(sat)}}{R_{142}} \quad \text{----} \quad (19.3.1)$$

Neglecting the current in R_{137}, the collector current of TR36 is

$$i_{c(sat)36} = \frac{E_c - V_{ce(sat)}}{R_{136}} \quad \text{----} \quad (19.3.2)$$

For saturation in TR36 we must have

$$i_{b36} \geq \frac{i_{c(sat)36}}{\bar{\beta}} \quad \text{----} \quad (19.3.3)$$

i.e., from (19.3.1) and (19.3.2),

$$\frac{E_b - V_{be(sat)}}{R_{134} + R_{138}} - \frac{E_c + V_{be(sat)}}{R_{142}} \geq \frac{E_b - V_{ce(sat)}}{\bar{\beta} R_{136}} \quad \text{----} \quad (19.3.4)$$

Rearranging terms, then for a given $\bar{\beta}$, the minimum value of E_b to ensure saturation of TR36 is

$$E_b \geq \frac{\frac{E_c + V_{be(sat)}}{R_{142}} + \frac{V_{be(sat)}}{R_{134} + R_{138}} - \frac{V_{ce(sat)}}{\bar{\beta} R_{136}}}{\frac{1}{R_{134} + R_{138}} - \frac{1}{\bar{\beta} R_{136}}} \quad \text{----} \quad (19.3.5)$$

Substituting nominal values of $R_{134} = R_{136} = 1.2$ kohm, $R_{138} = 12$ kohm, $R_{142} = 100$ kohm, $V_{be(sat)} = 0.7V$, $V_{ce(sat)} = 0.25V$, $E_c = 12V$, $\bar{\beta} = 21$, we get

$$E_b \geq \frac{\frac{(12 + 0.7)}{100} + \frac{0.7}{(12 + 1.2)} - \frac{0.25}{(21 \times 1.2)}}{\frac{1}{(12 + 1.2)} - \frac{1}{(21 \times 1.2)}} = 4.7V$$

----- (19.3.6)

For all values of E_b above 4.7V, therefore, the transistor will remain in saturation; false triggering of the bistable multivibrator from supply-borne noise is thus unlikely to occur.

The monostable multivibrator is far more susceptible to noise pulses on E_b. Referring to Fig. 41, assume that R_4 is omitted, and D4 replaced by a direct connection. In the quiescent state,

$$i_{b2} = i_{D2} - i_{R3} = \frac{E_b - v_{D2} - V_{be(sat)}}{R} - \frac{E_c + V_{be(sat)}}{R_3}$$

----- (19.3.7)

Now suppose a negative-going step of voltage ΔE_b be superimposed on the supply voltage E_b. There will be no immediate change in the charge on C so, assuming that D2 remains in conduction, the voltage step will be impressed on R_L, causing a step of current in C of

$$\Delta i_c = \frac{\Delta E_b}{R_L} \qquad \text{----- (19.3.8)}$$

The total current in D2 will then be

$$i_{D2} = \frac{E_b - \Delta E_b - v_{D2} - V_{be(sat)}}{R} - \frac{\Delta E_b}{R_L}$$

----- (19.3.9)

Due to the current represented by the second term, the effect of a small step ΔE_b can well be sufficient to cause i_{b2} to fall below the value required to maintain saturation in TR2. For example, we will calculate the magnitude of ΔE_b required to cause i_{D2} to be reduced to one-half of its nominal value; this reduction would be sufficient to cause triggering if the current gain of transistor TR2 were near the lower limit of its permissible range of values. From (19.3.9) and (19.3.7),

$$\frac{E_b - \Delta E_b - v_{D2} - V_{be(sat)}}{R} - \frac{\Delta E_b}{R_L} = \frac{E_b - v_{D2} - V_{be(sat)}}{2R}$$

----- (19.3.10)

giving

$$\Delta E_b = \frac{(E_b - v_{D2} - V_{be(sat)})RR_L}{2R(R + R_L)}$$ ----- (19.3.11)

Using the nominal values calculated in Sec. 19.1,

$$\Delta E_b = \frac{(12 - 0.7 - 0.7)(15 \times 1.2)}{(2 \times 15)(15 + 1.2)} = 0.39V$$

----- (19.3.12)

It is not uncommon for noise voltage pulses of this magnitude to occur on the d.c. supply voltage lines of pulse equipment.

For a positive-going noise pulse superimposed on E_b, the capacitor C charges through R_L, D2 and the base-emitter junction of TR2; the resulting current has a direction such as to add to the

forward base current of TR2, which thus remains in saturation. On termination of the noise pulse, however, the excess charge acquired by C during the pulse then discharges through D2, and the resulting current then reduces i_{D2}, with the same consequences as for a negative step in E_b.

Thus, the monostable multivibrator in its basic form compares unfavourably with the bistable multivibrator in respect of sensitivity to false triggering by noise superimposed on the supply voltage E_b. A considerable improvement can, however, be made, by the inclusion of D4 and R_4 (Fig. 41). The resistor R_4 has a high value, so that in the quiescent state of the multivibrator a small current flows in D4. On receipt of a negative step of noise voltage on E_b, D4 becomes reverse-biassed; negligible current flows in C, and TR2 remains in saturation. With a positive step of noise voltage on E_b, the capacitor C charges through D4, D2 and the base-emitter junction of TR2; the charging current merely adds to the base current of TR2, which therefore remains in saturation. On termination of the noise pulse, the charge accumulated on C causes the collector voltage v_{c1} to be above E_b, and D4 becomes reverse-biassed: C then slowly discharges through R_4 until the diode D4 conducts again. During the time C is discharging, a current of approximately E_b/R_4 flows in C, and in D2: by the use of a high value (270 kohm) for R_4, this current is small and calculable, and cannot bring TR2 out of saturation.

The astable multivibrator is also sensitive to noise pulses superimposed on E_b, and in this case the possibility of false triggering can be reduced by the use of the diode - resistor combination connected in each collector circuit. However, the only astable multivibrator used in the equipment is A (Fig. 38), which operates the warning lights. False triggering of the multivibrator could therefore cause no malfunction of the equipment: the diode - resistor circuits described above have therefore been omitted in this circuit, to avoid the effects of failure of these components.

19.4 Monostable multivibrator test results

For these tests, the circuit shown in Fig. 41 was used, with the components having the values calculated in Sections 19.1 to 19.3. Both short-term and long-term tests were carried out on the multivibrator. For the short-term tests, a multivibrator similar in construction to those used in the equipment was mounted in an environmental test chamber. The ambient temperature was varied over the range 0-50°C, thus exceeding by 20 degrees the range 10-40°C specified for the Control Centre unit. The positive and negative supply voltages were varied over the range 10-14V, this corresponding to a tolerance of twice the amount specified for the power supply units. The effect of these variations on the period of the multivibrator was measured using, as a standard, the 1 MHz pulses from a quartz-crystal controlled oscillator, with visual interpolation using an oscilloscope. It is expected that the error in measurement of the period will not exceed $\pm$ 0.5 μsec.

Fig. 44 shows the period T plotted against ambient temperature, with the supply voltages at their nominal values of $\pm$ 12V. The temperature coefficient of the period, corresponding to the slope of the straight line, is thus 0.027% per degree C.

The stability of period with respect to variations in supply voltages is shown in Fig. 45, the tests being conducted at laboratory temperature. Curve (a) gives the period T plotted against E_b, with E_c = 12V: curve (b) gives the period plotted against E_c, with E_b = 12V. The graphs show that over the specified range of supply voltages, the variation in period is approximately $\pm$ 1%.

The long-term tests used six multivibrators, constructed in the same way as the multivibrator used in the short-term tests. Supply voltages were obtained from two lead-acid car-type batteries: as these were also being used for tests on other apparatus, their

state of charge varied from day to day. The period of the multivibrators was measured at intervals, the supply voltages having previously been adjusted to their nominal values. For a few weeks, measurements were made daily, to ensure that there were no short-term variations in the period. Thereafter, the period was measured at less frequent intervals, and the results of measurements taken over three years are given in Table 10.

Summing up the results of these tests, it is concluded that the monostable multivibrator as designed has a stability of period which is adequate for use in this equipment.

A further test was carried out, to determine the effectiveness of the diode-resistor combination, (D4 and R_4 in Fig. 41), in reducing the susceptibility of the multivibrator to false triggering, caused by noise pulses on the supply voltage E_b. Positive and negative pulses, having variable amplitude and duration, were superimposed on E_b. For a multivibrator constructed without D4 and R_4, a negative or positive pulse of amplitude 0.3V was sufficient to cause triggering, while with D4 and R_4 connected, no triggering was possible by pulses of amplitude up to 6V. It is therefore concluded that the inclusion of these components effects a worth-while improvement in the noise immunity of the multivibrator.

20.1 METER CURRENT GENERATOR DESIGN

This Section is concerned with the design of the meter current generators PCG and NCG in Fig. 1, the purpose of which are explained in Sec. 4.3. The basic circuit used is shown in Fig. 46, while the complete circuit is given in Fig. 38.

The requirement of the current generators is that they shall deliver positive or negative current pulses of defined amplitude to the meter circuit, when the elements M and B (Fig. 1) are in given states. Referring to Fig. 46, the voltage V_z developed across the Zener diode D5, by current flowing in R_7, establishes a reference potential for the base of the current-defining transistors TR5 and TR6. The current in TR5 is commutated between the transistors TR1 and TR2, this action being controlled by the base voltage of TR1. When TR2 is conducting, and TR1 "off", the current pulse in TR2 collector is smoothed by the capacitor C_1, and flows in R_2 and in the circuit comprising R_1, in parallel with the series combination of R_3 and the meter resistance R_M. The values of these resistors are arranged so that under normal conditions of operation, saturation of TR2 does not occur. When current in TR6 is commutated into TR3, under the control of the base voltage of TR4, a similar action to the above occurs, but the resulting meter current is then in a direction opposite to the current obtained from TR2. If, due to a fault condition in the operation of the equipment, the time for which TR2 or TR3 conducts becomes excessive, the voltage across C_1 or C_2 builds up until TR2 or TR3 saturates, thus limiting the maximum meter current. The resistors R_2 and R_4 are included for, if the meter were connected directly between the collectors of TR2 and TR3, large current pulses would flow in the instrument as, due to its low resistance, the capacitors C_1 and C_2 would then be virtually in parallel. These pulses would probably cause vibration of the pointer of the meter, with a possible effect on the long-term accuracy of the instrument.

Since the circuit is symmetrical, the calculations for the collector current of TR3 are similar to those for the collector current of TR2. The amplitude i_{c2} of the latter only will therefore be determined, and is

$$i_{c2} = \frac{\alpha_2 \alpha_5 (V_z - V_{be5})}{R_5} \qquad \text{-----} \qquad (20.1.1)$$

where α_2 and α_5 are the common-base current gains of TR2 and TR5 respectively. The mean current flowing in R_2 is thus

$$I_{R2} = i_{c2} f t_\phi \qquad \text{-----} \qquad (20.1.2)$$

where t_ϕ is the duration of the current pulse, and f the frequency at which it is generated. The mean meter current is therefore

$$I_m = \frac{R_1 I_{R2}}{R_1 + R_3 + R_M} \qquad \text{-----} \qquad (20.1.3)$$

where R_M is the meter resistance. Substituting (20.1.2) in (20.1.3),

$$I_m = \frac{R_1 f t_\phi i_{c2}}{R_1 + R_3 + R_M} \qquad \text{-----} \qquad (20.1.4)$$

The meter used has a full-scale deflection current of 500 μA. If this is to correspond to a phase angle of 25° then, putting $R_1 = R_2 = R_3 = R_4 = R$, and $R_M << R$, the required collector current in TR2 is, from (20.1.4),

$$i_{c2} = \frac{2I_m}{f t_\phi} = \frac{2 \times 0.5 \times 360}{25} = 14.4 \text{ mA}$$

$$\text{-----} \qquad (20.1.5)$$

This current is adjusted by selection of the resistor R_5, to accommodate the tolerance in V_{be5} and the Zener diode voltage V_z. Subsequently, there will be a variation in i_{c2} caused by variation in ambient temperature. Assuming there to be negligible change in V_z over the range of temperature specified for the unit, the current i_{c2} will increase with increase in temperature to a value $(i_{c2} + \Delta i_{c2})$, where, from (20.1.1),

$$i_{c2} + \Delta i_{c2} = \frac{(\alpha_2 + \Delta\alpha_2)(\alpha_5 + \Delta\alpha_5)(V_z - V_{be5} + \Delta V_{be5})}{R_5} \quad \text{-----} \quad (20.1.6)$$

Thus, neglecting products of small quantities,

$$\frac{\Delta i_{c2}}{i_{c2}} = \frac{\Delta\alpha_2}{\alpha_2} + \frac{\Delta\alpha_5}{\alpha_5} + \frac{\Delta V_{be5}}{(V_z - V_{be5})} \quad \text{----} \quad (20.1.7)$$

Assuming the common emitter current gain of TR2 and TR5 to be nominally $\bar{\beta} = 100$, and allowing a tolerance of $\pm$ 15% to allow for changes in ambient temperature, the corresponding value of common base current gain is $\alpha = 0.99 \pm 0.002$. Taking the temperature coefficient of V_{be5} as 2 mV per deg. C, a variation of $\pm$ 15 deg. C in ambient temperature will cause a total change ΔV_{be5} of $\pm$ 30 mV. Then, for a Zener diode having $V_z = 5.3$V, substituting these values in (20.1.7) gives

$$\frac{\Delta i_{c2}}{i_{c2}} = \pm \left[\frac{0.002}{0.99} + \frac{0.002}{0.99} + \frac{0.03}{4.6} \right] = \pm 0.01 \quad \text{-----} \quad (20.1.8)$$

As discussed in Sec. 4.3, this figure, representing the error at the extremes of the specified temperature range, is considered to be acceptable, in view of the possible errors in the meter used.

The capacitor C_1 (or C_2) is obviously a component in which a leakage current would directly affect the meter indication. Since, usually, the leakage current of a capacitor increases with its capacitance value, an unnecessarily high value of capacitance should be avoided. On the other hand, too low a value will allow a large ripple voltage to exist across the capacitor, with the possibility of saturation occurring in TR2 (or TR3), and a reduction in the meter reliability. Consider the conditions when the current pulse in TR2 has a duration such as to cause full-scale deflection current in the meter. With a pulse frequency of 50 Hz, the pulse duration will then be

$$t_p = \frac{25 \times 20,000}{360} = 1390\ \mu\text{sec} \quad \text{----- (20.1.9)}$$

For a ripple voltage v_r across C_1 of 1V, then using the value of i_{c2} calculated in (20.1.5), the capacitance must have a value of approximately

$$C_1 = \frac{i_{c2} t_p}{v_r} \quad \frac{0.0144 \times 1390}{1} = 20\ \mu\text{F}$$

----- (20.1.10)

It would be desirable to use a capacitor having a value greater than this, to reduce the ripple voltage below 1V; to obtain an acceptable physical size, an electrolytic type of capacitor is therefore required. Some thought has been given to the choice of this component, and a capacitor having a tantalum anode, a tantalum cathode, and a dielectric of tantalum pentoxide, has been chosen. Particular attention to reliability and stability is given in the manufacture of these capacitors, which have a nominal capacitance value of 47 μF at a working voltage of 75. The specification guarantees a leakage current not exceeding 2 μA, over the temperature range -55^{o}C to $+150^{o}$C, at full rated voltage. The following[36] is an extract from a letter from the Plessey Company, concerning tests which have

been conducted on these capacitors: " ------ The information that we have for these capacitors comes from testing at or near upper temperature rating viz. 150°C : , and with full d.c. rated volts applied. The most authoritative results I can quote you are from tests carried out for Qualification Approval to a Defence Specification, and also some carried out by the Military Electronics Laboratory in Swindon. The first tests involved 16 capacitors (8 off 75V working and 8 off 3V working units) at 150°C for 2000 hrs. The second 10 capacitors (all 75V working units) at 125°C for 4000 hrs. On the basis of allowing up to 10% capacitance change, and doubling of both the leakage current and dissipation factor limits, no capacitors failed. I hope the above is adequate information to enable you to gain sufficient confidence in the reliability over the period in which you are interested, bearing in mind the very large difference in operating temperatures. The level of current pulses you are using should not be large enough to have any effect on the reliability of the capacitors as it is below 10% of the maximum permissible level. "

The leakage current of a capacitor of this type, operating within the working range, is proportional to voltage :[37] a derating factor of approximately 10:1 therefore applies, thus reducing the maximum leakage current to 0.2 μA over the full range of temperature given above. As the maximum temperature specified for the equipment is only 40°C, this will give a further reduction in the leakage current. Tests of leakage current on approximately 12 of these capacitors have been made : with applied voltages up to 30, the leakage current did not exceed 0.01 μA, representing an error of 1 part in 50,000 of full-scale deflection meter current. Two of the capacitors used in the F. T. M. equipment, which had been in service for some two years, were again tested for leakage current, and the results were unchanged. Although none of the tests described above were carried out for a period comparable with the expected life of the equipment, the ratio of measured to permissible leakage current is so large that the use of these capacitors is felt to be justified.

In calculating the value of the resistors R_{1-4}, the assumptions made in deriving equation (20.1.5) will be used. The effective collector load resistance, to d.c., of TR2 or TR3 is then 3R/2. Between pulses of i_{c2} (or i_{c3}), the meter current is supplied from the charge stored in C_1 and C_2; to obtain a well-smoothed meter current, a long discharge time-constant is desirable. Too high a value of R will, however, cause saturation of TR2 or TR3, and an error in phase angle indication. For full-scale deflection current, the mean voltage V_c across the capacitors is

$$V_c = \frac{i_{c2} f t_\phi 3R}{2} \qquad \text{-----} \qquad (20.1.11)$$

giving

$$R = \frac{2V_c}{3i_{c2} f t_\phi} \qquad \text{-----} \qquad (20.1.12)$$

Substituting the values V_c = 6V, i_{c2} = 14.4 mA, and $f t_\phi$ = 25/360, the required value of R is

$$R = \frac{2 \times 6 \times 360}{3 \times 14.4 \times 25} = 4 \text{ kohm} \text{ ---} \qquad (20.1.13)$$

Resistors of 3.9 kohm have therefore been specified. The maximum possible meter current is then limited to approximately twice full-scale deflection current.

As has already been mentioned, the commutation of current into the meter circuit is effected by variation of the base potentials of TR1 and TR4, (Fig. 46). Considering the transistor pair TR1-TR2, with the base potential $v_{b1} \geq +1V$, the current in TR5 flows in TR1, the current in TR2 then being negligible : with $v_{b1} \leq -1V$, TR2 conducts and the current in TR1 is then negligible. Current thus flows in the meter circuit when TR7 or TR8 are saturated; TR7 is saturated only when the inputs A and B to the diodes D1 and D2 are both at "high" potential, while TR8 saturates only when inputs C and D are both at "high"potential. The diodes

D1 and D2 form the gate G5 in Fig. 13, while D3 and D4 form the gate G3. The transistors TR7 and TR8 act as the gate G7. Corresponding inputs to the diodes controlling the base voltage of TR4 (Fig. 46) form the gates G6, G4 and G8 in Fig. 13.

The design of the gating system formed by D1-D4, TR7 and TR8 is straightforward. The values of resistors R_8 and R_9 are determined by a method similar to that used to evaluate R_1 and R_2, Fig. 41, Sec. 19.1, the maximum permissible excursion of v_{b1} being limited by the reverse base-emitter voltage rating of TR1 and TR2. The resistors R_{14-16} and R_{11-13} are arranged to supply sufficient base current to saturate TR7 or TR8 when the appropriate gate inputs are at "high" potential, while ensuring that a suitable reverse base-emitter voltage exists when the gate input voltage is "low". The detailed connections to these gates are shown in Fig. 38.

The results of the tests to determine the stability of the current generators are given in Sec. 24.1, which describes the tests made on the complete Control Centre equipment.

21.1 WARNING LAMP CIRCUITS

A general description of the operation of the warning lamp system has already been given in Sec. 9.1. Fig. 13 shows the logic diagram, while the complete circuit diagram is given in Fig. 38.

The astable multivibrator controlling the warning lamps is shown at A, Fig. 38. The design method is generally as described in Sec. 19.1. Transistors TR42 and TR45 correspond to TR1 and TR2, Fig. 41: the transistors TR43 and TR44, Fig. 38, act as current amplifiers, driving the lamps, which have a 40 mA current rating. Assuming that no collector current flows in TR41, it is important that the multivibrator shall continue to oscillate, thus warning the operator that the phase angle measurement system is not operating correctly. The possibility of a fault in the multivibrator causing the green lamp to glow continuously would therefore violate the "fail-safe" requirements of the system. It is possible to envisage a number of possible component faults which could cause this fault condition, for example, a collector-emitter short-circuit in the transistor TR44; the multivibrator shown in Fig. 38 is thus not completely "fail-safe". However, a reliability forecast for the components in the multivibrator which could cause a "continuous green" indication, results in an M.T.B.F. which is very long indeed. It was therefore decided to use this simple system, in the expectation that a failure in its operation would be extremely unlikely, and obvious to the operator or during routine testing of the equipment.

A contingency for which provision was made, is the possibility of both TR42 and TR45 being simultaneously saturated: both lamps would then be energised, and in the event of the red lamp failing, a "continuous green" indication would be given. Simultaneous saturation of TR42 and TR45 can, in principle, occur; the voltage

gain of these transistors is then less than unity, and a stable condition of the multivibrator exists. It has been found impossible to achieve this condition experimentally, using the transistors specified, although it is readily shown in some multivibrators using integrated circuits; the components D76, D77 and C_{23} have, however, been included, to prevent any possibility of its occurrence. Their action is as follows: during normal oscillation of the multivibrator, C_{23} is charged from E_b via R_{170} and D76, and R_{176} and D77, alternately; C_{23} provides a reservoir of charge, supplying the base currents to saturate TR42 or TR45. Should saturation occur simultaneously in both of these transistors, the voltage on C_{23} falls until one of the transistors becomes unsaturated, when oscillations commence.

Under normal conditions of operation of the equipment, the oscillations of A are inhibited by the saturation of transistor TR41, (Fig. 38), the base current of which is provided from the output of the diode pump[38] formed by D72, D73, C_{21} and C_{22}. This is driven from the monostable multivibrator M5, which is triggered from MB21. The purpose of M5 is to ensure that the diode pump is provided with an input voltage always of constant amplitude and duration, independent of the duration of the pulse output from MB21, which latter varies with the phase angle conditions. Saturation of TR41 causes the base potential of TR42 to become negative; collector current in that transistor ceases, and base current in TR45 is provided via D78, R_{177}, D76 and R_{170}. TR45 therefore saturates, causing saturation of TR44, which energises the green lamp. Resistors R_{171} and R_{173} are provided to prevent excessive transient power dissipation in TR43 and TR44 which would otherwise occur on switching on these transistors, due to the low resistance of the lamp filaments when cold.

22.1 DESIGN OF THE SUBSTATION UNIT

The F. T. M. version of the substation unit used discrete components throughout, and many of the circuits developed for the Control Centre equipment were used. The unit is now obsolete, and will not be further described. A substantial fraction of the components in the F. T. M. unit were those associated with the time delay generator (Sec. 7.2), and when the design of the M. S. E. V. version was undertaken, the advantages of using integrated circuits for the nine binary stages were obvious. The unit was therefore redesigned generally to exploit the capabilities of the integrated circuits then available.

A choice had to be made of the type of integrated circuit (i. c.) best suited to this application. At the commencement of the design, the types of i. c. logic elements which were readily available were Resistor-Transistor Logic (RTL), Diode-Transistor Logic (DTL), and Transistor-Transistor Logic (TTL).

The advantages of RTL were low cost, an established reliability record (Sec. 16.4), a well-proven encapsulation in TO5 cans, and a specification allowing a $\pm$ 10% variation in d. c. supply voltages. In addition, this type of logic element appeared to lend itself to a neat and economical design of the substation unit. The advantage of DTL over RTL was the higher value of noise immunity inherent in this type of element : a serious disadvantage was the high cost of these elements at the time a decision on the type of i. c. was being made. The advantages of TTL were a higher noise immunity than RTL, and the availability of elements having several binary counters in one package : only three packages would be required for the nine binary divider stages in the time delay generator. The disadvantages of TTL were the $\pm$ 5% tolerance requirement for the d. c. supplies, and also the "dual-in-line"type of encapsulation : when the choice of i. c. was being made, both

the ceramic and plastic packages had been manufactured for a period which was small compared with the expected life of the phase angle equipment, and confidence in their reliability could not be assured.

The choice therefore lay between RTL and TTL. There would have been little difference in the cost of substation units made from either of these elements. The greater noise immunity of TTL was not a major factor in the choice; the logic system is so simple that all of the circuit elements can be mounted on one printed circuit board, and effective decoupling of the d.c. supplies is readily achieved. Using TTL, the reduction in the number of packages in the binary divider stages was attractive, but this was offset by an increase in the number of elements elsewhere in the circuit, due to unavoidable awkwardness in the design caused by the inherent nature of the TTL elements. In designing equipment for a life of a decade or more, a designer prefers to use components of proven reliability, and this consideration, coupled with the relaxed permissible tolerance on d.c. supply voltages, led to the selection of RTL for this equipment. In view of the developments in integrated circuit technology which have since occurred, this decision might well be reconsidered if the equipment is ever redesigned : it might be preferable to integrate the whole of the elements on one silicon chip, providing the number of units required was sufficient to justify the cost of development.

The logic diagram for the M.S.E.V. substation unit is shown in Fig. 47: the circuit diagram is shown in Fig. 48, while Fig. 49 gives the voltage waveforms at various points in the circuit. In the latter, the suffix refers to the pin or electrode of an element, followed by the designation of that element as given in Fig. 48.

A general description of the operation of the F. T. M. substation unit has already been given in Sec. 8.1, and Fig. 11. The logic system for the M. S. E. V. unit was rearranged to avoid the need for the logical delays D1 and D2 in Fig. 11, and to make use of the inbuilt capabilities of the integrated circuits. Referring to Fig. 47, the 50 Hz voltage of which phase measurement is to be made is applied to the voltage comparator FC, the output voltage of which has a "square" waveform. This voltage is applied, via the OR gate G3, to the monostable multivibrator M13; the resulting 200 μsec. output pulse from M13, suitably amplified by A, is delivered to the pilot line by the transformer LT, and is the primary pulse as defined in Sec. 6.1. The voltage from FC is also applied to the AND gate G2, and this gate input is therefore at logical "1" potential for the first half cycle of the 50 Hz voltage. On receipt of the secondary pulse from the Control Centre, the output voltage from LC caused by this pulse is thus able to trigger B0 via G2: this determines the start of the period T_d, which is generated by the crystal oscillator X and binary divider chain B1-B9, as explained in Sec. 7.1. At the termination of this period, i.e., at a time some 12-13 msec. after the generation of the primary pulse, the output from FC will then be logical "0" : the output from the inverter I will thus be "1" , allowing M13 to be triggered from B0 via G4 and G3, and resulting in the generation of a tertiary pulse.

The primary and tertiary pulses delivered to the pilot line by A are inevitably also delivered to LC : precautions have therefore to be taken to avoid the generation of a pulse by M13 at a time T_d after the primary and tertiary pulses, in addition to the intended generation of a pulse following the reception of a secondary pulse. This incorrect mode of operation is prevented by the gates G2 and G4. At the instant of reception by LC of a primary pulse generated by M13, the output from FC will already be at logical "1" ; B0 will therefore be triggered by LC, but at the termination of the period

T_d the output of I will be "0", and M13 will therefore not be triggered. At the instant of reception of a tertiary pulse, the output of FC will be "0"; B0 will therefore not be triggered, and neither, therefore, will M13. Thus, the possibility of the generation of unintended pulses by M13 is avoided.

22.2 Substation Voltage Comparators

There are two voltage comparators in the substation unit. The comparator LC, (Fig. 47 and 48), senses the instant when the secondary pulse voltage developed across the line transformer LT reaches the value V_{ref}, and its action is similar to the voltage comparators in the Control Centre unit, described in Section 18. The accuracy required in this voltage comparator has already been discussed in Sec. 13.1, where it was shown that for a pilot line of probably the poorest characteristics likely to be used, an error of 1/10 degree in phase angle measurement would be caused by an error of 85 mV in the sensing level V_{ref}.

The voltage comparator FC, (Figs. 47 and 48), senses the zero crossover of the 50 Hz test voltage from the 110/110V isolating transformer VT. The accuracy required may be determined very simply. Let the test voltage developed across the secondary of the transformer VT be $e = \hat{e}\sin\omega t$. When passing through the zero value,

$$\left.\frac{de}{d\omega t}\right|_{\omega t = 0} = \hat{e} \qquad \text{-----} \qquad (22.2.1)$$

Thus, the error $\Delta\omega t$ caused by an error ΔV_{ref} in the nominally zero reference voltage will be

$$\Delta\omega t = \frac{\Delta V_{ref}}{\hat{e}} \qquad \text{-----} \qquad (22.2.2)$$

For a maximum error $\Delta\omega t$ of 1/10 degree, then with the 110V r.m.s. input voltage from VT, the allowable error in reference voltage is

$$\Delta V_{ref} = \hat{e}_{\Delta\omega t} = \frac{110\sqrt{2}}{10 \times 57.3} = 0.27 \text{ volt} \quad \text{-----} \quad (22.2.3)$$

For the M.S.E.V. substation unit, the commercially-available comparator type 710C was used; a diagram of connections is given in Fig. 50, and the published electrical characteristics in Table 11. A definition of terms used in the latter is given in Table 12.

Consider the comparator FC, Fig. 48. The test voltage from VT is applied to one input terminal via the resistor R_6 which, together with the diodes D4 and D5, protect the comparator against excessive input voltage. The value of R_6 is a compromise; a high value restricts the accuracy of voltage zero sensing, while a low value causes unnecessary heating in R_6. A resistor R_5, of nominal value equal to R_6, is connected in series with the other input terminal. Let

V_{os} = input offset voltage,
i_{os} = input offset current,
i_b = input bias current,

as defined in Table 12. The input current to terminals 3 and 2 (Fig. 50) will then be

$$i_3 = (i_b + \frac{i_{os}}{2}), \text{ and } i_2 = (i_b - \frac{i_{os}}{2}), \text{ respectively.}$$

Let $R_5 = (R_A + \Delta R)$, and $R_6 = (R_A - \Delta R)$, the term ΔR representing the tolerance on the nominal value R_A. Then, the voltage V_{ref} across VT required to cause the output voltage to be at the logic threshold value will be

$$\Delta V_{ref} = v_{os} + (i_b + \frac{i_{os}}{2})(R_A + \Delta R) - (i_b - \frac{i_{os}}{2})(R_A - \Delta R)$$

$$= v_{os} + 2i_b \Delta R + R_A i_{os} \quad \text{-----} \quad (22.2.4)$$

Taking worst-case values of v_{os} and i_{os} in the $0^{o}C$ to $70^{o}C$ temperature range given in Table 11, and assuming a $\pm$ 2% tolerance on R_A then, substituting these values in (22.2.4), we get

$$\Delta V_{ref} = 6.5 + (2x40x0.02x22) + (22 \times 7.5)$$
$$= 6.5 + 35.2 + 165$$
$$= 226.3 \text{ mV} \quad \text{-----} \quad (22.2.5)$$

Alternatively, taking the worst-case $25^{o}C$ values of v_{os} and i_{os} given in Table 11, substitution of these in (22.2.4) gives

$$\Delta V_{ref} = 5 + (2 \times 25 \times 0.02 \times 22) + (22 \times 5)$$
$$= 5 + 22 + 110$$
$$= 137 \text{ mV} \quad \text{-----} \quad (22.2.6)$$

In both of these cases, the component of ΔV_{ref} caused by the offset current i_{os} is by far the largest. The component could be reduced by decreasing the value of R_5 and R_6, with a corresponding increase in the power dissipated in R_5. With R_5 = 22 kohm, the power dissipated in that resistor is 0.55 watt, and it is considered that a value much in excess of this would be undesirable, in the interests of stability and reliability of the unit.

A substantial reduction in ΔV_{ref} could be made by initial adjustment of the potential to which R_5 is connected. This could be done by connecting a high resistance from pin 2 to the appropriate d.c. supply. However, this would require an extra "adjust-on-test" operation during manufacture of the unit, and it was thought to be an unnecessary refinement in view of the acceptable "worst-case" value of ΔV_{ref} given in equations (22.2.6) and (22.2.5).

The voltage comparator FC is, of course, fundamental to the accuracy of the phase angle measurement; an error ΔV_{ref} in the nominally zero crossover voltage will cause a corresponding error in measured phase angle, as given by equation (22.2.2). This error in phase indication will be very small, for any expected change in ΔV_{ref} caused by changes in supply voltages, ambient temperature, or the effects of ageing of the components. However, it is possible that a much larger change in ΔV_{ref} could occur, should a gross malfunction of the comparator be caused, for example, by catastrophic failure of an element within the integrated circuit. This contingency is provided for by the diodes D4 and D5; by their clipping action on the input from VT, the voltage applied to FC cannot exceed approximately $\pm$ 0.8V. From equation (22.2.3) this voltage corresponds to an error of only 0.3 degree in phase angle. Should the comparator FC develop a fault causing ΔV_{ref} to exceed $\pm$ 0.8V, it will cease to operate; thus D4 and D5 give "fail-safe" protection against large undetected errors in phase measurement caused by such a failure.

In the case of the comparator LC, the error ΔV_{ref} between the voltage developed across the line transformer LT, for an output voltage at logical threshold, and the nominal value of 1 volt, will be much less than for the comparator FC, as the resistor R_8 in series with the input is now only 10 kohm, and the initial adjustment of $(R_2 + R_3)$, to accommodate the Zener diode voltage tolerance, performs a similar function for the offset voltage of LC. Subsequent variations in ΔV_{ref} will therefore be caused only by variations in operating voltages, temperature and the effects of ageing of the components.

Extended tests were carried out on eighteen 710C voltage comparators, in an attempt to assess the possible magnitude of these variations. 10 kohm resistors were connected in series with each of the inputs, and one input was earthed: the voltage ΔV_{ref} required at the other input to cause the output voltage to be at the logic threshold value was then measured. The eighteen comparators were assembled on a chassis, each having provision for the connection of feedback from the output to the inverting input, via a suitable level-shifting potential divider; by this means the comparators could be maintained in the active state during the long-term tests.

The first test was to measure the variation in ΔV_{ref} with ambient temperature. For this, the chassis was mounted inside a totally-enclosed aluminium box, which was itself mounted in an environmental test chamber. With supply voltages at their nominal values, the temperature inside the chamber was varied in steps over the range $-20^{o}C$ to $+50^{o}C$, this being 20 degrees greater than the specification requires. The value of ΔV_{ref} for each comparator, at each step in temperature, was then measured. The results are shown in Fig. 51, which has been drawn normalized to $20^{o}C$, i.e., to show the relative variation in ΔV_{ref} with change in temperature of the comparators. The lines in the Figure represent the limits of ΔV_{ref} for the eighteen comparators tested. It will be seen that over the required temperature range of $0^{o}C$ to $+50^{o}C$, the worst sample shows a variation not exceeding 7.1 mV.

The second test was to measure the variation in ΔV_{ref} which occurred when the supply voltages were varied. This test was conducted at laboratory temperature. With the negative supply voltage set at 5, 6 or 7 volts, the positive supply voltage was varied in steps from 10V to 14V. For each combination of supply voltages, ΔV_{ref} was measured, and the results are given in Table 13. It will be seen that over the $\pm$ 1V and $\pm$ 0.5V tolerance specified for the positive and negative supply voltages respectively, the total variation of ΔV_{ref} in the worst unit does not exceed $\pm$ 1.65 mV.

Element No.	Positive Supply Voltage +10	+11	+12	+13	+14	Negative Supply Voltage
1	-2.4	-2.2	-2.0	-1.8	-3.4	
2	+2.9	+3.1	+3.3	+3.5	+3.5	
3	+5.9	+6.1	+6.2	+6.1	+6.7	
4	+2.0	+2.5	+2.5	+2.5	+2.8	
5	+0.1	+0.7	+1.2	+1.6	+2.0	
6	-6.4	-5.7	-4.8	-4.6	-4.0	
7	+6.9	+7.5	+7.7	+7.9	+7.9	
8	+6.4	+6.5	+6.7	+6.6	+6.5	-5
9	+1.7	+2.1	+2.2	+2.4	+2.6	
10	+10.2	+10.4	+10.5	+10.5	+10.8	
11	-3.5	-3.0	-2.9	-2.6	-2.6	
12	+26.4	+26.3	+26.2	+25.7	+25.4	
13	+22.5	+22.2	+21.5	+21.3	+20.6	
14	+1.3	+1.9	+2.1	+2.3	+2.5	
15	+2.0	+2.2	+2.3	+2.5	+2.6	
16	+7.5	+7.7	+7.7	+7.6	+7.5	
17	-0.8	-0.6	-0.2	-0.1	-0.1	
18	-3.2	-2.5	-2.3	-2.0	-1.7	

TABLE 13. Variation in voltage comparator error ΔV_{ref}, (mV), with variation in supply voltages.

continued...

Element No.	Positive Supply Voltage +10	+11	+12	+13	+14	Negative Supply Voltage
1	-5.8	-4.5	-4.0	-3.7	-3.4	
2	+2.2	+3.2	+3.6	+3.5	+3.8	
3	+5.3	+6.2	+6.5	+6.6	+6.5	
4	0	+1.3	+1.7	+1.4	+1.6	
5	-2.6	-0.8	0	+0.5	+0.9	
6	-12.2	-9.9	-8.5	-8.0	-6.8	
7	+6.7	+7.7	+8.1	+8.6	+8.5	
8	+5.9	+6.7	+6.8	+7.2	+6.9	
9	+0.5	+1.5	+2.0	+2.3	+2.5	-7
10	+10.2	+11.0	+11.2	+11.2	+11.2	
11	-5.3	-4.9	-4.2	-3.9	-3.7	
12	+31.9	+31.9	+31.3	+31.1	+30.8	
13	+23.9	+24.0	+23.7	+23.3	+28.8	
14	-0.6	+0.3	+0.7	+0.8	+1.0	
15	+0.8	+1.8	+2.1	+2.2	+2.2	
16	+7.6	+8.2	+8.2	+8.1	+8.1	
17	-1.8	-0.9	-0.5	0	+0.1	
18	-6.4	-4.8	-4.2	-3.7	-3.4	
1	-4.2	-3.5	-3.2	-2.9	-2.7	
2	+2.8	+3.3	+3.5	+3.3	+3.6	
3	+5.7	+6.3	+6.4	+6.4	+6.5	
4	+1.3	+1.9	+2.1	+2.4	+2.2	
5	-1.1	0	+0.5	+0.9	+1.3	
6	-9.6	-7.8	-7.2	-6.5	-5.8	
7	+6.9	+7.7	+7.9	+8.3	+8.1	
8	+6.6	+6.8	+6.9	+6.7	+6.6	-6
9	+1.1	+1.8	+2.1	+2.3	+2.5	
10	+10.4	+10.9	+10.9	+11.0	+10.8	
11	-4.3	-4.0	-3.8	-3.2	-3.3	
12	+29.8	+29.4	+29.1	+28.9	+28.7	
13	+23.7	+23.6	+22.9	+22.8	+21.8	
14	+0.3	+1.1	+1.2	+1.4	+1.9	
15	+1.7	+2.1	+2.3	+2.3	+2.3	
16	+7.9	+8.0	+8.2	+7.9	+8.1	
17	-1.4	-0.7	-0.1	-0.2	-0.3	
18	-4.8	-3.8	-3.4	-3.0	-2.6	

A long-term test was then conducted, at laboratory temperature and nominal supply voltages, to determine the variation of ΔV_{ref} over an extended period. The results of tests over approximately two years are shown in Table 14, which gives the value of ΔV_{ref} for the eighteen voltage comparators. It will be seen that the variation of ΔV_{ref} over that period does not exceed 1.2 mV for the worst unit.

It would seem, from the preceding tests, that the total effect of variations in ambient temperature and supply voltages over the whole of the specified range, added to the effect of two years ageing, is to cause a variation in ΔV_{ref} of approximately 10 mV, for the worst unit tested. This variation in the comparator FC would cause an error in phase angle indication of 1/270 degree, (equation 22.2.3), while in LC it would cause an error of 1/85 degree on a poor pilot line (Sec. 13.1). It is concluded, therefore, that the performance of the 710C voltage comparator is adequate for these applications.

22.3 Substation Circuit Design

A general description of the operation of the substation unit has already been given in Sec. 22.1. This present Section will give an explanation of the way in which the circuits have been arranged to exploit the inbuilt capabilities of the integrated circuit elements available. A complete circuit diagram is given in Fig. 48, while circuits of the elements type 915 and 926 shown thereon are given in Fig. 53. A list of components used is given in Appendix B. Voltage waveforms in various parts of the circuit, measured with respect to earth, are shown in Fig. 49.

As can be seen from the truth table in Fig. 53, B0 is a type 926 "JK" element[42]: the connection of pin 4 to +3.6V via R_{12} allows B0 to be "set", but not "cleared", by a pulse applied at pin 3. During the positive half-cycle of the 50 Hz test voltage applied to pin 3 of FC, the output voltage of that element will be "low", thus

allowing B0 to be set by the secondary pulse output from LC. During the negative half-cycle of the test voltage, the output voltage of FC will be "high"; B0 is thus insensitive to the tertiary pulses from LC.

The element A in Fig. 48 is a type 915 dual 3-input gate. For ease of description, the transistors in this element will be referred to by a suffix corresponding to the number of the input pin; for example, the transistor having an input at pin 1 will be labelled TR1. The gate formed by TR8 acts as the inverter I in Fig. 47 : the 3-input gate formed by TR1-3 acts, with transistor D, as the monostable multivibrator M13 in Fig. 47. The design of this multivibrator is somewhat unorthodox. In the quiescent state, D is conducting, due to base current flowing in R_{16}. When the 50 Hz test voltage passes through the zero value into the positive half-cycle, the output voltage v_{9A} of TR8 rises; TR1 saturates, and remains so for the remainder of the half-cycle. The resulting fall in potential at pin 4 is communicated by C_3 to the base of D, which transistor then ceases to conduct. Current in R_{16}, charging C_3, now causes the base potential of D to rise and, after a period of approximately 200 μsec., D conducts once more. This action results in a positive pulse of voltage at the collector of D, which pulse is transmitted to the transistor T, causing this to saturate and deliver a primary pulse to the line transformer LT. The action of A and D in generating a primary pulse is thus non-regenerative, and the trailing edge of this pulse might be expected to be poorly defined. However, the voltage gain of the cascaded transistors D and T is sufficiently high that the output pulse waveform is experimentally indistinguishable from that produced when A and D are operated regeneratively. In any case, the waveform of the trailing edge of the pulse has no significance in the action of the system.

During the negative half-cycle of the test voltage, TR8 conducts; TR1 is therefore "off". On completion of the period T_d, (Sec. 7.2), the output voltage v_{9B0} of B0 rises, and the "differentiating" action of C_2 and R_{13} causes TR3 momentarily to conduct: the resulting fall in output voltage v_{4A} is transmitted to D, and thence fed back via R_{14} to TR2. This regenerative action results in the generation of a 200 μsec. tertiary pulse, which is amplified by T and delivered to the line transformer LT.

In this system of pulse generation, transistors TR1, TR2 and TR3 all contribute to the output voltage v_{4A} from pin 4. For example, with TR1 and TR2 both saturated, as happens during the generation of a primary pulse, v_{4A} will have a slightly lower value than when only TR1 is saturated, which condition occurs after the pulse has terminated. This change in v_{4A} is minimized by returning R_{13} to pin 1 on A, rather than to earth; the resistor R_{15} is included so that the remaining small variation in v_{4A} cannot cause sufficient current to flow in C_3 to bring D out of saturation.

The crystal oscillator X from which the time delay T_d (Sec. 7.2) is derived, has an output voltage v_{7X} of approximately "square" waveform. This is fed, via a current-limiting resistance R_{25}, [39] to B1, the first of the nine frequency-dividing stages. When B0 is "set" by the secondary pulse from LC, the output voltage v_{9B0} falls, allowing pulses from X to trigger B1. After 2^9 trigger pulses have been thus received by B1, B9 returns to the "0" state, and the rise in output voltage v_{9B9} from that element, after "differentiation" by C_1 and R_{11}, is applied to the "preclear" input, pin 1, of B0. This results in a change of state in B0, and the resulting rise in v_{9B0} prevents any further triggering of B1 from X : all of the elements B1-B9 are then in the "0" state.

The design of the crystal oscillator is straightforward. The same type 710C integrated circuit used for LC and FC is also used as a voltage amplitude-limited amplifier to generate the oscillations. The square-waveform output voltage v_{7X} from the element X is delivered, via a suitable potential divider R_{20-21}, to the 100 kHz crystal. This causes a current in the crystal which, due to the high "Q" of the crystal, is a close approximation to a sinusoid; the resulting sinusoidal voltage across R_{22} forms the input voltage to the element X, and is of sufficient magnitude to cause X to act as an overdriven amplifier, resulting in the "square" output voltage waveform. An advantage of this mode of operation is the simplicity of the circuit, compared with a usual arrangement wherein sinusoidal oscillations are generated, and additional circuits used to convert these to a pulse waveform. Another advantage is the stability of frequency gained by operating the crystal at series resonance : the resistors R_{21} and R_{22} have values small compared with the effective series resistance (nominally 800 ohms) of the crystal, and the "Q" of the crystal is not therefore seriously degraded by the circuit to which it is connected. There is one possibility, however, against which precautions must be taken. Should the crystal become open-circuited, then the effect of the self-capacitance C_s of the crystal and associated wiring might permit relaxation oscillations which, not being accurately controlled in frequency, would cause an error in T_d and hence in the phase angle indication. This contingency has been provided for by the inclusion of capacitor C_4 which, acting as a low-pass filter in series with the high-pass filter formed by C_s and R_{22}, ensures that the loop gain can never, at any frequency, approach unity; unintended oscillations thus cannot occur. With the values shown, and assuming a crystal self-capacitance C_s = 5 pF then, for oscillation, a voltage gain of the element X in excess of 8000 would be required: this is a value unlikely to be approached in this type of integrated circuit. Experimentally, using an i.c. selected for high gain, a capacitance of

approximately 100 pF was required for oscillation to occur.

A further contingency which could arise is that with the inverting input to X earthed, the offset voltage of the element might be sufficient to cause the output voltage to remain at one or other of the limiting values. The voltage gain of the amplifier would then be zero, and oscillations would never start. This possibility is avoided by connecting the inverting input (pin 3) to the potential divider formed by R_{23} and R_{24}, and smoothing the voltage obtained therefrom by the capacitor C_5. Suppose now that oscillation ceases : the potential of v_{3X} will rise towards v_{7X}; the values of R_{23} and R_{24} have been chosen so that v_{3X} will then always pass through zero. The action of this "d. c. feedback" is thus to ensure that when oscillations are absent, the amplifier is brought into the middle of its dynamic range, and thus into the condition of maximum voltage gain.

The design of the 200 μsec. pulse generator output stage T is dependent on the maximum load across which the output voltage must be developed. It is essential, for proper operation of the measurement system, that the transistor T shall always saturate when a pulse is being generated. Referring to Fig. 54, which gives a detail of the circuit supplying base current to T, the network equations are

$$E_b - v_{b1} + i_1(R_{17} + R_{14} + R_b) - i_2 R_{17} = 0 \qquad (22.3.1)$$

$$E_b - v_{bT} + i_1 R_{17} - i_2(R_{17} + R_{18}) = 0 \qquad (22.3.2)$$

$$E_c + v_{bT} - i_3 R_{19} = 0 \qquad (22.3.3)$$

Eliminating i_1 between (22.3.1) and (22.3.2),

$$i_2 = \frac{(E_b - v_{bT})(R_{17} + R_{14} + R_b) - (E_b - v_{b1})R_{17}}{(R_{17} + R_{18})(R_{14} + R_b) + R_{17}R_{18}} \quad \text{-----} \quad (22.3.4)$$

From (22.3.3),

$$i_3 = \frac{E_c + v_{bT}}{R_{19}} \quad \text{-----} \quad (22.3.5)$$

The base current i_{bT} of transistor T is

$$i_{bT} = i_2 - i_3 \quad \text{-----} \quad (22.3.6)$$

To calculate the minimum value of i_{bT}, the following worst-case values are taken :

E_b = 11V, E_c = 6.5V, v_{bT} = 1.8V, v_{b1} = 0.7V,

R_b = 450-20% = 360 ohms

R_{14} = 1500-5% = 1425 ohms, R_{17} = 470+5% = 493 ohms,

R_{18} = 220+5% = 231 ohms, R_{19} = 3300-5% = 3130 ohms.

Substituting these values in (22.3.4) and (22.3.5), and using (22.3.6),

$$i_{bT} = \frac{(11 - 1.8)(493 + 1425 + 360) - (11 - 0.7)493}{(493 + 231)(1425 + 360) + (493 \times 231)} - \frac{(11 + 1.8)}{3130}$$

$$= 8.65 \text{ mA} \quad \text{-----} \quad (22.3.7)$$

The minimum d.c. current gain $\bar{\beta}_{min}$ of the BFY56A transistor at 25°C and with I_c = 150 mA is given in the maker's data as 40. Applying a reduction of 25% for operation down to 0°C, and a

further 15% for ageing, $\bar{\beta}_{min}$ is then 25.5. Thus, the base current i_{bT} is sufficient to ensure that a minimum collector current of $i_{cT} = \bar{\beta}_{min} i_{bT} = 25.5 \times 8.65 = 220$ mA is available.

This collector current has to supply the magnetizing current i_{mag} of the line transformer, and the current in the load, the latter comprising the currents in the pilot line and terminating resistor R_2, (Fig. 23). The value of the magnetising current is

$$i_{mag} = \frac{(E_b - V_{ce(sat)})t_p}{L} \quad \text{-----} \quad (22.3.8)$$

where t_p = pulse duration, and

L = shunt inductance of the line transformer.

Substituting worst-case values $E_b = 11V$, $V_{ce(sat)} = 0$, $L = 0.5$ H, $t_p = 200$ μsec., then

$$i_{mag} = \frac{11 \times 220}{0.5 \times 10^6} = 4.4 \text{ mA} \quad \text{---} \quad (22.3.9)$$

Neglecting, in the worst-case, the resistance of the transformer windings, and the saturation voltage of the series transistors TR1 and TR2, (Fig. 23), the current i_{PL} available for the pilot line is then

$$i_{PL} = i_{cT} - i_{mag} - \frac{(E_b - V_{ce(sat)})}{R_{2min}}$$

$$= 220 - 4.4 - \frac{11}{209}$$

$$= 163 \text{ mA} \quad \text{-----} \quad (22.3.10)$$

This corresponds to a pilot line of characteristic impedance $Z_o = E_b/i_{PL} = 11/0.163 = 67.5$ ohms. It is unlikely that any pilot line used with this equipment will have a characteristic impedance lower than this value. The transistor T will thus always saturate when a pulse is generated, and a pulse of standard amplitude will be transmitted, as required for the correct operation of the system.

The diodes D6-D8 associated with T protect that transistor from excessive transient voltages induced in the pilot line, which may be caused by electrical noise or by line testing procedures. The use of the Zener diode D7 ensures that this protection is given with negligible effect on the reverse overswing voltage of the transformer, discussed in Section 11.

23.1 POWER SUPPLY UNITS

The power supply units for the Control Centre and substation equipments were designed and manufactured by Roband Electronics Ltd., to a University specification. The type P2780 units used in the Control Centre equipment were made in early 1967 for the F. T. M. version and, owing to the long delivery forecast, the order had to be placed at an early stage in the design of this equipment. It was necessary, therefore, to make an estimate of the required output of the units, and the degree of protection against the transmission of a. c. supply voltage transients needed, some time before the current consumption or sensitivity of the circuits to transient voltages were known. As a result, the output of these units is greater than that required by the Control Centre phase angle measurement circuits alone. However, during this project a further requirement arose, this being the accurate measurement of supply frequency:[7] the equipment for this latter measurement has therefore been mounted in the same case as the phase angle equipment, and both share the same P2780 power supply unit.

The specification[40] for the P2780 units agreed with Roband Electronics includes the following :

Input voltage	:	110V or 240V r. m. s., +10% - 15%.
Output voltages	:	+12V at 1A d. c., -12V at 1A d. c.
Output resistance	:	0. 05 ohm.
Ripple and noise	:	< 1 mV r. m. s.
Reliability	:	50, 000 hours M. T. B. F.
Long-term stability	:	Neither output voltage shall depart from nominal by more than 1 volt, and the value of the positive and negative voltages shall not differ by more than 0. 6V, during a time equal to the M. T. B. F.

Filtering	:	Efficient filters to be provided, to give maximum attenuation to transient voltage "spikes" that may occur on the a.c. supply voltage. This to include triple independent screens between primary and secondary of the power transformer.

When this specification was issued, it was intended that the P2780 unit would also be used in the substation equipments : an ambient temperature range of $-10^{\circ}C$ to $+50^{\circ}C$ was therefore specified. As the unit is now used only in the Control Centre equipment, for which a $+10^{\circ}C$ to $+40^{\circ}C$ range is specified, this temperature range is unnecessarily wide. For the power units installed, therefore, an improvement in the stability figures given above may be expected.

The power supply units for the substation equipments are type P2780B, and have a specification generally similar to the above, with the following differences :

Output voltages	:	+12V $\pm$ 1V at 150 mA. +3.6V $\pm$ 0.18V at 500 mA. -6V $\pm$ 0.6V at 50 mA.
Transient output voltages	:	Input/output filtering shall be provided which will prevent any of the output voltages exceeding the absolute maximum rating of the load voltage, when the unit is switched on or off, or in the event of a transient voltage occurring in the a.c. input voltage.

The absolute maximum load voltages are:

+12V supply : +14V.
+3.6V supply : +4.5V.
-6V supply : -7V.

Under these transient conditions there shall be negligible reverse output voltage.

Overload protection: Current-limiting overload protection shall be fitted.

In addition to the specification given above, there is a further requirement for the P2780B substation power units. During the development of the F. T. M. equipment, it became obvious that the reliability of the system could be improved by using the source of 50 Hz test voltage also to provide the power for the substation equipment, rather than to obtain the latter from a separate supply. The input current to a rectifier using a capacitive filter is normally rich in harmonics, and some concern was felt, when contemplating the connection of such a rectifier to a substation V.T., that these harmonics might affect the indication of other measuring instruments connected to the same V. T. A careful test was therefore made, in the presence of representatives of the M. E. B. and C. E. G. B., of the harmonic content of the V. T. voltage waveform, using a sensitive wave analyser. It was shown to their satisfaction[41] that the harmonic content was unaffected by connection of the phase angle equipment, using a P2780 power supply unit. The further requirement for the P2780B unit was, therefore, that the harmonic content of the a. c. input current should be low, and not, in any case, greater than that for the P2780 unit. The measured harmonic content of the input current to both units is given in the next Section.

23.2 Power supply unit tests

The stability of output voltage of three of the P2780 units was checked, by measuring the voltage before and after a period in service. The results are given below.

Unit	Output voltages April 1967	Output voltages Sept. 1968	Voltage change
A	+12.018	+11.990	-0.028
	-11.966	-11.956	-0.010
B	+12.018	+12.063	-0.043
	-12.067	-12.052	-0.015
C	+12.067	+11.984	-0.083
	-12.010	-11.992	-0.018

These results are considered satisfactory.

Twelve of the P2780B units were tested continuously at full load, for 1000 hours, and the three output voltages of each unit were measured before and after the test. In all cases the voltage change was less than 20 mV.

The harmonic content of the a.c. input current i to the P2780 and P2780B units, when supplying the substation equipment, was measured, and the harmonic content of the supply voltage v was measured also. The results are given below.

Frequency	P2780		P2780B	
	v	i	v	i
f	0 db	0 db	0 db	0 db
2f			-58	-56
3f	-40	-3	-40	-12
4f			-70	-60
5f	-56	-5	-42	-10
6f			-70	-70
7f		-10	-53	-22
8f			-70	-70
9f		-16	-55	-27
10f			-70	-70
11f		-27	-60	-27

In these measurements, -70 db represents the smallest discernible indication. The r.m.s. value of the input current to the P2780 and P2780B units was 160 mA and 184 mA, respectively. It will be seen from the above table that the harmonic content of the input current to the P2780B unit is less than that for the P2780 unit, on which latter the tests to determine the acceptability of the equipment to the M.E.B. and C.E.G.B. were made.

The measured current consumption of the Control Centre and substation units is given below.

Control Centre	+12V	-12V
Phase measurement unit :	220 mA	63 mA
Frequency measurement unit :	515 mA	113 mA

Substation unit

+12V 64 mA : +3.6V 250 mA : -6V 16 mA.

24.1 M. S. E. V. EQUIPMENT TESTS

For the Multi-Station Engineered Version of the equipment, one Control Centre unit and twelve substation units were made. Figs. 60 and 61 show the completed units. Installation in the Birmingham Area of the M. E. B. was started early in 1970, and completed by May of that year.

As has already been mentioned, the Field Trials Model of the Control Centre unit has been used, after modification, as the M. S. E. V. unit. To obtain the required multi-substation operation, a pair of double-pole substation selector switches, mounted on a separate panel, connect the "pilot line A or B"terminals shown in Fig. 38 to any pair of incoming pilot lines. As the switch contacts and the associated wiring are metallically connected to the pilot lines, they have a breakdown voltage rating of 2 kV to earth, as specified for the line transformers (Sec. 11.1). The F. T. M. unit had already been in service for many months, and further "burn-in" tests were considered unnecessary. Tests were, however, made to determine the effect of ambient temperature on the performance of the unit. For these tests the Control Centre unit was mounted in the environmental chamber; one line input was connected to a substation unit via the pilot line "X" (Sec. 14.1), and the other input connected directly to a second substation unit. Test voltages of accurately-known phase difference were applied to the substation units from the calibrator (Sec.26.2). Readings of indicated phase angle were taken, at three values of ambient temperature, and the results are given in Table 16. In spite of the use of an illuminated magnifier, there is the possibility of a small reading error caused by the seven thicknesses of plate glass in the chamber window through which the meter was observed. The variations in indicated phase angle with ambient temperature are consistent with those predicted for the meter current generators in Sec. 20.1.

The tests made on the M. S. E. V. substation equipment were more elaborate. After manufacture, the twelve printed circuit boards containing the components shown in Fig. 48, and also the twelve boards carrying the line terminating network shown in Fig. 23, were mounted in an environmental chamber. The boards were supplied with d. c. and pulse signals corresponding to those to be used in service. During approximately eight hours in each day, a temperature cycle of 2 hours at 0^{o}C, followed by 2 hours at 50^{o}C, was followed; the supply voltages were switched "on" during the heating part of the cycle, and "off" when the units were being cooled. For the remainder of the day, the supply voltages were switched "on", and the ambient temperature was that of the laboratory. This sequence of operation was continued for a total time of 1458 hours. A similar programme was carried out for the power supply units: in this case, however, the sequence described above was continued for only 300 hours, and was followed by a 1000-hour "burn-in" at laboratory temperature.

Voltage waveforms at various points in the circuits were noted, both before and after the temperature cycling tests described above. The value of V_{ref}, and also the voltage V_z across the Zener diode D1 (Fig. 48) were measured; the results are given in Table 15. These tests showed a satisfactory stability of all parameters measured.

The 50 Hz test voltage isolating transformers (VT in Fig. 48), were tested for possible phase error in the following manner. The primary windings of all of the transformers under test were connected to a 110V r. m. s. 50 Hz a. c. supply of sinusoidal waveform. To the same supply was connected the inputs of two voltage comparators, similar to FC in Fig. 48. The steps in output voltage of these comparators, corresponding to the positive-going zero crossover of the 50 Hz voltage, were displayed simultaneously on an oscilloscope, and the time difference between them noted : this time difference is nominally zero, but was in fact a small fraction of 1 μsec., due to the tolerance in V_{ref} discussed in Sec. 22. 2.

The input of one comparator was then transferred to the secondary winding of the VT under test, and the change in the time difference between the comparator output voltage steps noted. This change was interpreted as the transformer phase error, and for the twelve transformers tested, did not exceed 0.1 μsec., corresponding to 0.0018 degree at 50 Hz. This is considered to be an adequate performance.

Finally, when the manufacture of all the substation units was complete, each unit was tested at the extremes of the specified range of ambient temperature and supply voltage. The unit under test was mounted in the environmental chamber and connected, via a "Variac" variable voltage transformer, to a 110V 50 Hz supply. A second unit, outside the chamber, was connected directly to the same supply. The pilot line outputs of the units were connected to the corresponding inputs of the Control Centre unit, the meter of which was replaced by an instrument of increased sensitivity. The phase angle indication, nominally zero, was noted for various values of temperature and supply voltage over the ranges 0^{o}C to 50^{o}C, and -15% to +10%, respectively. The maximum deviation from zero of any of the twelve units tested was 1/30 degree of phase angle.

25.1 OVERALL SYSTEM PERFORMANCE TESTS

Two series of tests on the overall performance of the pilot line phase measurement system were made. The first series was conducted by the M. E. B., to assess the accuracy of the system over an extended period, and under conditions of normal operation. Two substation units were mounted in the Stockfield Road, Birmingham, substation, and supplied with test voltages from two V. T. s connected to different power supply circuits within the substation. The substation units were connected, via pilot lines of different lengths, to the Control Centre unit located in the Control Room at Summer Lane, Birmingham. An Ad-Yu type 405 Phasemeter was connected between the same two V.T. s in the substation, allowing an independent measurement of phase angle to be made. The phase angle indicated by the two systems was regularly compared by the operators, using a telephone link between Control Room and sub-station. The results of these tests are given in Appendix C, from which it will be seen that the largest difference in the indicated phase angle was 55'. The specification of the Ad-Yu phasemeter quotes a maximum error of $\pm$ 1°, or 2% of the phase angle indicated. The phasemeter was carefully checked before the tests commenced, but when they were complete it was found that an electrolytic smoothing capacitor associated with the d. c. power supply of the instrument had failed, allowing a considerable ripple to exist on the h. t. supply voltage. Before the capacitor was replaced, therefore, the phasemeter was again checked, but the accuracy appeared to be little impaired by the breakdown. The M. E. B. were satisfied with the results of the tests given in the Appendix.

The second series of tests, carried out in the University laboratory, was to determine the error in the indicated phase angle when various pilot lines were used. Two substation units were fed from a common 110V a. c. supply; the line output of one substation unit was connected to the Control Centre unit via a pilot line supplied by the M. E. B., while for the other substation unit a direct

connection was made. The phase difference $\Delta\phi$, nominally zero, was measured using a Cambridge Unipivot microammeter having a full-scale deflection current corresponding to only 2^{o} phase angle, in place of the meter normally used. The resulting increased sensitivity allowed the errors in phase measurement caused by the different line characteristics to be accurately measured. The value of error $\Delta\phi$ for each of the twelve pilot lines used for the tests described in Sec. 14.3 was measured, and these tests were repeated to measure the error $\Delta\phi'$ when the two inputs to the Control Centre unit were interchanged. The results are given in Table 17, and show that even when using the lines J and K, which are longer than the maximum specified, (see Sec. 14.3), the error is less than $0^{o}07'$ of phase angle. The results also show that the asymmetry between the two input circuits of the Control Centre unit corresponds to a phase angle of less than $0^{o}04'$.

A further test was made to investigate the effect of varying the frequency of the test voltage on the phase angle indication. Two substation units were connected to the Control Centre unit by pilot line and direct connection, as described for the test above. The input test voltages for the substation units were obtained from the calibrator (Sec. 26.2). Using various values of input phase angle, from -25^{o} to $+25^{o}$, the indication on the meter in the Control Centre unit was noted as the input frequency was varied over the range 46-51 Hz. No variation with change in frequency in any of the phase angle indications could be observed.

In addition to the above tests of the accuracy of the system, the level of electrical noise present on the twelve pilot lines installed in the Birmingham Area was measured, after the M.S.E.V. equipment was fully operational. For this test, the 50 Hz input to each substation unit was disconnected, and the noise voltage V_n developed across terminals 7 and 10 (Fig. 27) of the line transformer in the Control Centre unit measured. Of this voltage, an amount equal to 0.45 mV was generated within the Control Centre units

probably by induction from the power supply transformer. The test results are given in Table 18, and show that at the time the measurements were taken, the total noise voltage on any line did not exceed 0.65 mV. The waveform of the noise voltage was carefully scrutinized, to detect any pulse voltages that might be present : no repetitive pulses of significant amplitude were observed on any pilot line.

The d.c. loop resistance r and the time delay t_A of each line are also given in Table 18. The value of t_A was obtained by measurement, at the Control Centre, of the time t_{cc} between the transmission of a secondary pulse, and the reception of a tertiary pulse. Then

$$t_A = \frac{t_{cc} - T_d}{2} \qquad \text{-----} \qquad (25.1.1)$$

where T_d = 5.115 msec., as given in Sec. 7.2.

The results given in Table 18, and also those for the twelve pilot lines given in Table 3, are displayed in Fig. 55, in which time delay is plotted against loop resistance. The circled points refer to Table 3, while the crosses refer to Table 18. It will be seen that for a given line resistance, the variations in delay correspond to a phase angle exceeding 1^o. These experiments provide the evidence for the abandonment of early attempts to deduce the time delay of a line from measurements of its loop resistance.

A record was kept, over a period of several weeks, of the phase angle between voltages in substations at Stockfield Road and Hall Green, Birmingham. Fig. 56 shows the results taken over one day.

26.1 TEST EQUIPMENT

Throughout the development of this system of remote phase measurement, test equipment from the University laboratories was available. The more commonly-used items are given below.

Oscilloscope :	Tektronix type 547, with plug-in units type 1A1, 1A4 and G.
Pulse Generators :	Advance type 5002D.
	Hewlett-Packard type 222A.
Pulse Counter :	Hewlett-Packard type 5245L, with Time Interval Unit type 5262A.
Time Mark Generator :	Tektronix type 180A.
Digital Voltmeter :	Dynamco type DM 022.

In addition, the Ad-Yu type 405 Phasemeter was purchased by the M.E.B. The specification for this instrument quotes an absolute accuracy within $\pm 1^{o}$, or 2% of phase angle indicated; this limited accuracy precluded its use for much of the laboratory development work, although it was valuable as an independent check as described, for example, in Sec. 25.1. To calibrate the equipment a generator of voltage waveforms having an accurately-known phase difference was a necessity, the error in phase preferably not exceeding 1/100 degree. As no commercially-available generator giving the required waveforms to this accuracy was known, it was necessary to develop an instrument for this duty, and this is described in the next Section.

26.2 The Phase Angle Calibrator

This instrument is designed to provide two output voltages of frequency nominally 50 Hz, amplitude approximately 6V peak-to-peak, and "square" waveform symmetrical about earth potential. The relative phase of the voltages may be selected from the values 0, 5, 10, 15, 20 and 25 degrees. In addition, two further outputs give 200 μsec. positive pulses, which coincide with the positive-going edges of the "square" waveform voltages. The amplitude of these pulses is continuously variable from zero to +4V, each output being independently controllable. Between pulses, both output voltages are zero, with respect to earth.

The calibrator serves a dual purpose. The "square-wave" output voltages, when applied to the 50 Hz test input terminals of two substation units, provide test signals of accurately-known phase difference. When used in conjunction with the Control Centre unit, tests of overall system accuracy can then readily be made. The 200 μsec. output voltage pulses, applied to the Control Centre unit line input terminals, may be used to check the accuracy of the current generators and meter in that unit. Suitable resistors connected in series with each 200 μsec. pulse output allow direct connection of the calibrator to the Control Centre unit : these resistors absorb the resulting secondary pulses generated by the latter unit, avoiding damage to the equipment which might otherwise occur. Fig. 57 shows the logic diagram of the calibrator, while Figs. 58 and 59 show the circuit diagram of the unit. A component list is given in Appendix D.

The high accuracy of phase angle generation is achieved by the use of a counting technique. Referring to Fig. 57, the astable multivibrator A oscillates at 3600 Hz. The output Q2 of A triggers a divider chain consisting of the binary dividers B1 and B2, and the ternary dividers T1 and T2. The total division ratio of the chain is 36, and the dividers are thus in the "0" state 100 times per second. The AND gate G2 has inputs connected to each element

in the divider chain, permitting an output only when the elements are all in the "0" state. A further input is connected to the output Q1 of A, which is complementary to Q2. Thus, the output of G2 consists of pulses which have a frequency of 100 Hz, and coincide with the output Q1 of A. The binary divider B4 is triggered from G2, giving an output voltage of "square" waveform, and frequency 50 Hz. This, after amplification by AA, provides one of the calibrator output voltages. A second AND gate G1 is also connected to the divider chain. However, the output from this gate, while coinciding with the Q1 pulses from A, occurs at a time in the cycle of the divider chain later than the output from G2: this time may be selected by the switch S1, which connects the inputs of G1 to the appropriate outputs of the divider chain elements. The output of G1 triggers the binary divider B3, the output voltage of which, after amplification by AB, provides the second 50 Hz "square" waveform output voltage, lagging in phase on the voltage from AA. The AND gates G3 and G4 are provided to ensure that a 180^{o} ambiguity in relative phase between these output voltages cannot exist : the element B3 can be triggered to a given state only if that state has been already attained by B4. The positive-going steps in output voltage from B4 and B3 are used to trigger the monostable elements M1 and M2 which provide, after amplification by AC and AD, the 200 μsec. output voltages.

The circuit design of the calibrator follows the principles given previously in Sections 16, 17 and 19, and many of the circuits are similar to those used in the Control Centre unit. Further description will therefore be limited to the ternary dividers T1 and T2. Each of these dividers may be regarded as three RTL logic elements, the resistor inputs of each element being connected to the outputs of the remaining two elements. Consider the divider T1 in Fig. 58. The transistors TR7-9, together with the associated resistors, comprise the RTL elements. The resistor values are chosen so that at any one time, two transistors are

saturated, while the third is "off". The diode-capacitor gating system causes the negative-going trigger pulses from B2 to be routed to the base of each transistor in turn; the arrangement therefore behaves as a 3-state ring counter.

The power supply circuit is shown in Fig. 59. A commercially-available stabilizer unit is used for the +12V supply; a simple Zener diode stabilizer is adequate for the -12V supply. The current consumption of the calibrator is 150 mA at +12V, and 3 mA at -12V, d.c.

27.1 RADIO LINK SYSTEM

Many of the preceding Sections have been concerned with the design of the remote phase measurement system using pilot lines to convey the phase information from substation to Control Centre. An alternative system has been investigated using a 460 MHz f.m. radio link instead of the pilot line, for use with those substations where no pilot line exists. There would seem to be no reason why a mixed radio link/pilot line system should not be successful, the Control Centre receiving signals from some substations equipped with pilot lines, and from others for which a radio link is fitted. No experimental work on such a mixed system has been done, however.

There are several fundamental differences in the operation of the pilot line and radio link systems. The first difference is in the method of selecting the pair of substations between which the phase measurement is to be made. With the pilot line system a pair of rotary switches is sufficient, but with the radio link system it is necessary to send signals from the Control Centre to select the substations chosen. Further signals are then required to instruct the performance of functions within the substation, such as a change in transmitter frequency, before phase measurement can begin. This is a subject on which work has already been done but, not forming part of the phase measurement system proper, will not be further discussed in this report.

A second difference between the two systems is that whereas a common pilot line is used for the transmission of primary, secondary and tertiary pulses, in the radio link system separate radio frequencies f_T, f_A and f_B are used for the transmissions from the Control Centre, substation A and substation B, respectively.

There is then no need for the substation time delay generator, and the precautions taken in the pilot line substation equipment, to prevent false operation due to feedback of transmitted pulses into the receiving channel, are also unnecessary. The circuits of the radio link substation unit thus become very simple. To offset this advantage, it is unlikely that a separate radio frequency will be available for each substation: if only two frequencies f_A and f_B are allocated for all the substations in an installation, some means of changing the radio frequency transmitted by the substations, by command from the Control Centre, is essential.

An advantage of the radio link system is that the velocity of propagation of the radio waves is constant and, neglecting reflection effects, the path from substation to Control Centre is in a straight line. This eliminates the need for the protection against re-routeing of the pilot lines given by the repetitive transmission delay measurement system described in Sec. 7.3. However, measurements have shown that the time delay caused by the circuits in the U.H.F. transmitter and receiver is considerable, and it is suspected that this time delay may not be constant, due to the variation in the characteristics of the radio equipment between units, and with age and operating conditions. The repetitive delay measurement thus becomes important in correcting for any such variations that may occur. It will be understood that the effectiveness of this correction depends on the assumption of equal delay for transmission in opposite directions, (Sec. 14.3), which was based on experiments made on pilot lines. This assumption does not necessarily hold when separate channels for the two directions are used. It seems likely, therefore, that if commercially-available radio equipment for which no delay value is specified is used, the accuracy of phase angle measurement may be less than that achieved by a pilot line system. No experiments have been made to determine the cause of the delay in the radio units. It is possible that much of the delay is caused by the circuits shaping the frequency response to the communications requirements.

If this is so, a satisfactory consistency of delay between units may be achievable by a suitably close tolerance on the value of the shaping circuit components, and a satisfactory constancy of delay by the use of components of appropriate quality.

The experiments made to measure the time delay in the radio transmitters and receivers were necessarily restricted, owing to the limited number of these units available. Also, it was not possible to measure the delay of a transmitter or receiver alone; the only measurement possible was the total delay from transmitter input to receiver output.

Two Elliot transmitter-receivers using valves, and two Cossor transmitter-receivers using semiconductors were used. The output of a transmitter was applied to the input of a receiver via a suitable attenuator. The total time delay of various combinations of these units was measured, the possible variations being limited by the crystal frequencies available. Initially, the units were adjusted to the appropriate communications specification. The transmitter inputs were supplied with 1V 200 μsec. pulses from a pulse generator. The receiver gain controls were adjusted to give an output voltage of 1V peak, and this voltage was applied to the input of a voltage comparator adjusted to operate at 0.5V. The time delay between the leading edge of the transmitter input pulse and the instant of voltage comparator operation was measured, and the results are given in Table 19. The greatest difference in the delay times is 16 μsec., which would cause an error of 0.14^{o} in the phase angle measurement.

To determine the feasibility of phase measurement using a radio link, a Control Centre unit similar to that shown in Fig. 38 was constructed. The outputs of two 460 MHz receivers, tuned to f_A and f_B, were connected to the unit in place of the line transformers A1 and B1 shown in the Figure. The input to the transmitter, tuned to f_T, was taken from the collector of TR25, via a resistive potential divider adjusted to suit the transmitter input

signal level specified. No line transformers or coupling networks were, of course, required. Two substation units were constructed, similar to that shown in Fig. 48. The outputs of two 460 MHz receivers, both tuned to f_T, were connected to the units in place of the line transformers LT, while the two transmitter inputs were connected, via suitable potential dividers, to the collector of D. One transmitter was tuned to f_A, and the other to f_B. Apart from those mentioned above, no further modifications to the pilot line units were made, to convert them for use with the radio link, although a much simpler unit could have been designed. Additional circuits were included, however, to prove the feasibility of the substation selection and command functions : these form the subject of a separate report.

The substation units were fitted in substations at Hall Green and Stockfield Road, Birmingham, in which pilot line units were already operating. The two units in each substation were connected to a common 50 Hz test voltage. Aerials were erected at the sub-stations, and on the roof of the University building. The two Control Centre units were mounted adjacent to each other in the laboratory, allowing a rapid comparison of the phase angle indications to be made.

At frequent intervals, extending over a period of several weeks, the phase angle measured on the pilot line system was compared with that measured using the radio link equipment. The discrepancy between the results of the two measurements was never greater than 0.1° in phase angle. The operation of the equipment was demonstrated to representatives of the Electricity Council and the M. E. B., who expressed satisfaction with the results.

28.1 CONCLUSION

A system has been developed for the measurement of phase angle between voltages situated at points remote from each other, and from the point where the results of the measurement are displayed. Compensation is made automatically for the transmission delay of the signals which, if this compensation were not made, would cause a serious error in the measurement. Although the system is primarily intended for operation at 50 Hz, the same principles could be used to enable the measurement to be made at frequencies other than this value. Two versions of the system have been developed, one version uses pilot lines for the connections between the voltages to be measured and the measurement display point, the other version uses a radio link for this purpose. The pilot line system equipment has been fully developed, and installed in the Birmingham Area: the radio link system equipment has been developed as a feasibility model only.

The performance of the pilot line equipment satisfies, and in most cases exceeds, the specification given in Sec. 3.1. Theoretical considerations predict, and experiments confirm, that the accuracy of phase measurement is within a small fraction of one degree, using the pilot lines typically in use by the M. E. B. The maximum permissible length of pilot line depends upon the line characteristics, the allowable signal level, and the electrical noise induced in the line. It is possible, by a simple adjustment of a reference voltage, to modify the equipment performance to effect a compromise between maximum length of line, accuracy of measurement, and degradation of performance caused by electrical noise induced in the line. With the requirement of 12 miles maximum line length required by the M. E. B., a satisfactory compromise has been readily achieved. On installation, no setting-up adjustments are necessary, and regular recalibration is not required. No adjustment to suit individual pilot lines is needed, and an accurate knowledge of the line characteristics is

unnecessary. The phase angle measurement may be made without any preliminary checking procedure, and, apart from the switches selecting the points chosen for phase comparison, no controls, or preset components, are used.

The equipment has been designed inherently to possess a high degree of reliability. With very few exceptions, malfunction of any part of the equipment, or failure or reversal of the pilot lines, causes a warning signal to be given. Considerable deterioration in the characteristics of the pilot lines can occur before the accuracy of measurement is significantly impaired. The installation has been in operation in the Birmingham Area for several months, and prototype installations for many months, without an equipment failure. In addition, long-term tests of vital circuits have been conducted over periods extending to several years.

The radio link equipment was developed to a stage where it could be operated side-by-side with the pilot line equipment, to compare the measurements made by both systems under operational conditions. The results of these tests show that the radio link system is a satisfactory alternative to the pilot line system.

During the development work, it was found necessary to design certain items of specialized test gear, one of which, the phase-angle calibrator, will be required to check the equipment in the field.

In any project, there comes a time when development has to cease, and production begin. In most cases this occurs at a stage in the development well short of that considered desirable by the project leader. In this, the present project was no exception. Further development would undoubtedly improve the equipment. The Control Centre unit is a modified version of the original prototype; a redesign of this unit would probably yield a useful increase in accuracy and simplicity. The results of the tests on

the pilot lines provided by the M. E. B., at a late stage in the project, indicate that a small improvement in accuracy should be achievable by a redesign of the pilot line transformers. Perhpas the greatest benefit from further design work would accrue from an investigation into a possible relaxation in the specification for the power supply units in the substation equipment, to reduce their cost and complexity.

There are many alternatives to the present system which might usefully be investigated. Some of these have already been mentioned; the methods of substation time delay measurement outlined in Sec. 7.3 are an example. There is a scarcity of information on the electrical noise occurring on pilot lines : a greater knowledge of this would probably allow an increase in the maximum permissible length of pilot line. For applications requiring a very long pilot line, there appears to be no reason why repeaters should not be used, provided that the time delay to signals transmitted in both directions could be equalized : the problems associated with such a system could usefully be investigated.

Although the measurement of phase angle by detecting the instant of zero voltage crossover is acceptable for this project, the presence of harmonics in the test voltage may cause a substantial error in a measurement made in this way. If a measurement is required when voltages containing an appreciable harmonic content are to be used, there is a need for the development of circuits responding to the fundamental component of the voltage only.

The principles which have been developed for this project on remote phase measurement have potential for wider application. The time interval between the occurrence of a single pair of events can be measured at an arbitrary point, by measurement of the relative times of arrival of signals generated at the time of the

events, and subsequently applying a correction found by measurement of the difference in the transmission delay times. An example of this application might be in the measurement of seismic waves. Another use of the principles would enable the generation, from a given location, of signals arriving at arbitrarily distant points with a known separation in time. This would be accomplished by a measurement of the transmission delay time difference before the signals were transmitted, and using this to control the relative times of transmission to the distant points. An example of this application is the establishment of a system of national synchronizing signals, with transmission of the signals over the public telephone network.

29.1 ACKNOWLEDGEMENTS

This project is a example of cooperation between Industry and University. The author would like to express his gratitude to the M. E. B., who initiated the project, and who have given constant encouragement throughout its prosecution; also to the Electricity Council, who provided most of the financial support. The author would also like to thank the members of the M. E. B. staff, Tony Blackmore, Keith Horton, and Clive Marklew, and especially Cyril Hart, for their devoted toil in constructing and testing the equipment.

APPENDIX "A"

COMPONENT LIST FOR CONTROL CENTRE UNIT

Component numbers refer to circuit diagram, Fig. 38.

RESISTORS Electrosil type TR5, metal oxide, 2% tolerance

Component No.	Value, ohms	Component No.	Value, ohms	Component No.	Value, ohms
R1	2.2k	R24	56k	R46	100k
R2	270k	R25	100k	R47	4.7k
R3	2.2k	R26	1.2k	R48	270
R4	270	R27	270k	R49	3.9k
R5	10k	R28	12k	R50	3.9k
R6	39k	R29	100k	R51	56
R7	1.8k	R30	680k	R52	220
R8	1.2k	R31	15k	R53)	adjust on
R9	1.2k	R32	1.2k	R54)	test
R10	2.7k	R33	100k	R56	3.9k
R11	27k	R34	100k	R57	3.9k
R12	3.9k	R35	270k	R58	56
R13	1.8k	R36	1.2k	R60	270
R15)	adjust on	R37	12k	R61	220
R16)	test	R38	100k	R62)	adjust on
R17	12k	R39	10k	R63)	test
R18	3.3k	R40	10k	R64	10k
R19	3.3k	R41	100k	R65	1.2k
R20	680k	R42	1.2k	R66	10k
R21	56k	R43	10k	R67	1.2k
R22	15k	R44	10k	R68	10k
R23	1.2k	R45	1.2k	R69	100k

Component No.	Value, ohms	Component No.	Value, ohms	Component No.	Value, ohms
R70	10k	R103	33k	R136	1.2k
R71	100k	R104	15k	R137	12k
R72	470	R105	2.2k	R138	12k
R73	100k	R106	100k	R139	150k
R74	100k	R107	1.2k	R140	33k
R75	10k	R108	270k	R141	2.2k
R76	470	R109	1.2k	R142	100k
R77	100k	R110	100k	R143	680k
R78	100k	R111	12k	R144	100k
R79	10k	R112	2.2k	R145	15k
R80	270k	R113	270k	R146	100k
R81	10k	R114	10k	R147	1.2k
R82	100k	R115	2.2k	R148	12k
R83	1.2k	R116	270	R149	270k
R84	1.2k	R117	39k	R150	1.2k
R85	15k	R118	1.8k	R151	2.2k
R86	100k	R119	1.2k	R152	100k
R87	2.2k	R120	1.2k	R153	150k
R88	150k	R121	2.7k	R154	33k
R90	33k	R122	27k	R155	150k
R91	1.2k	R123	39k	R156	15k
R92	33k	R124	1.8k	R157	33k
R93	2.2k	R126)	adjust on	R158	2.2k
R94	100k	R127)	test	R159	100k
R95	12k	R128	12k	R160	1.2k
R96	12k	R129	3.3k	R161	1.2k.
R97	1.2k	R130	3.3k	R162	270k
R98	33k	R131	680k	R163	12k
R99	2.2k	R132	56k	R164	100k
R100	100k	R133	56k	R165	56k
R101	150k	R134	1.2k	R166	100k
R102	150k	R135	100k	R167	270k

Component No.	Value, ohms
R168	22k
R169	22k
R170	2.7k
R171	220
R172	100k
R173	220
R174	100k
R175	270k
R176	2.7k
R177	47k
R178	220
R179	220
R180	470
R181	470
R182	470
R183	470
R184	4.7k
R185	4.7k
R186	4.7k
R187	4.7k
R188	1.5k
R189	1.5k
R190	1.5k
R191	1.5k
R192	100k

RESISTOR Electrosil type C5, metal oxide, 1% tolerance

Component No. R55; value 50 ohms.

RESISTORS Electrosil type TR5, metal oxide, 1% tolerance

Component Nos. R14, R59, R125; value 560 ohms.

CAPACITORS Polystyrene film, Salford Electrical Instruments type RPF, 2.1/2% tolerance 125V d.c. working.

Component No.	Value,
C3	0.64 μF
C4	0.11 μF
C9	0.02 μF
C10	270 pF
C11	270 pF
C12	270 pF
C13	270 pF
C14	0.73 μF
C17	270 pF
C18	0.37 μF
C19	270 pF
C20	0.22 μF

CAPACITORS Metallised polyester film, Mullard type C281, 10% tolerance, 250V d.c. working

Component No.	Value
C1	0.01 μF
C2	0.01 μF
C7	0.1 μF
C8	0.1 μF
C15	0.01 μF
C16	0.01 μF
C21	1 μF
C22	1 μF
C23	1 μF

CAPACITORS Tantalum electrolytic, Plessey type TAHSL.

Component Nos. C5, C6; value 47 μF, 75V d.c. working, ref. no. 402/8/50032/004.

CAPACITORS Electrolytic, Mullard.

Component Nos. C24, C25, value 16 μF, 64V d.c. working, type C428AR/H16.

TRANSISTORS Silicon Planar, SGS-Fairchild Ltd.

Component Nos. TR1-TR10, type 2N2484.

Component Nos. TR11-TR12, type BFY 64.

Component Nos. TR13-TR16, type BFY 56A.

All other transistors type 2N914.

INDICATING LAMPS Thorn.

Component Nos. PL1-PL2, 6V 40 mA rating, ref SGF9/A.

DIODES Zener, Mullard Ltd.

Component Nos. D1-D3, type BZY78 reference diode.

Component Nos. D4-D5, type BZY88 C6V8 stabilizer diode.

DIODES Silicon, SGS-Fairchild Ltd.

All diodes not mentioned above, type 1N914.

PILOT LINE PULSE TRANSFORMERS

Gardners Transformers Ltd., type GR 69361.

METER Ernest Turner Electrical Instruments Ltd.

Type 455LS/150461, 500-0-500 μA centre zero.

Max. error 0.5% F.S.D., over range 10^{o}C to 40^{o}C.

APPENDIX "B"

COMPONENT LIST FOR SUBSTATION UNIT

Component numbers refer to circuit diagram Fig. 48.

RESISTORS Metal oxide, Electrosil type TR5, 2% tolerance

Component No.	Value, ohms	Component No.	Value ohms	Component No.	Value ohms
R2)	adjust on	R11	10k	R18	220
R3)	test	R12	1.5k	R19	3.3k
R4	12k	R13	680	R20	1k
R8	10k	R14	1.5k	R21	100
R9	470	R15	100	R22	100
R10	470	R16	5.6k	R23	10k
				R24	47k

RESISTORS Metal oxide, Electrosil type TR5, 1% tolerance

Component No. R1, value 560 ohms.

Component No. R5, value 22 kohms.

RESISTORS Metal oxide, Electrosil type TR6, 1% tolerance

Component No. R6, two resistors each of value 11 kohms.

Component No. R17, value 470 ohms.

CAPACITORS Polystyrene film, Salford Electrical Instruments type RPF, 2.1/2% tolerance, 125V d.c. working.

Component No. C1, value 2200 pF.

Component Nos. C2, C4, value 4700 pF.

CAPACITORS Metallised polyester, Mullard type C281, 10% tolerance, 250V d.c. working.

Component No. C3, value 0.15μF.

Component Nos. C5-C9, value 1 μF.

TRANSISTORS Silicon planar, SGS-Fairchild

Component D, type 2N914.

Component T, type BFY 56A.

DIODES Zener, Mullard

Component D1, type BZY78.

Component D7, type BZY88 C6V8.

DIODES Silicon, SGS-Fairchild

All diodes, except Zener diodes, type 1N914.

INTEGRATED CIRCUITS SGS-Fairchild

Components LC, FC and X, type 5771039.

Components B0-B9, type 5992629P.

Component A, type 5991529P.

QUARTZ CRYSTAL Salford Electrical Instruments

5° RX element in evacuated glass holder type QC 855, frequency 100 kHz $\pm$ 0.01%.

PILOT LINE TRANSFORMER Gardners Transformers

Component LT, type GR 69361.

VOLTAGE TRANSFORMER Crompton Parkinson

Component VT, 110/110V, 0.6VA burden, phase angle error not exceeding 5 minutes.

LINE COUPLING NETWORK

Similar to that used in Control Centre unit, Fig. 38, with components as specified in Appendix "A".

APPENDIX "C"

Date 1968	Time	Phase angle indication at Substation	Control Centre	Difference
8 Jan.	1630	$0^{o}10'$	$-0^{o}40'$	50'
9 Jan.	1000	$0^{o}10'$	$-0^{o}30'$	40'
10 Jan.	0842	$0^{o}20'$	$-0^{o}10'$	30'
11 Jan.	0830	$0^{o}15'$	$-0^{o}40'$	55'
	0839	$0^{o}15'$	$-0^{o}20'$	35'
12 Jan.	1630	$-1^{o}10'$	$-1^{o}45'$	35'
15 Jan.	0833	$2^{o}40'$	$2^{o}20'$	20'
	1632	$2^{o}00'$	$1^{o}40'$	20'
16 Jan.	0831	$3^{o}00'$	$2^{o}40'$	20'
	1631	$2^{o}10'$	$1^{o}55'$	15'
17 Jan.	0832	$2^{o}30'$	$2^{o}10'$	20'
	1630	$2^{o}40$	$2^{o}20'$	20'
18 Jan.	1635	$1^{o}20'$	$1^{o}00'$	20'
19 Jan.	0830	$2^{o}55'$	$2^{o}30'$	25'
	0840	$3^{o}00'$	$2^{o}50'$	10'
	0850	$2^{o}55'$	$2^{o}40'$	15'
	0900	$3^{o}00'$	$2^{o}40'$	20'
	0910	$3^{o}00'$	$2^{o}40'$	20'
	0920	$2^{o}50'$	$2^{o}30'$	20'
	0930	$2^{o}45'$	$2^{o}25'$	20'
	0940	$2^{o}50'$	$2^{o}30'$	20'
	0950	$2^{o}40'$	$2^{o}15'$	25'
	1000	$2^{o}50'$	$2^{o}30'$	20'
	1010	$2^{o}45'$	$2^{o}25'$	20'
	1020	$2^{o}25'$	$2^{o}15'$	10'
	1030	$2^{o}50'$	$2^{o}40'$	10'
	1040	$2^{o}45'$	$2^{o}30'$	15'
	1050	$2^{o}40'$	$2^{o}20'$	20'
	1100	$2^{o}40'$	$2^{o}20'$	20'
	1110	$2^{o}40'$	$2^{o}30'$	10'

Appendix "C" continued.

1120	$2^{o}40'$	$2^{o}20'$	20'
1130	$2^{o}40'$	$2^{o}20'$	20'
1140	$2^{o}50'$	$2^{o}40'$	10'
1150	$2^{o}40'$	$2^{o}20'$	20'
1200	$2^{o}40'$	$2^{o}20'$	20'
1210	$2^{o}20'$	$2^{o}10'$	10'
1220	$2^{o}20'$	$2^{o}10'$	10'
1230	$2^{o}40'$	$2^{o}20'$	20'
1240	$2^{o}40'$	$2^{o}20'$	20'
1250	$2^{o}30'$	$2^{o}10'$	20'
1300	$2^{o}30'$	$2^{o}20'$	10'
1310	$2^{o}55'$	$2^{o}40'$	15'
1320	$2^{o}50'$	$2^{o}40'$	10'
1330	$2^{o}50'$	$2^{o}40'$	10'
1340	$3^{o}00'$	$2^{o}45'$	15'
1350	$2^{o}35'$	$2^{o}20'$	15'
1400	$2^{o}50'$	$2^{o}40'$	10'
1410	$3^{o}00'$	$2^{o}45'$	15'
1420	$3^{o}15'$	$2^{o}55'$	20'
1430	$3^{o}15'$	$3^{o}00'$	15'
1440	$2^{o}55'$	$2^{o}45'$	10'
1450	$2^{o}50'$	$2^{o}35'$	15'
1500	$3^{o}10'$	$2^{o}55'$	15'
1510	$3^{o}00'$	$2^{o}45'$	15'
1520	$2^{o}40'$	$2^{o}25'$	15'
1530	$2^{o}50'$	$2^{o}25'$	25'
1540	$2^{o}40'$	$2^{o}20'$	20'
1550	$2^{o}40'$	$2^{o}25'$	15'
1600	$2^{o}40'$	$2^{o}25'$	15'
1610	$2^{o}00'$	$1^{o}40'$	20'
1620	$1^{o}35'$	$1^{o}15'$	20'

APPENDIX "D"

COMPONENT LIST FOR PHASE ANGLE CALIBRATOR

Component numbers refer to circuit diagrams Figs. 58 and 59.

RESISTORS Metal oxide, Electrosil type TR5, 2% tolerance.

Component No.	Value, ohms	Component No.	Value, ohms
R1-R11, R15-R16	1k	R150	33k
R17-R18	270k	R151	150k
R19	330	R152-R155	12k
R20-R27	220	R156-R157	270k
R31-R37	12k	R158-R159	1k
R38	10k	R160-R161	3.3k
R39-R50, R54-R65	100k	R162-R163	180
R66-R75, R79-R84	2.2k	R164	33k
R85-R88	15k	R165	150k
R89-R97	1.2k	R166-R171	220
R98-R101	33k	R202	Adjust on test
R102-R113, R120-R127	56k	R203	5.6k
R128-R139, R146-R147	56k	R204	100
R148-R149	22k	R205	270
		R206	220

RESISTORS Metal oxide, Electrosil

Component No. R201, value 25 ohms, consisting of four type TR5 resistors in parallel, each 100 ohms 2% tolerance.

CAPACITORS Polystyrene film, Salford Electrical Instruments type RPF, 125V d.c. working

Component Nos. C1 - C2, value 0.013 μF, 1% tolerance.

Component Nos. C3 - C12, C16 - C21, value 270 pF, 2.1/2% tolerance.

Component Nos. C22 - C23, value 0.02 μF, 2.1/2% tolerance.

CAPACITORS Metallised polyester, Mullard type C281, 10% tolerance, 250V d.c. working

Component Nos. C24 - C25, value 0.01 μF.

Component Nos. C28 - C29, value 1 μF.

Component Nos. C102 - C103, value 0.1 μF.

Component No. C104, value 0.47 μF.

CAPACITORS Electrolytic, Mullard type C428

Component Nos. C26 - C27, value 50 μF, 40V d.c. working, ref. no. C428AR/G50.

CAPACITORS Electrolytic, Mullard

Component Nos. C105-C106, value 2800 μF, type C432FR/J 2800

Component No. C107, value 1400 μF, type C432 FR/H 1400.

CAPACITOR Polyester, Dubilier type 470

Component No. C101, value 0.01 μF, 300V a.c. working, ref. no. 14232.

TRANSISTORS Silicon planar, SGS-Fairchild

Component Nos. TR1-TR2, type V405A.

All other transistors, type 2N914.

DIODES Zener

Component Nos. D1-D2, Mullard type BZY88 C6V2.

Component No. D105, International Rectifier type IZ12.

DIODES Silicon

Component Nos. D101-D104, Mullard type BYX22/400.

All others except those above mentioned, SGS-Fairchild type 1N914.

POTENTIOMETERS Wirewound, Reliance type MW

Component Nos. VR1-VR2, value 100 ohms.

VOLTAGE STABILIZER Roband Electronics

Component VS, type EPS2.

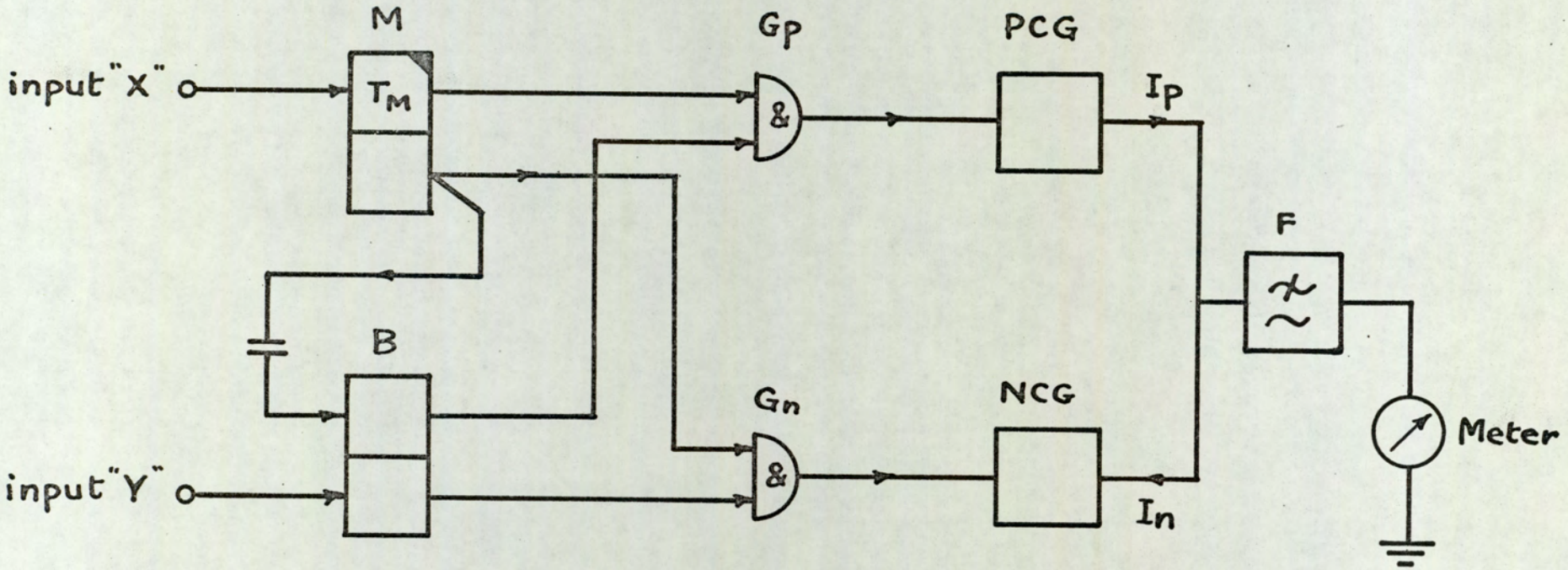


Fig. 1 Phase Angle Measurement

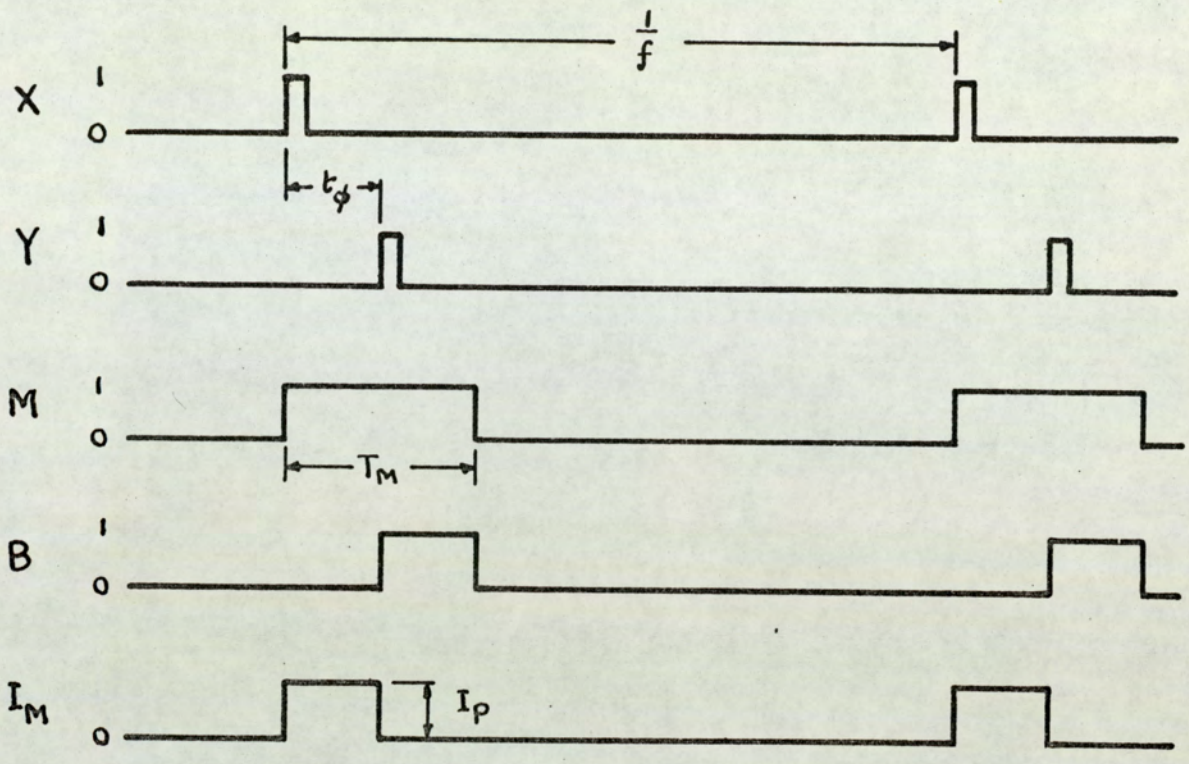


Fig. 2. X leads Y

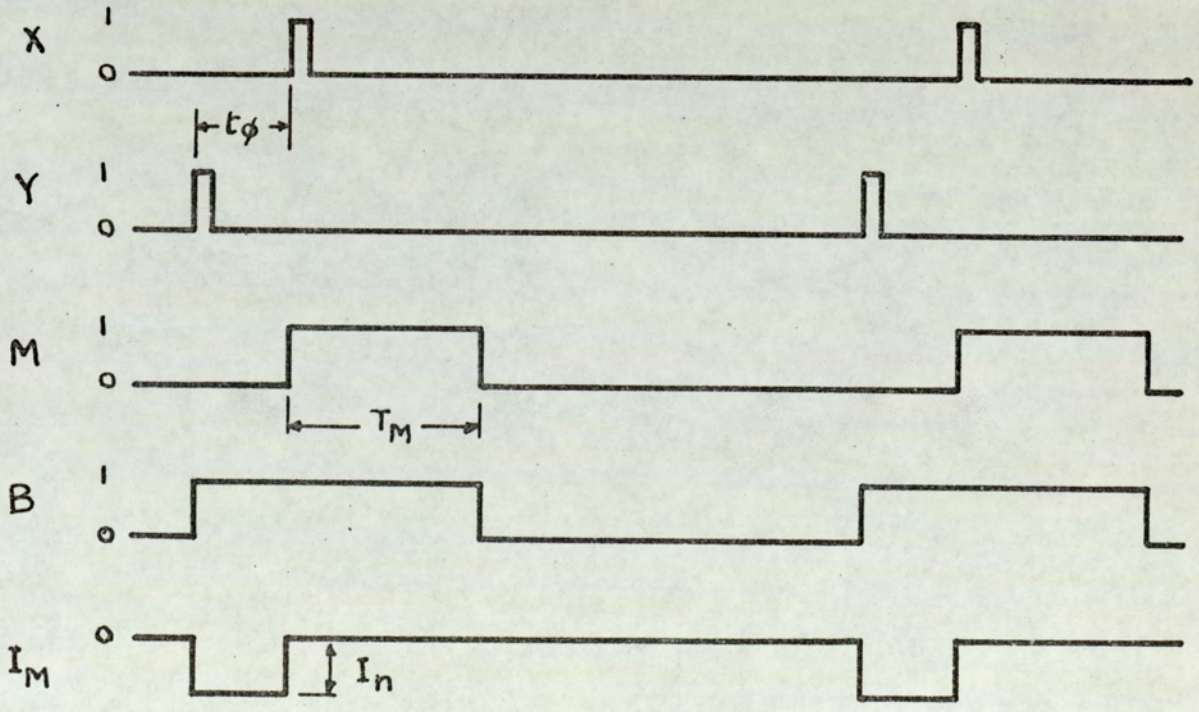


Fig. 3. Y leads X

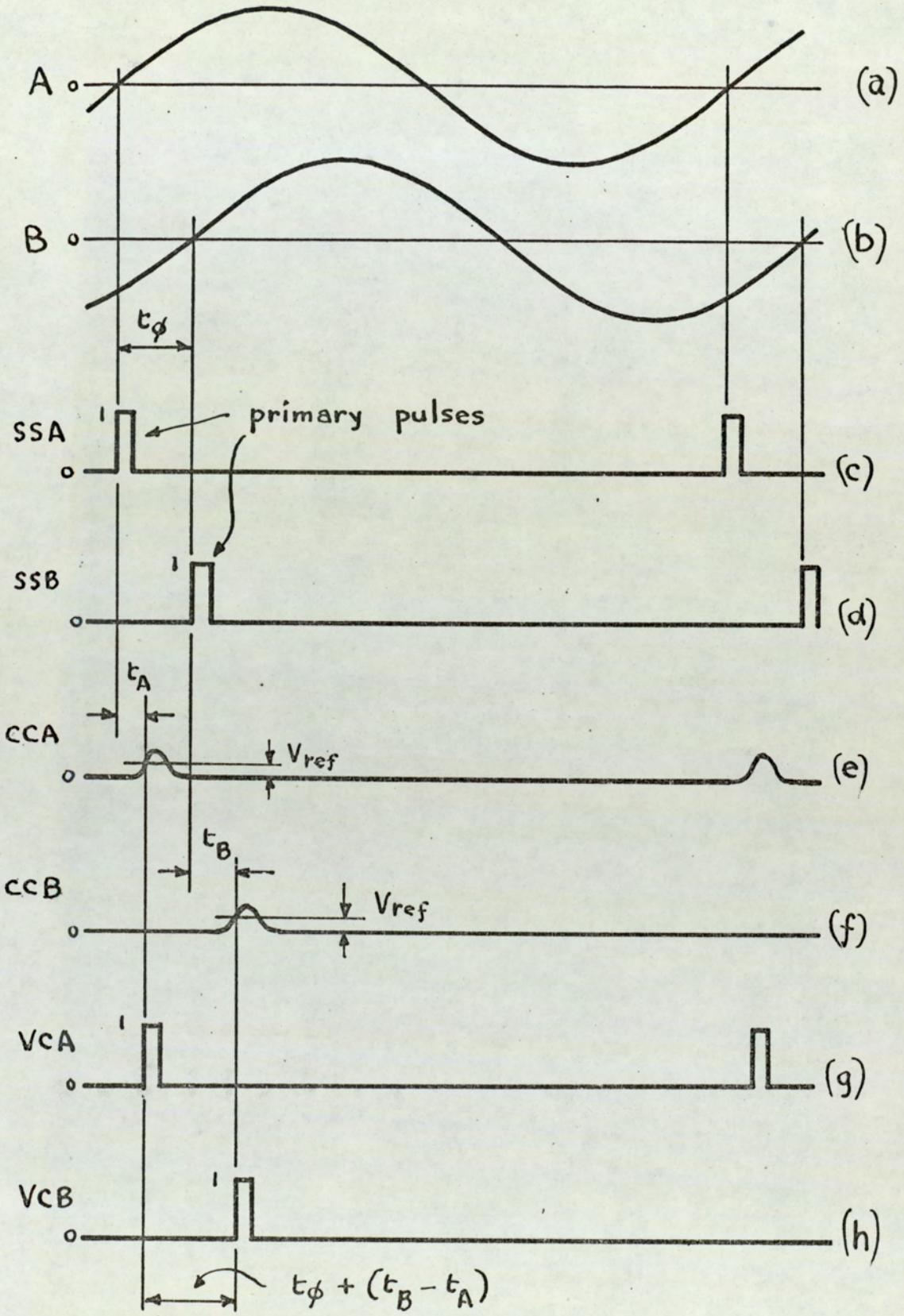


Fig. 4. System Waveforms

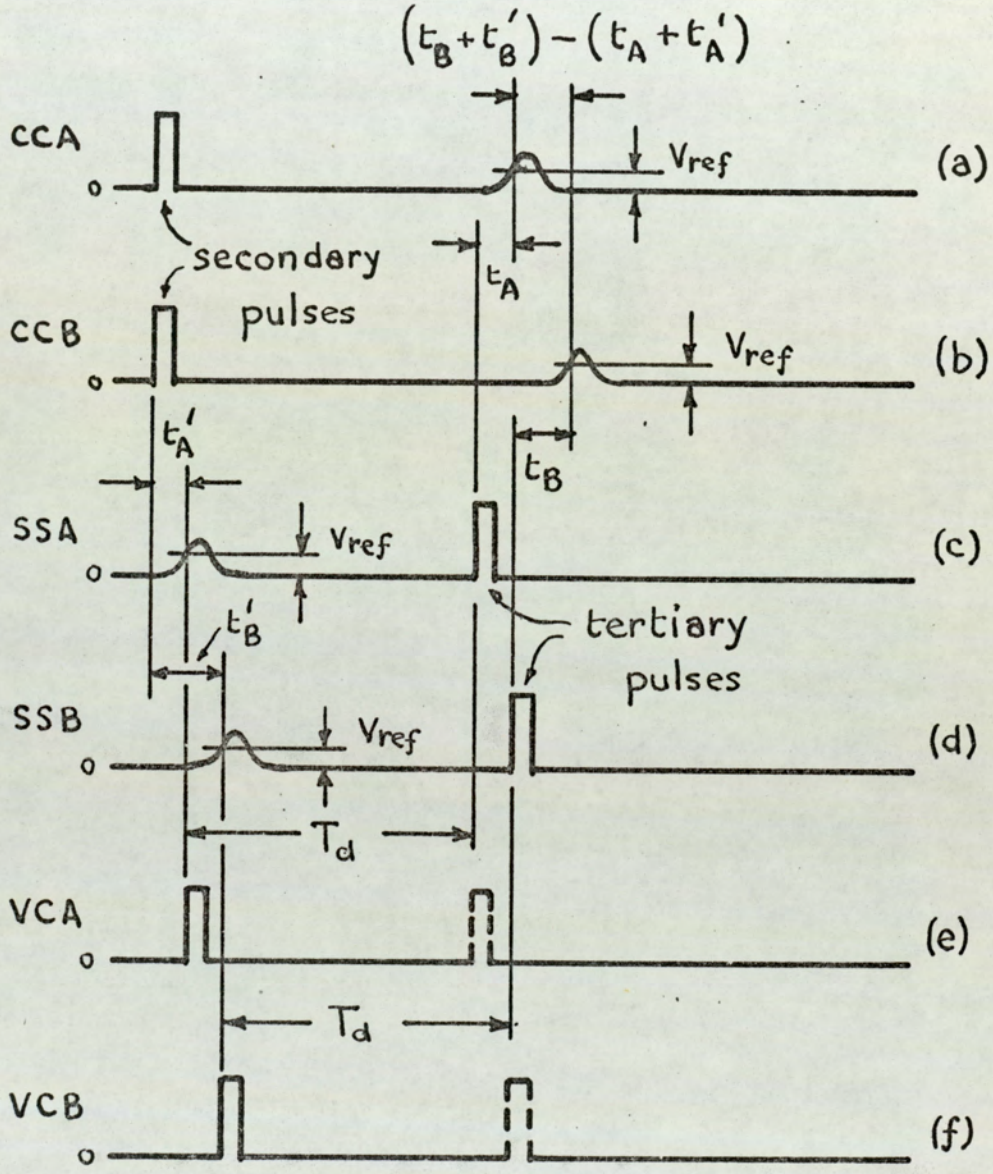


Fig. 5.

System Waveforms

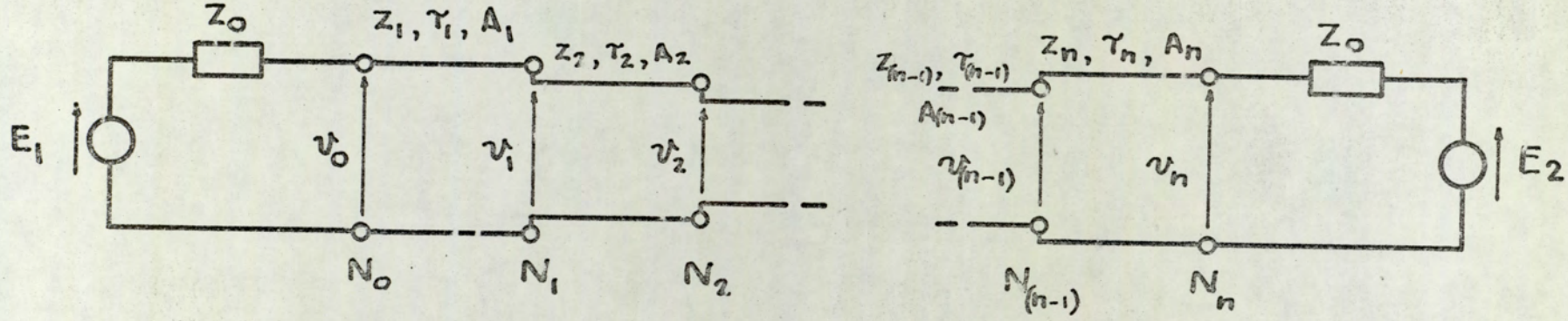


Fig. 5A. Composite Line

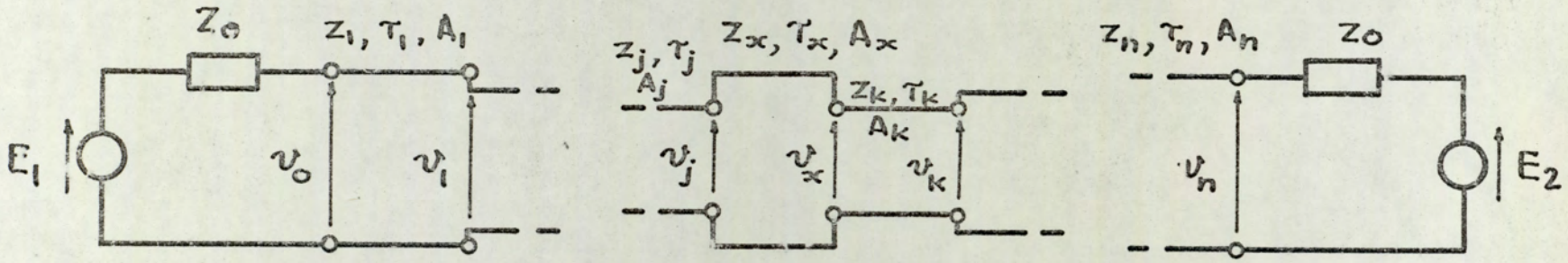


Fig. 5B. Composite Line, with section added

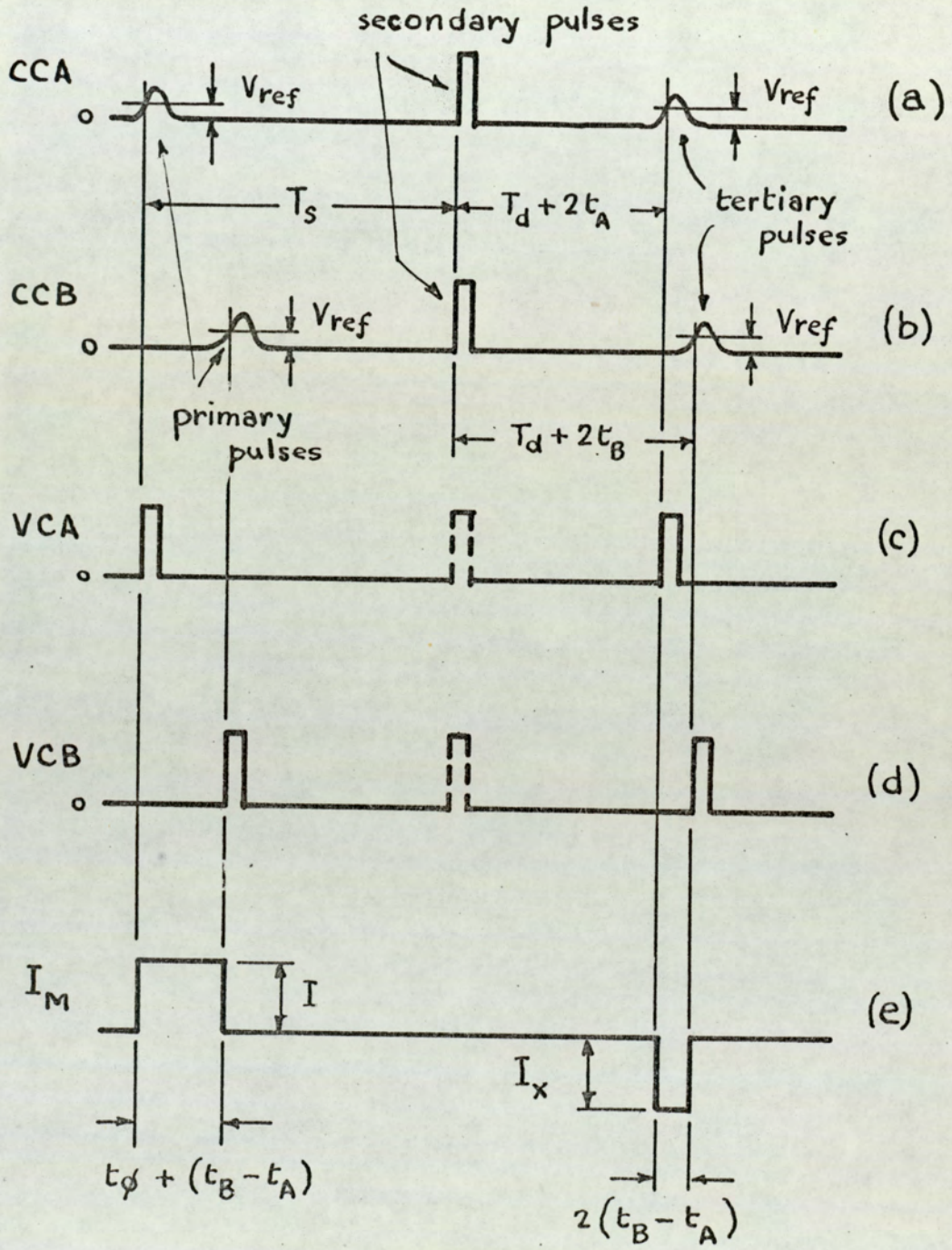


Fig. 6 System Waveforms

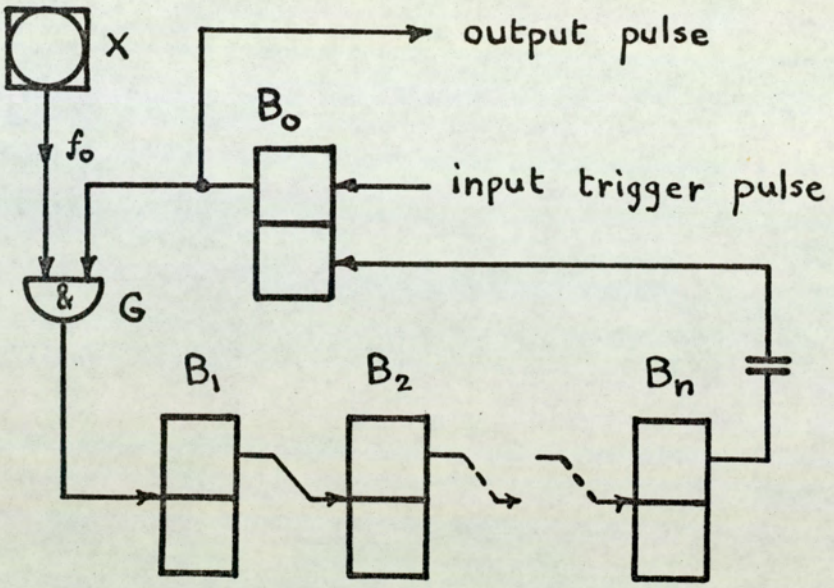


Fig. 7

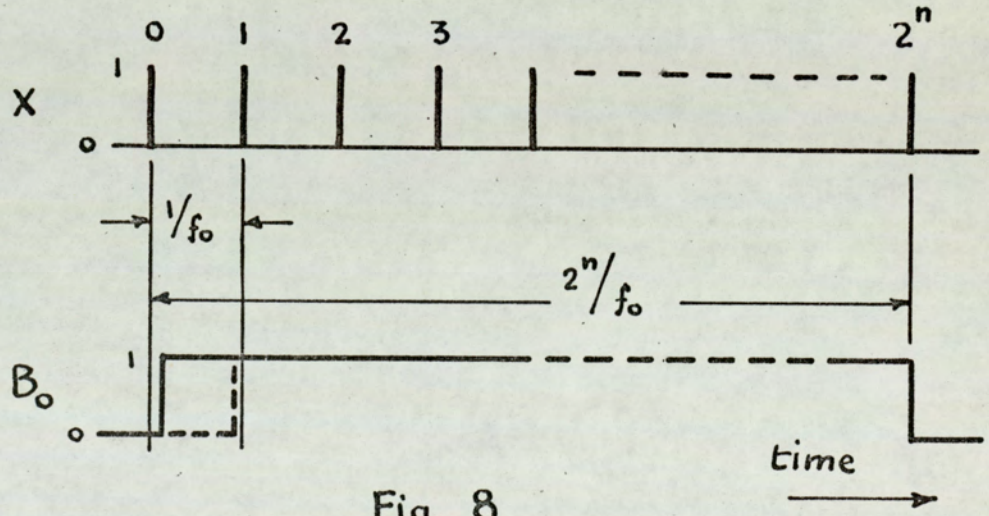


Fig. 8

Time Delay Generator

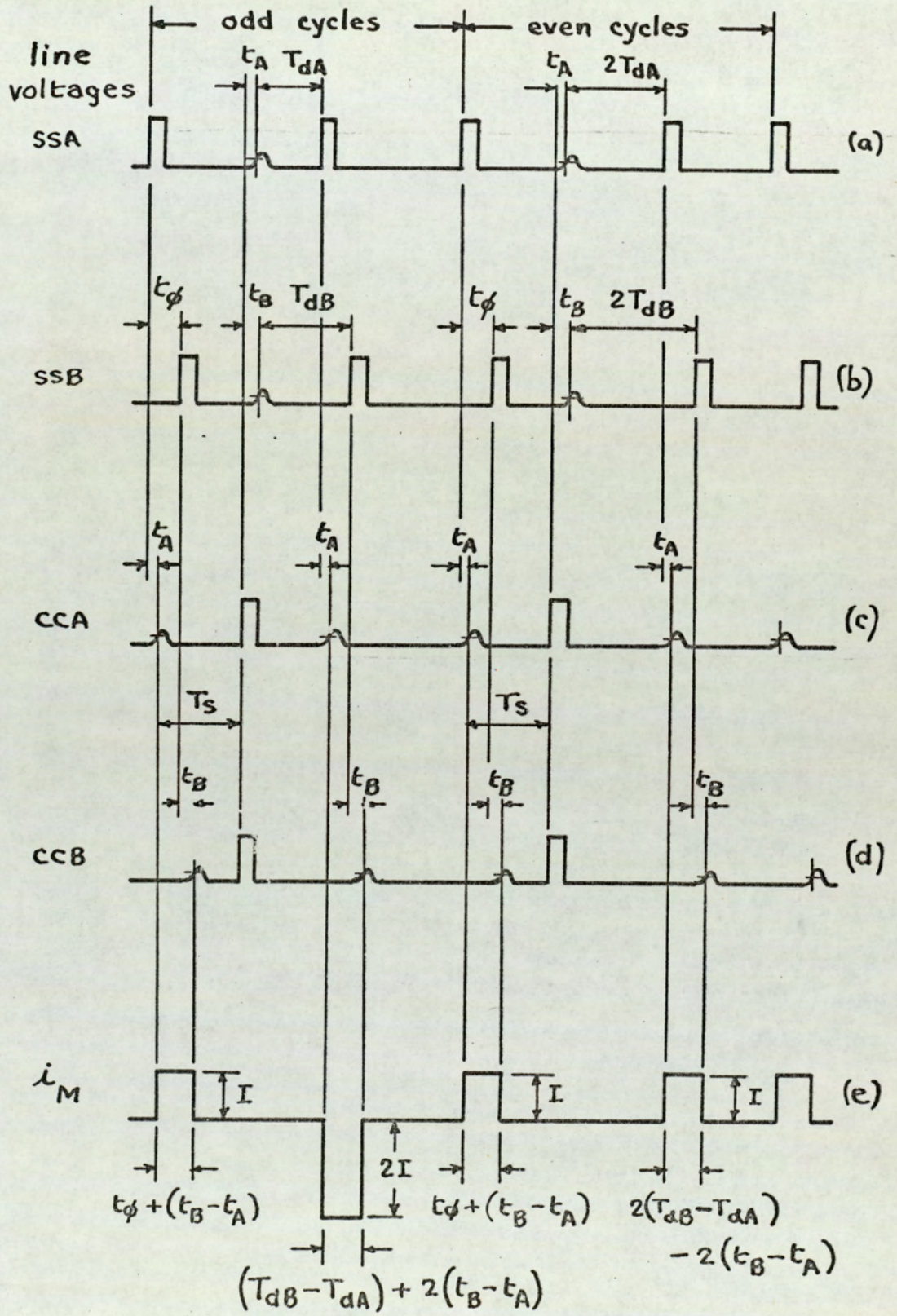


Fig. 9 Waveforms of possible alternative system

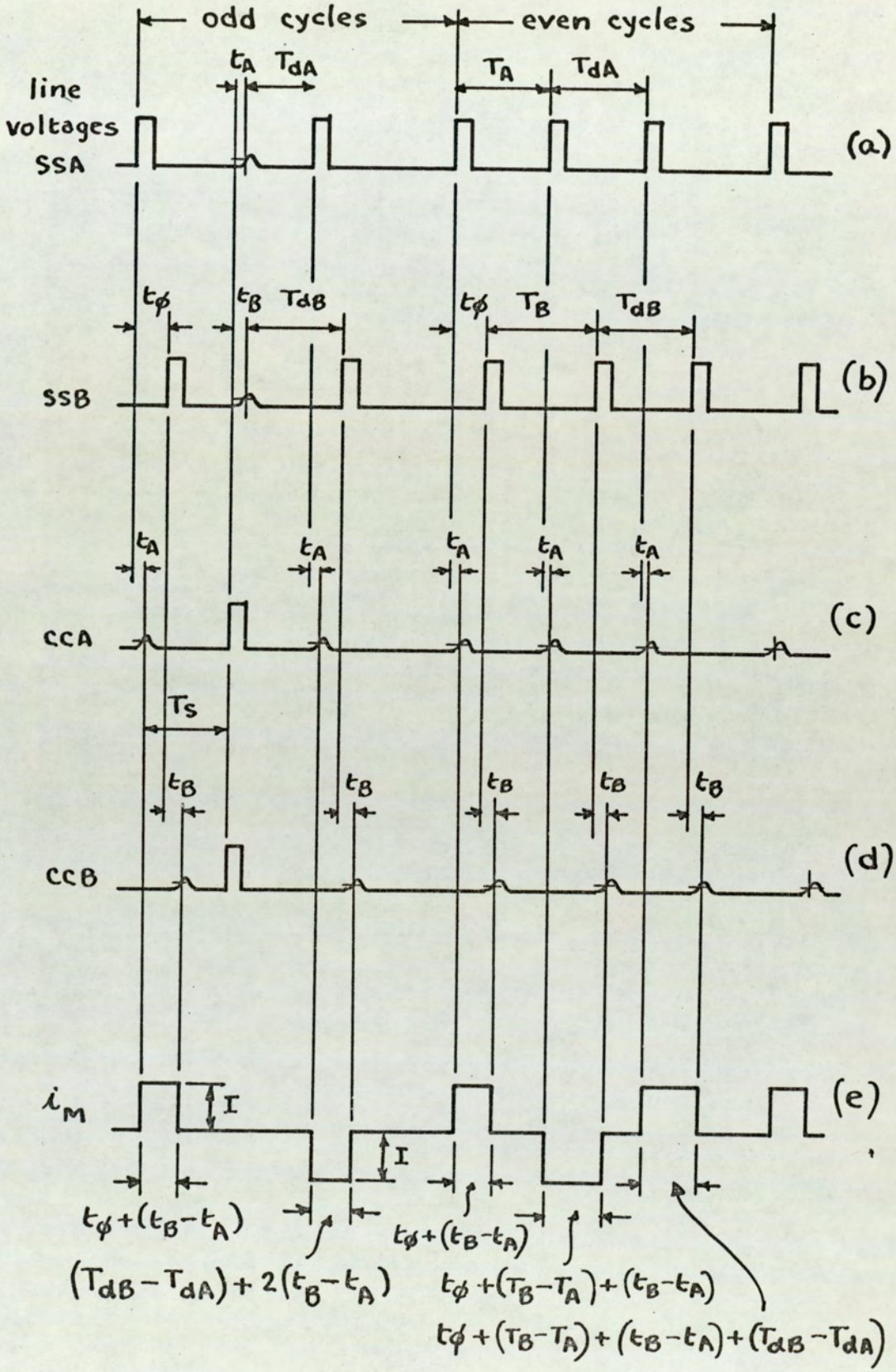


Fig. 10 Waveforms of a possible alternative system

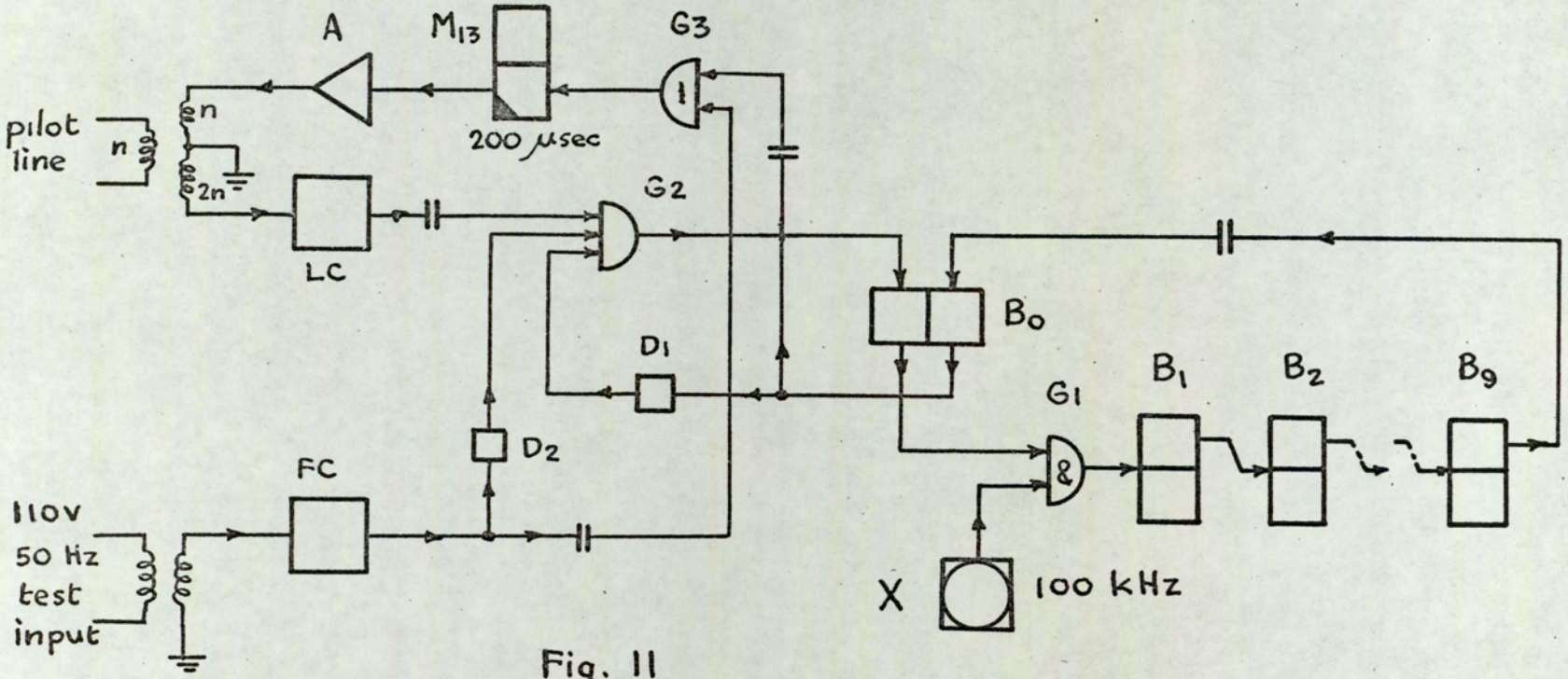


Fig. 11

Substation Logic Diagram

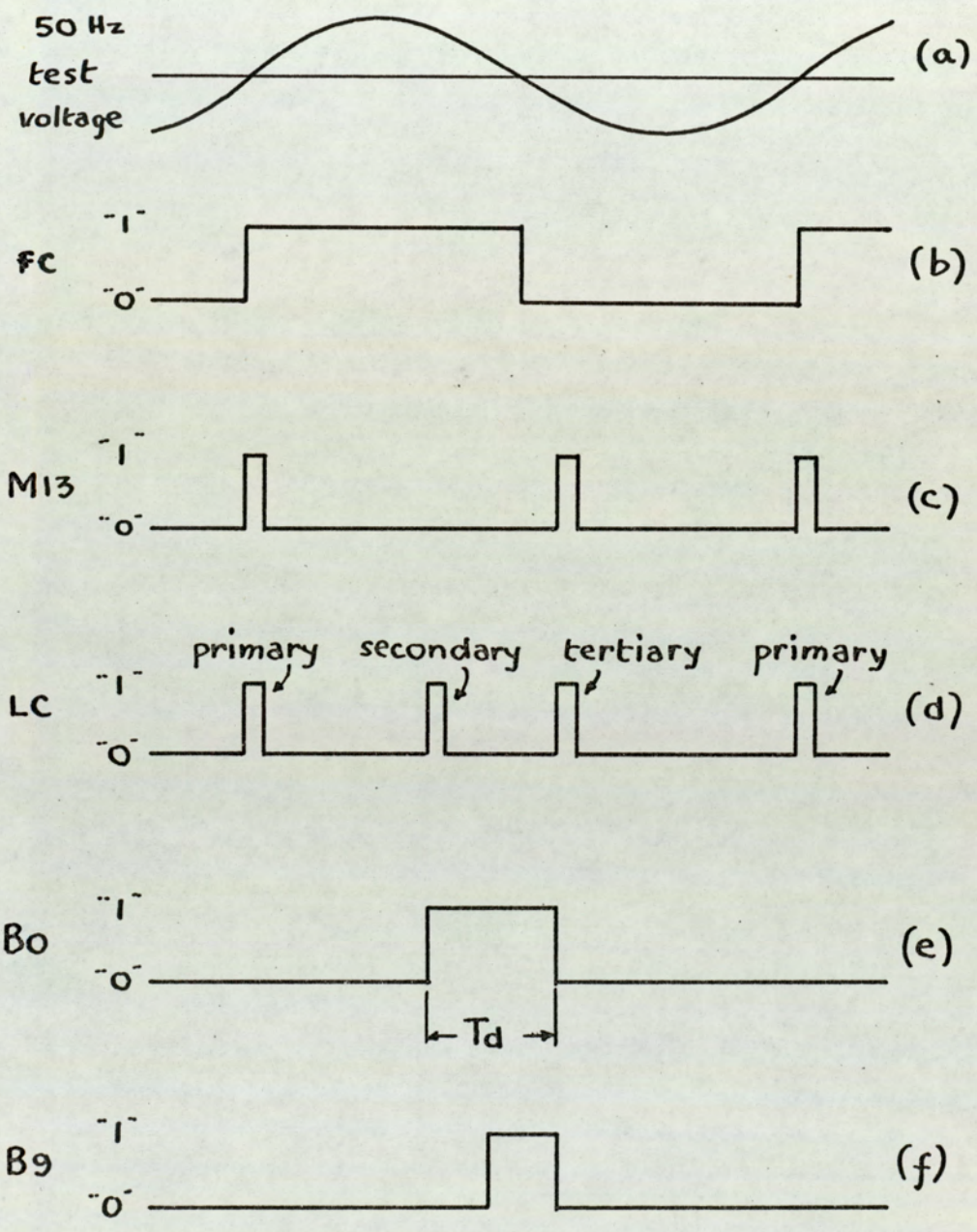


Fig. 12 Substation Waveforms

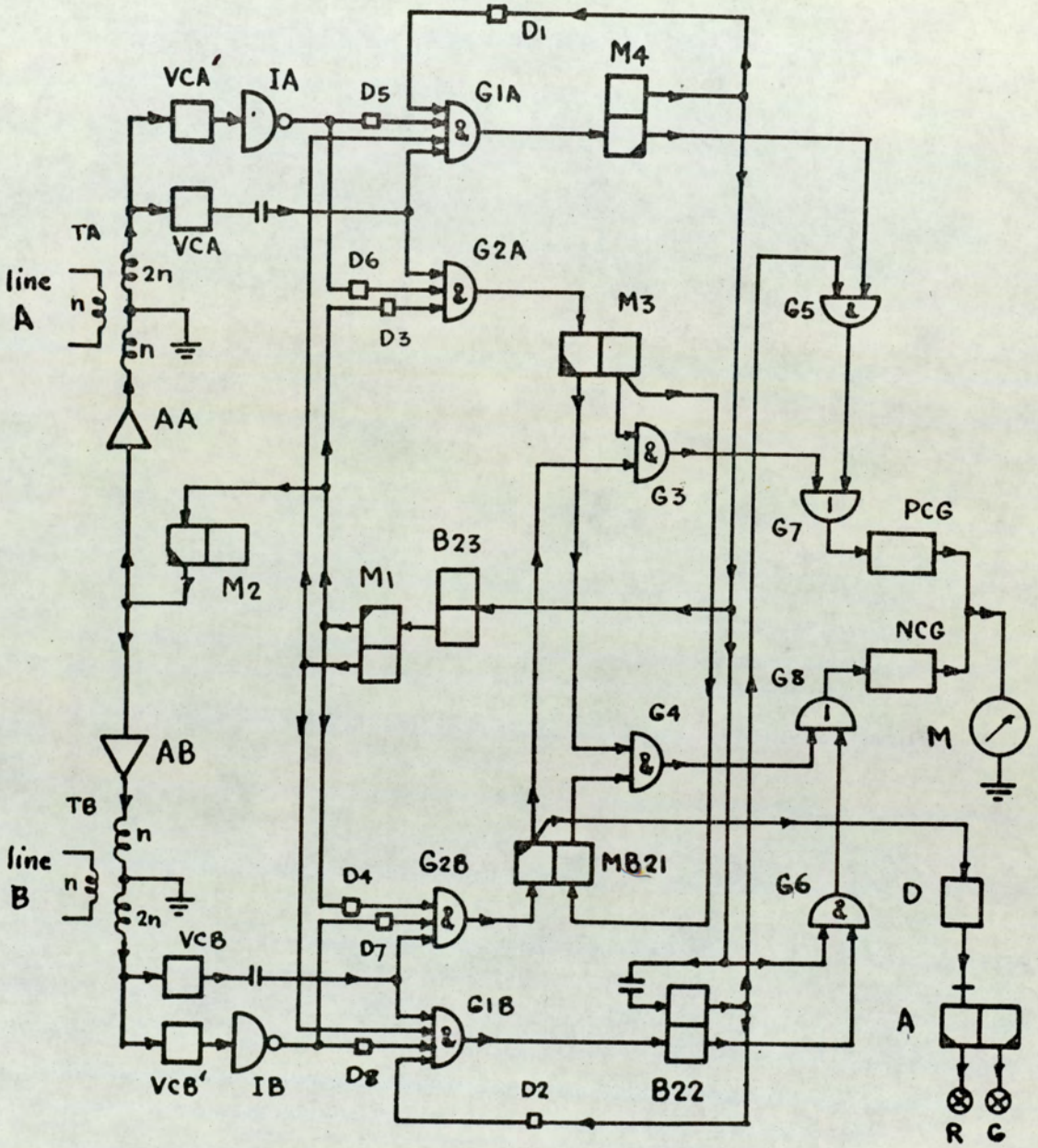


Fig. 13

CONTROL CENTRE LOGIC DIAGRAM

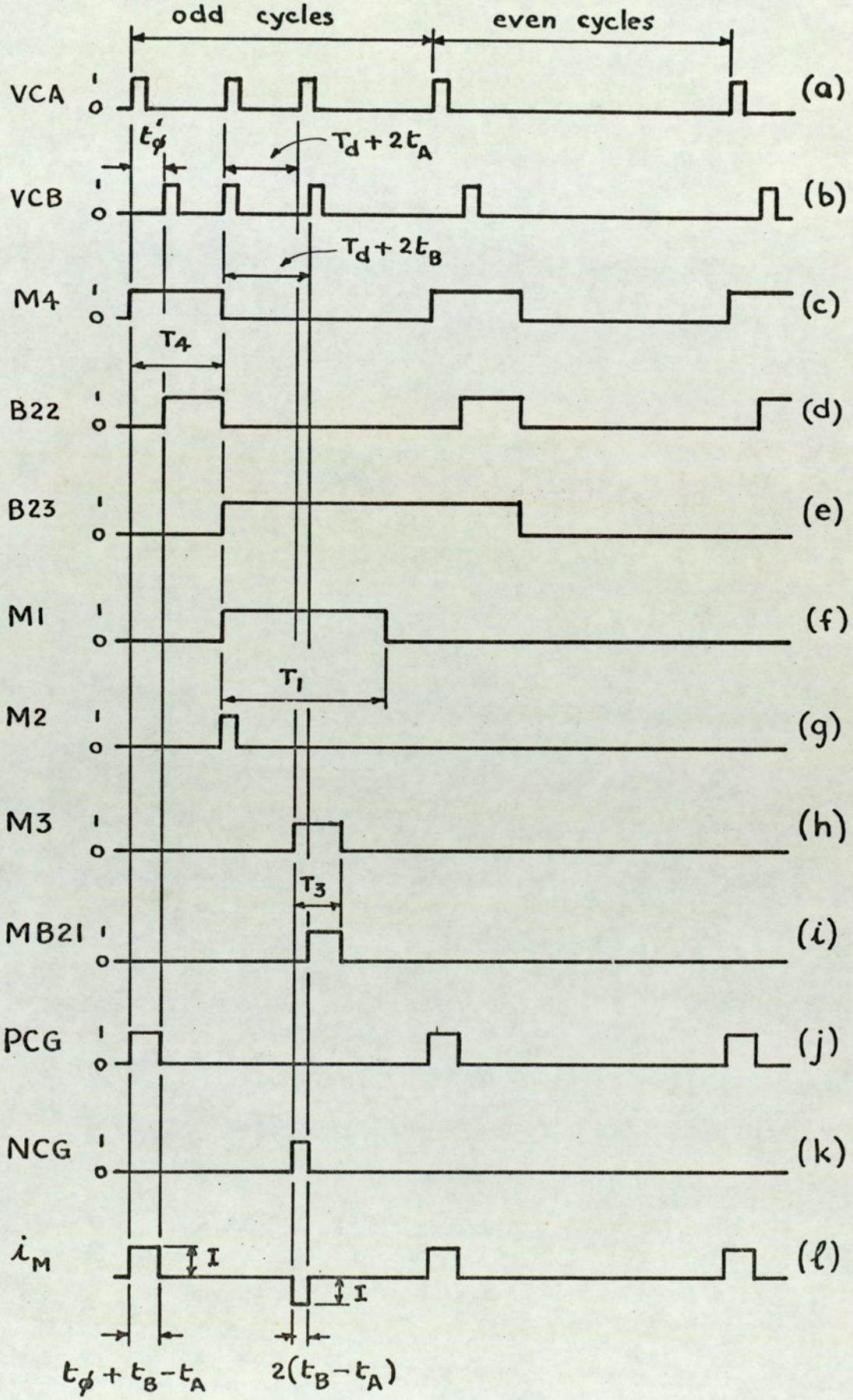


Fig. 14. Control Centre Waveforms

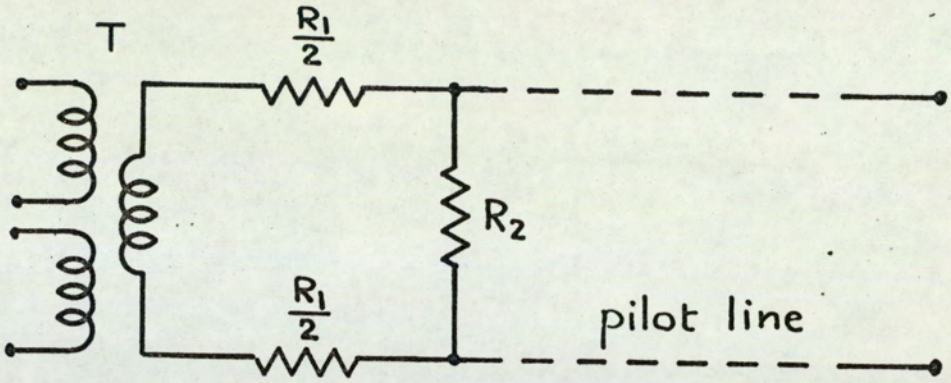


Fig. 15 Basic line coupling network

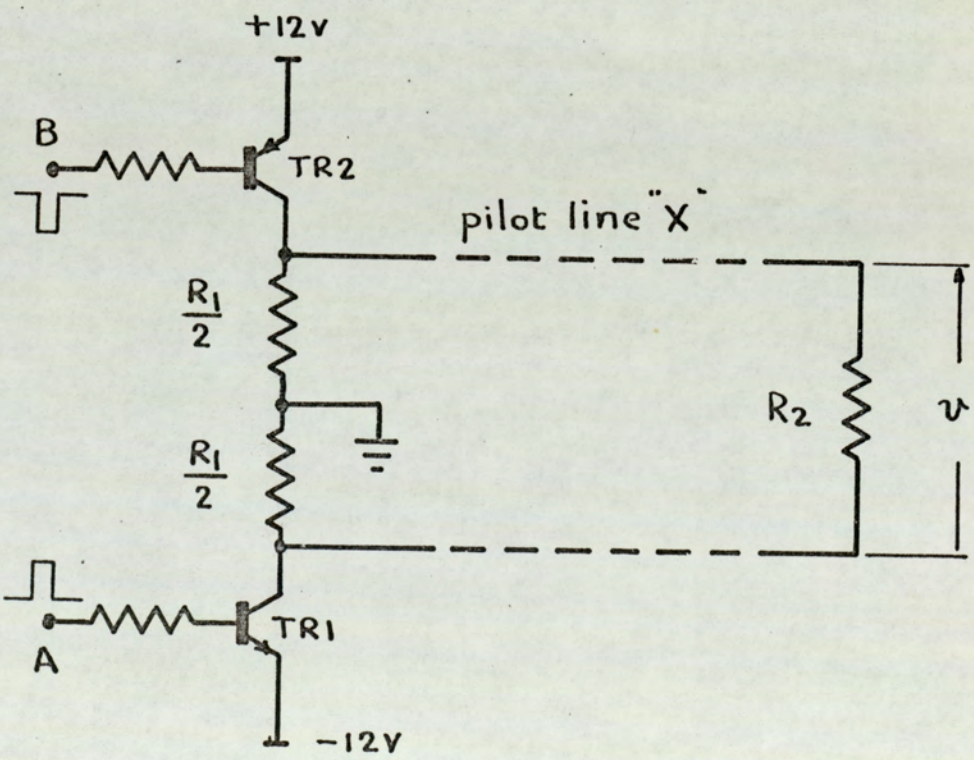


Fig. 16 Line discharge test circuit

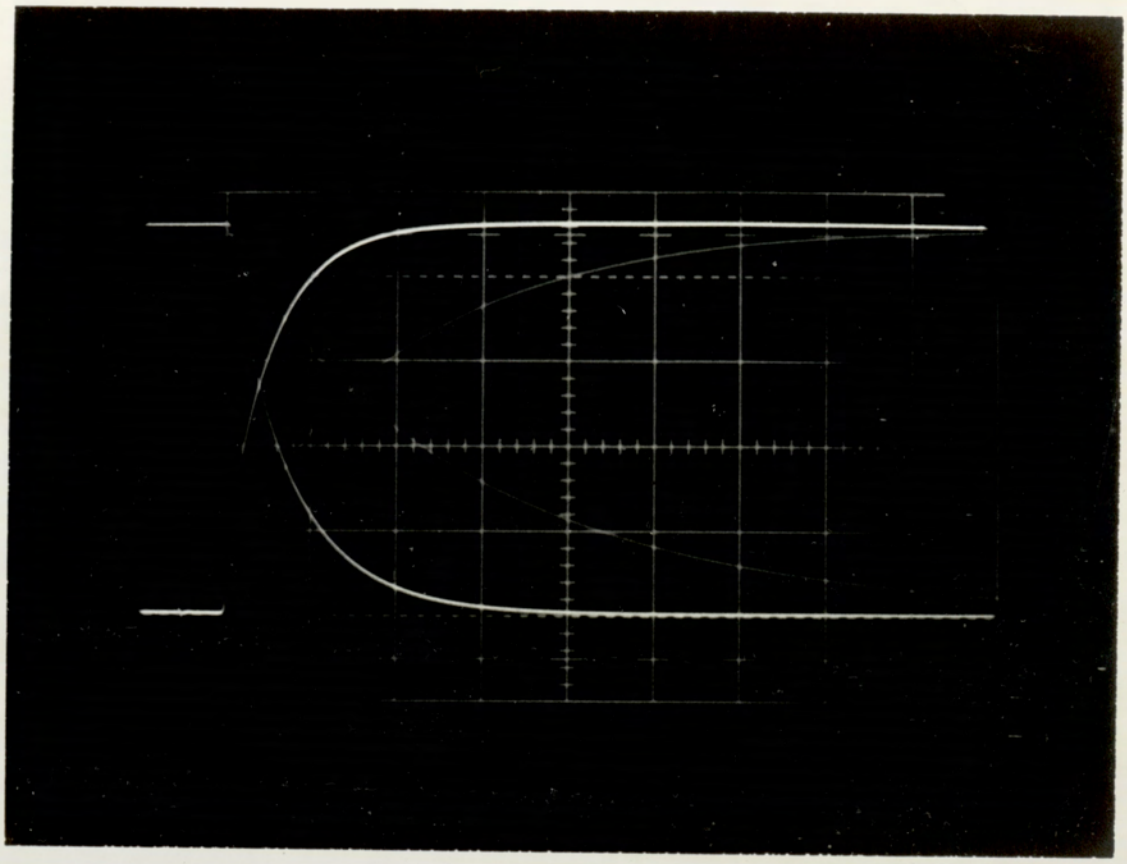


Fig.17 1V/div.
200 usec./div.
50 usec. /div.
R_2 =200 ohms.

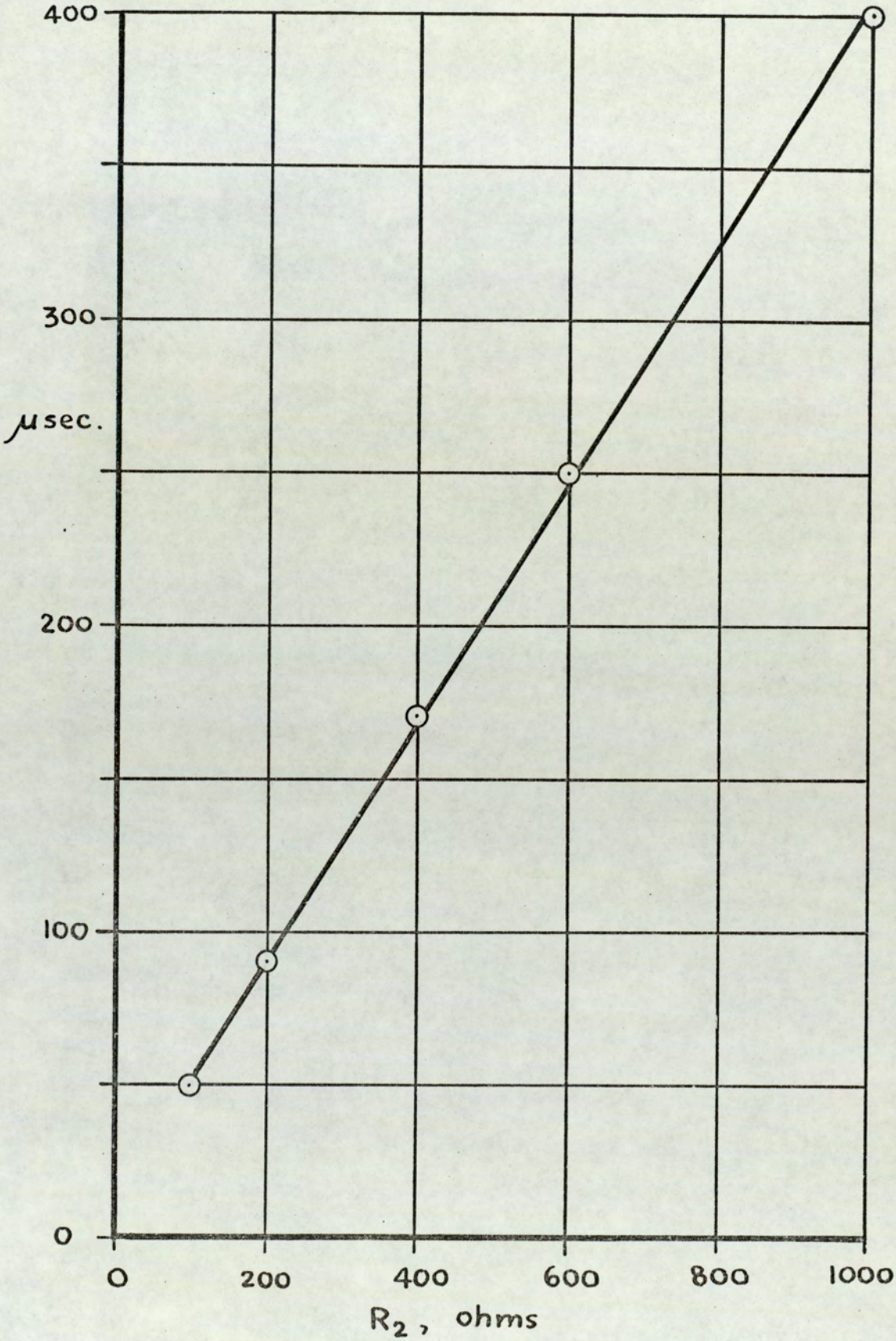


Fig. 18 Time for line to discharge to one-half initial voltage

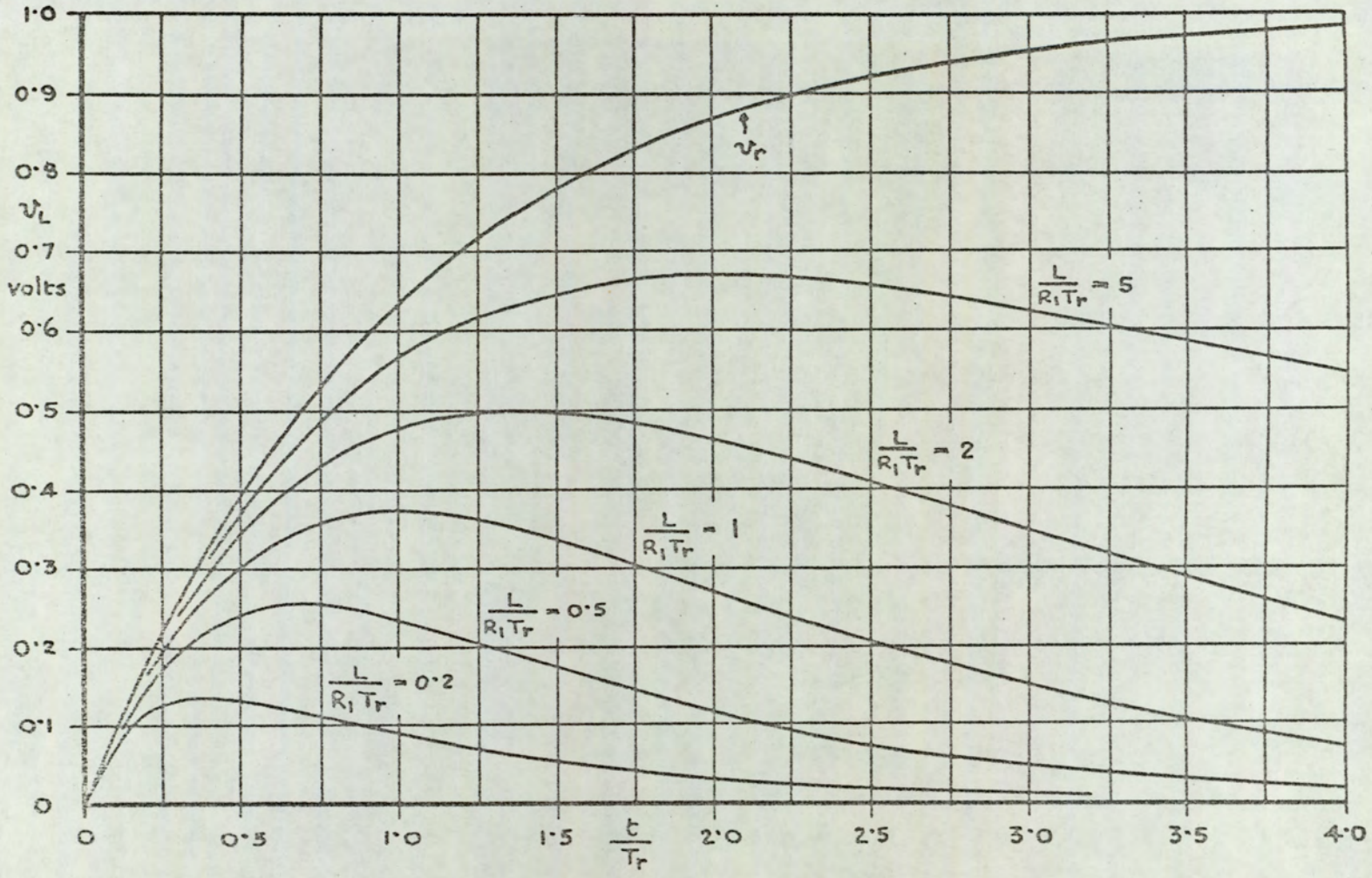


Fig. 19 Pulse Distortion by Transformer

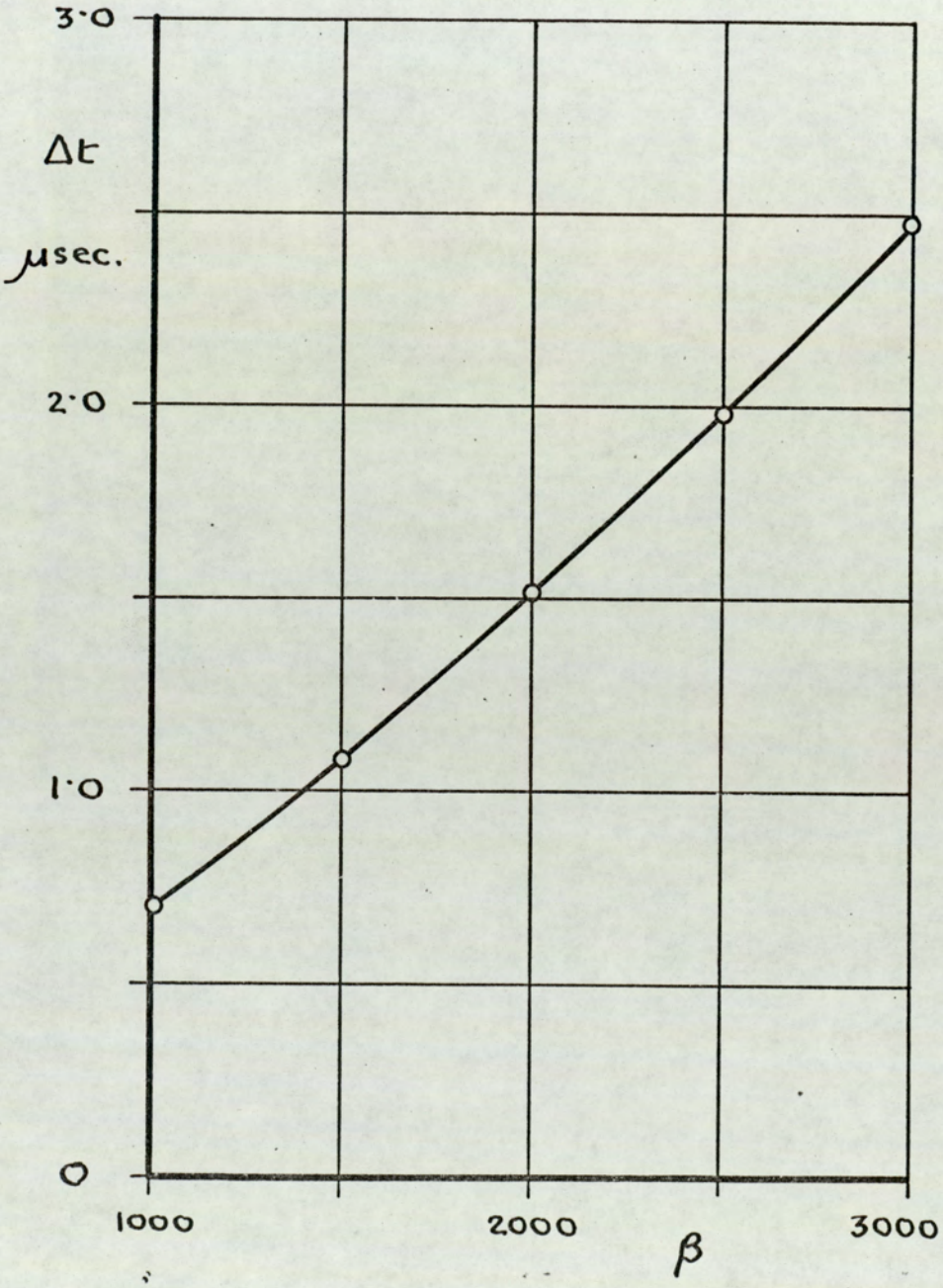


Fig. 20 Transformer timing error

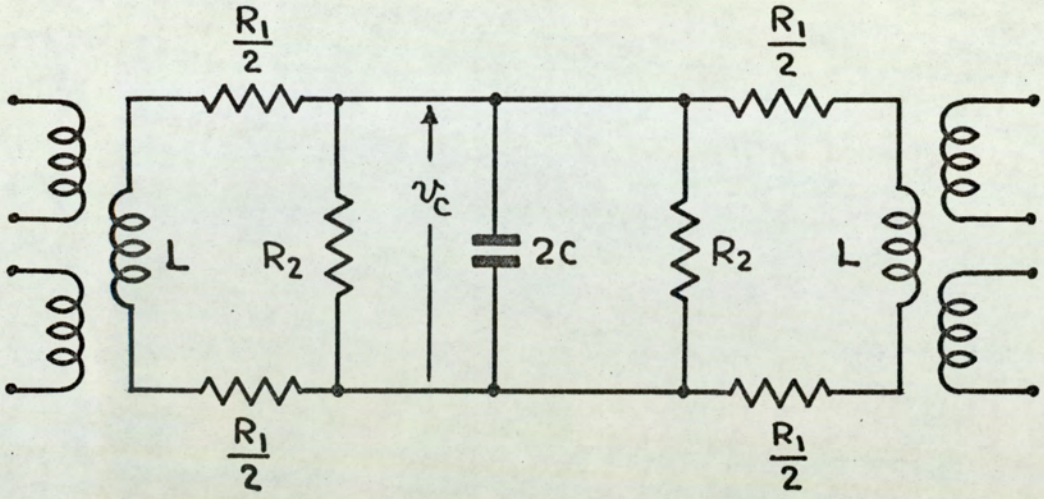


Fig. 21

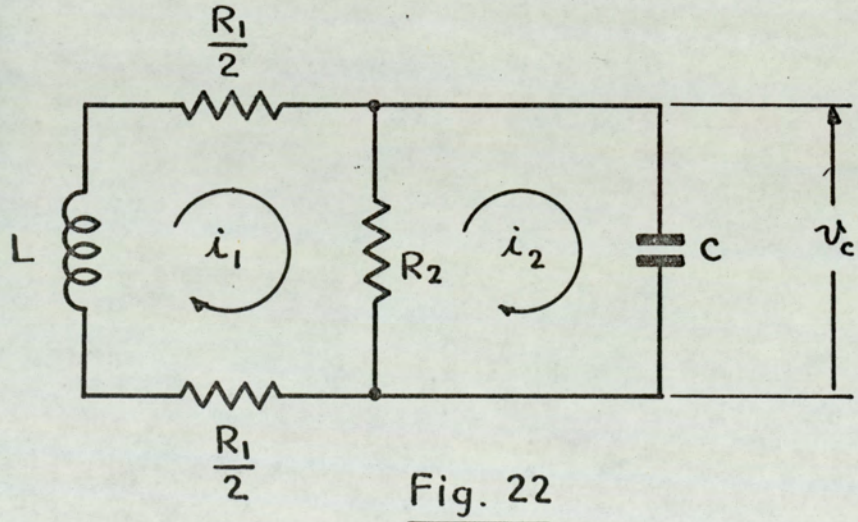


Fig. 22

Pilot line equivalent circuits

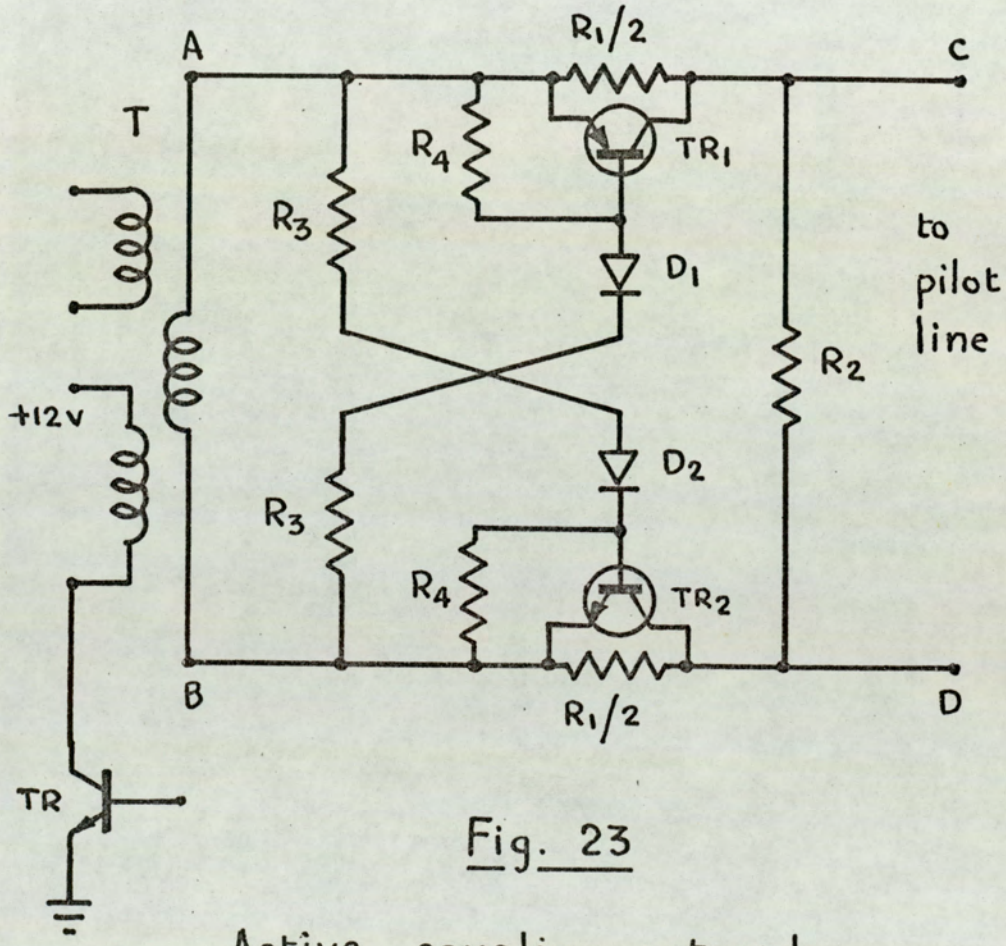


Fig. 23

Active coupling network

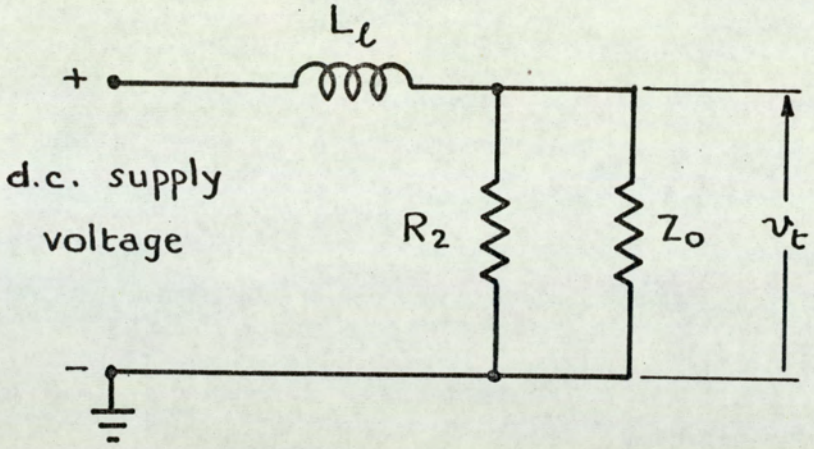


Fig. 24 Equivalent circuit during transmitted pulse

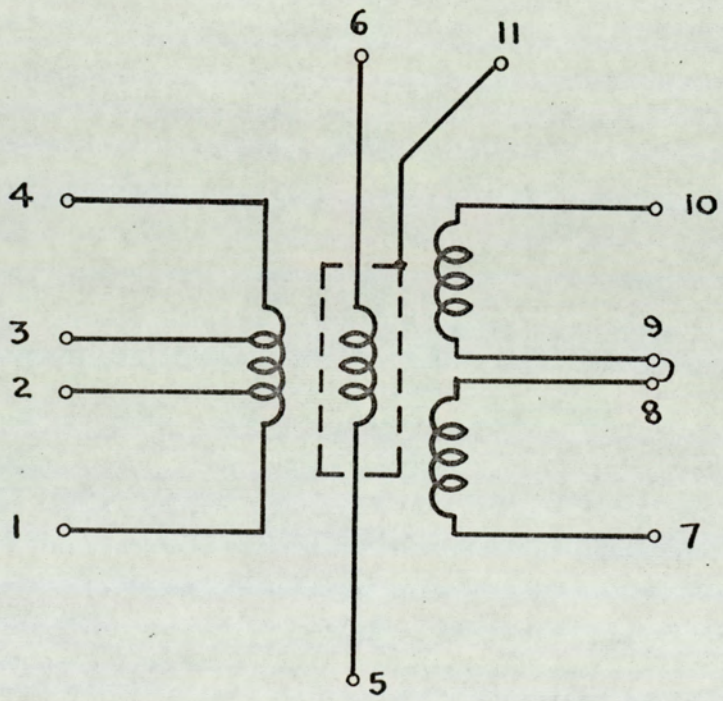


Fig. 25 Transformer connections

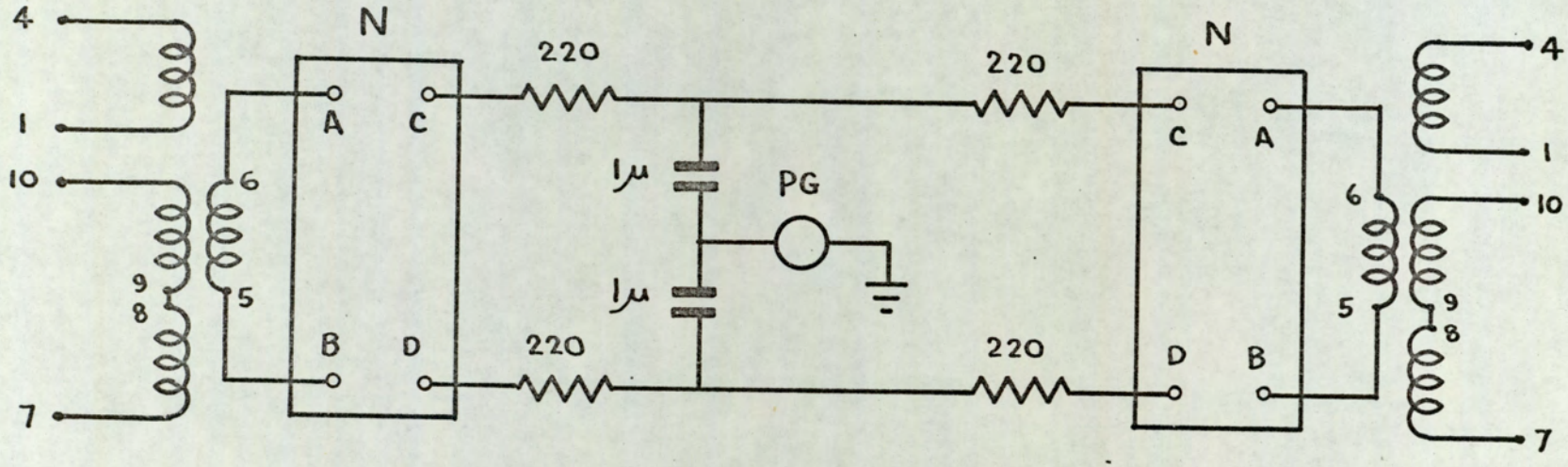


Fig. 26 Common-mode test circuit

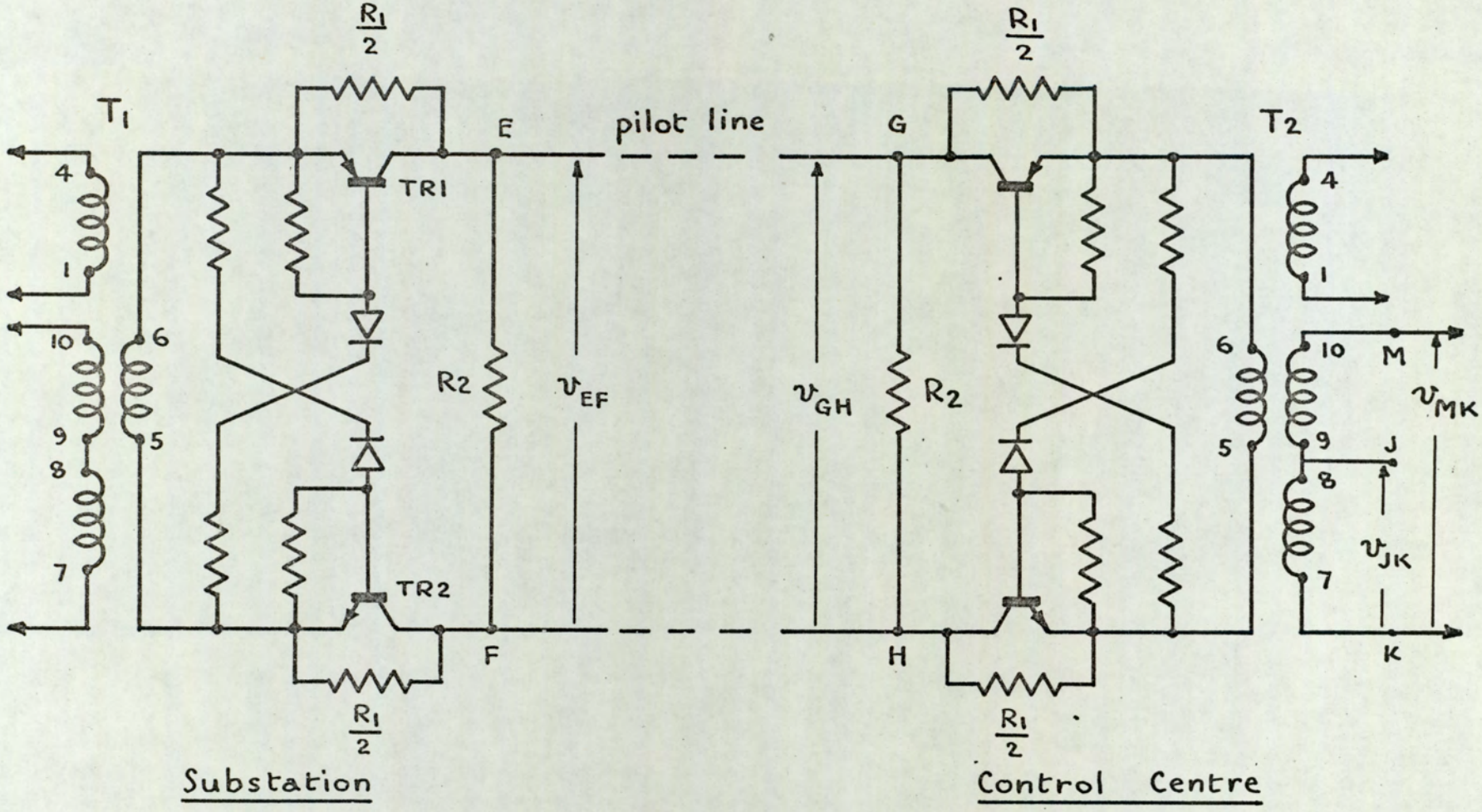


Fig. 27 Pilot line test circuit

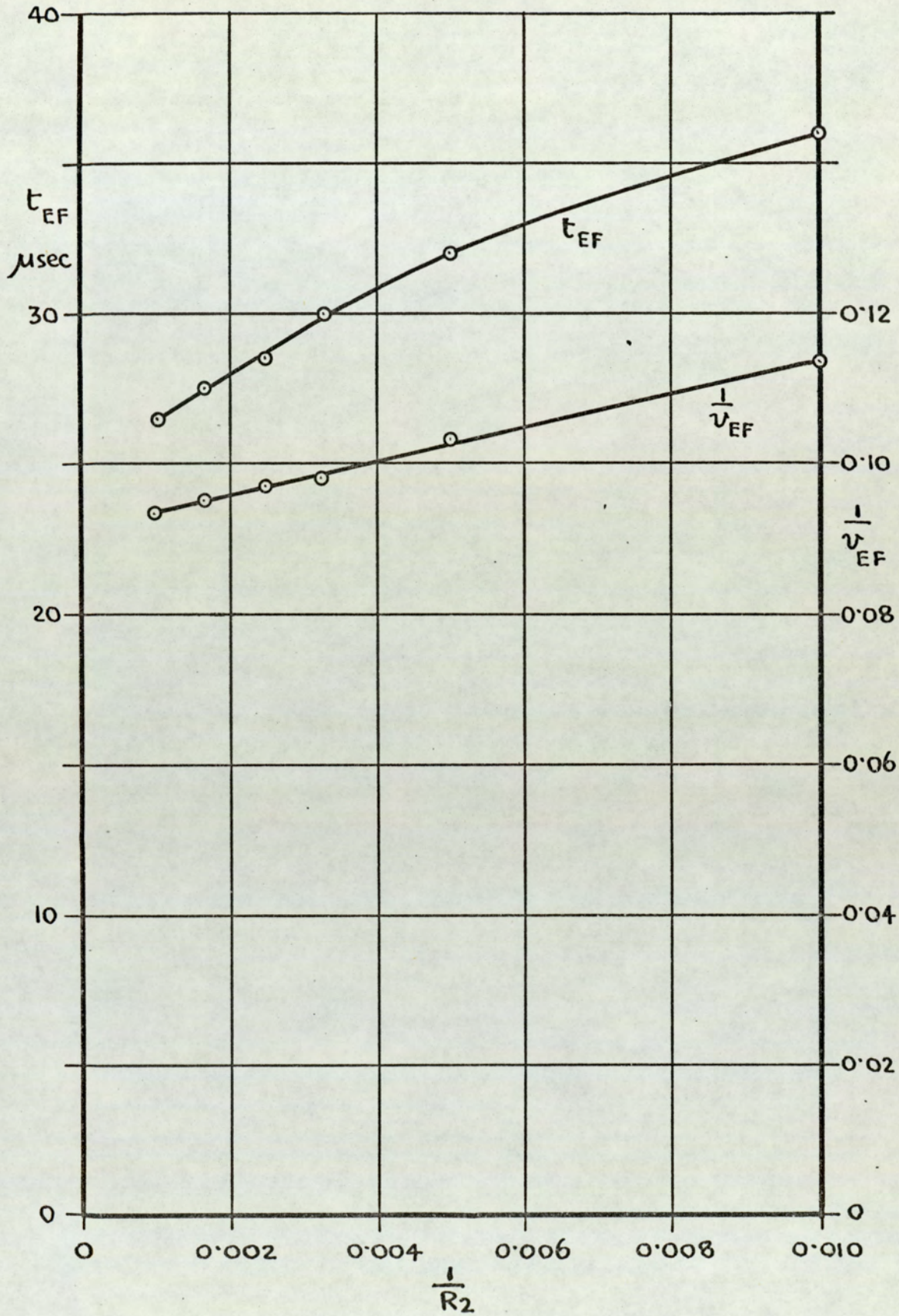


Fig. 28 Coupling network tests

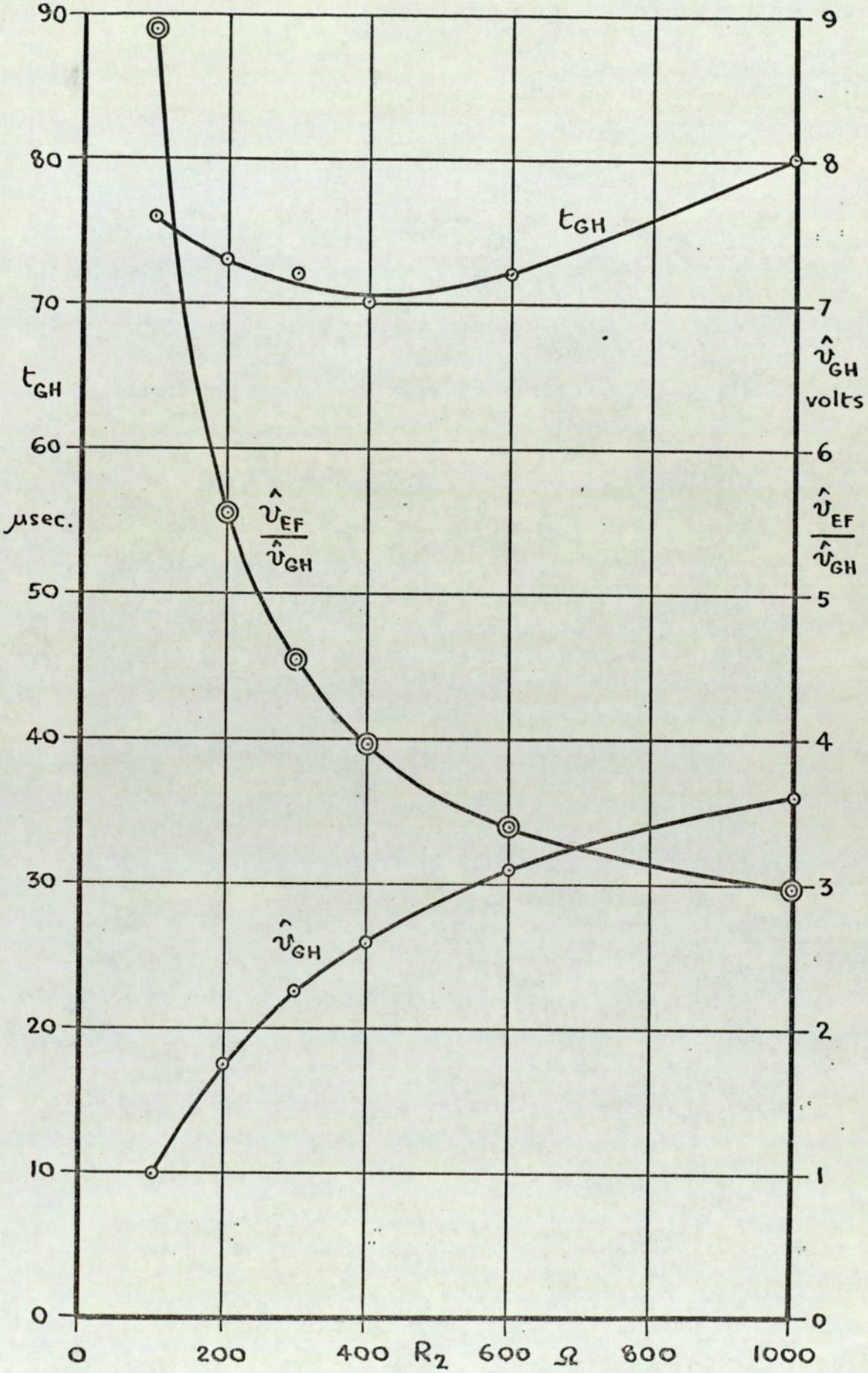


Fig. 29 Coupling network tests

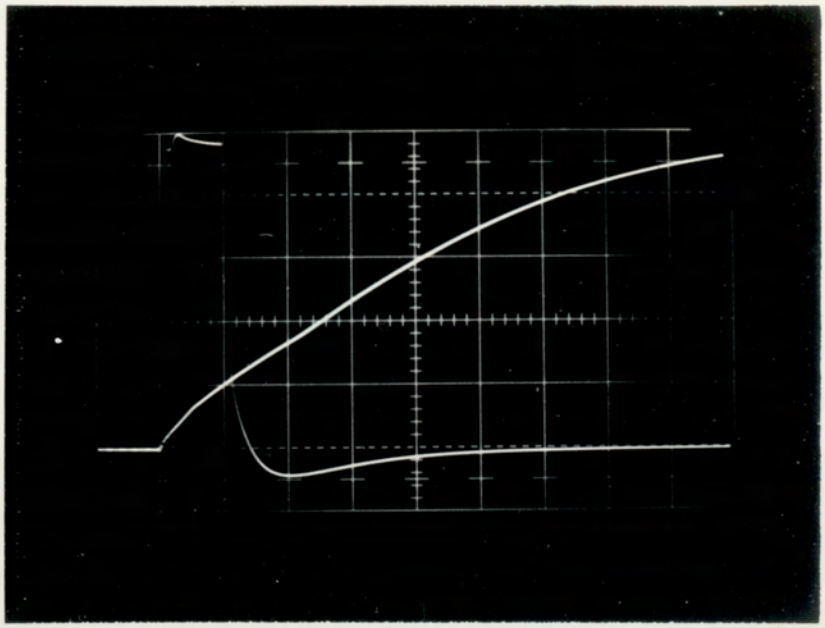


Fig.30 2V/div.
500 μsec./div.
10 μsec./div.

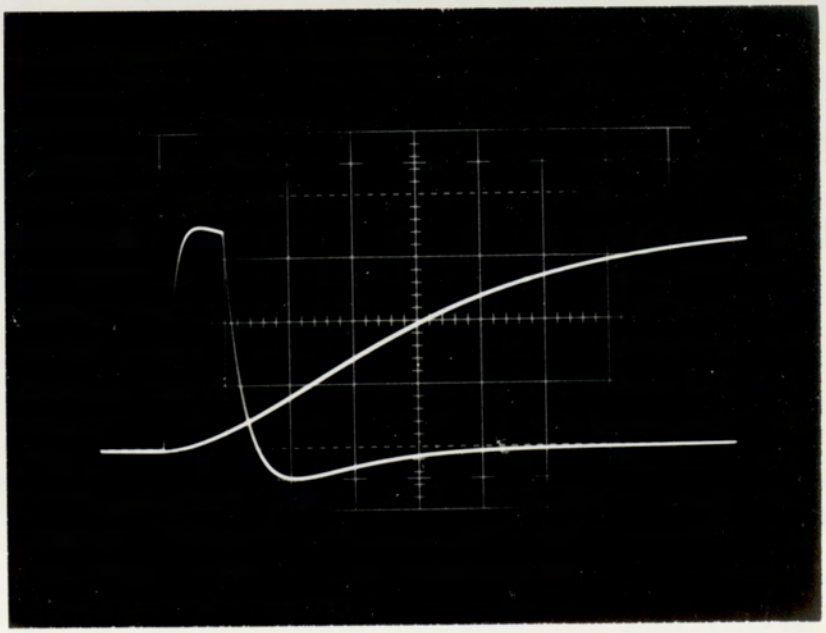


Fig.31 0.5V/div.
500 μsec./div.
20 μsec./div.

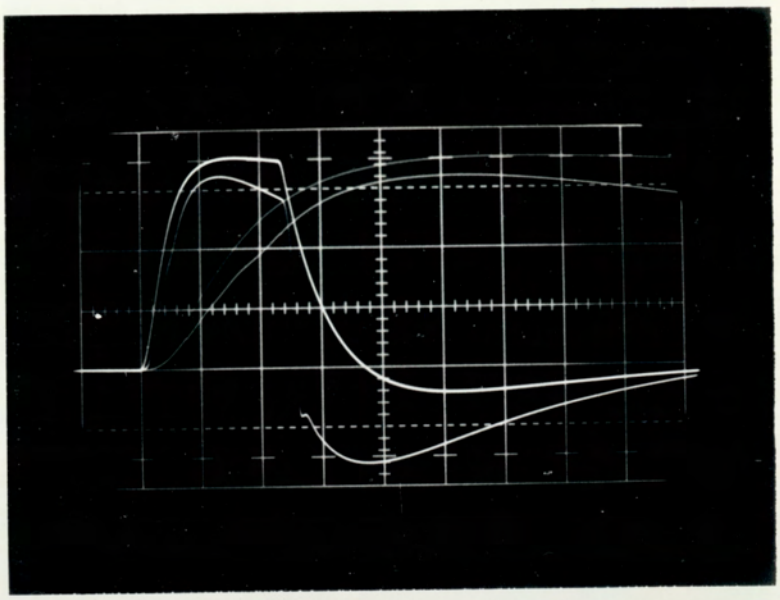


Fig.32 0.5V/div.
200 μsec./div.
50 μsec./div.

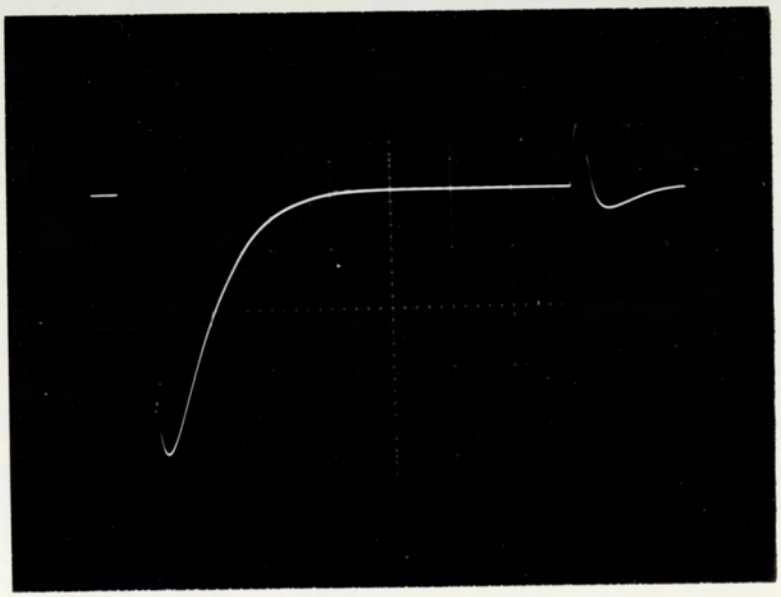


Fig.34 2V/div.
1 m Sec./div.
$\frac{R\,1}{2}$ = 500 ohms.
R_2 = 200 ohms.

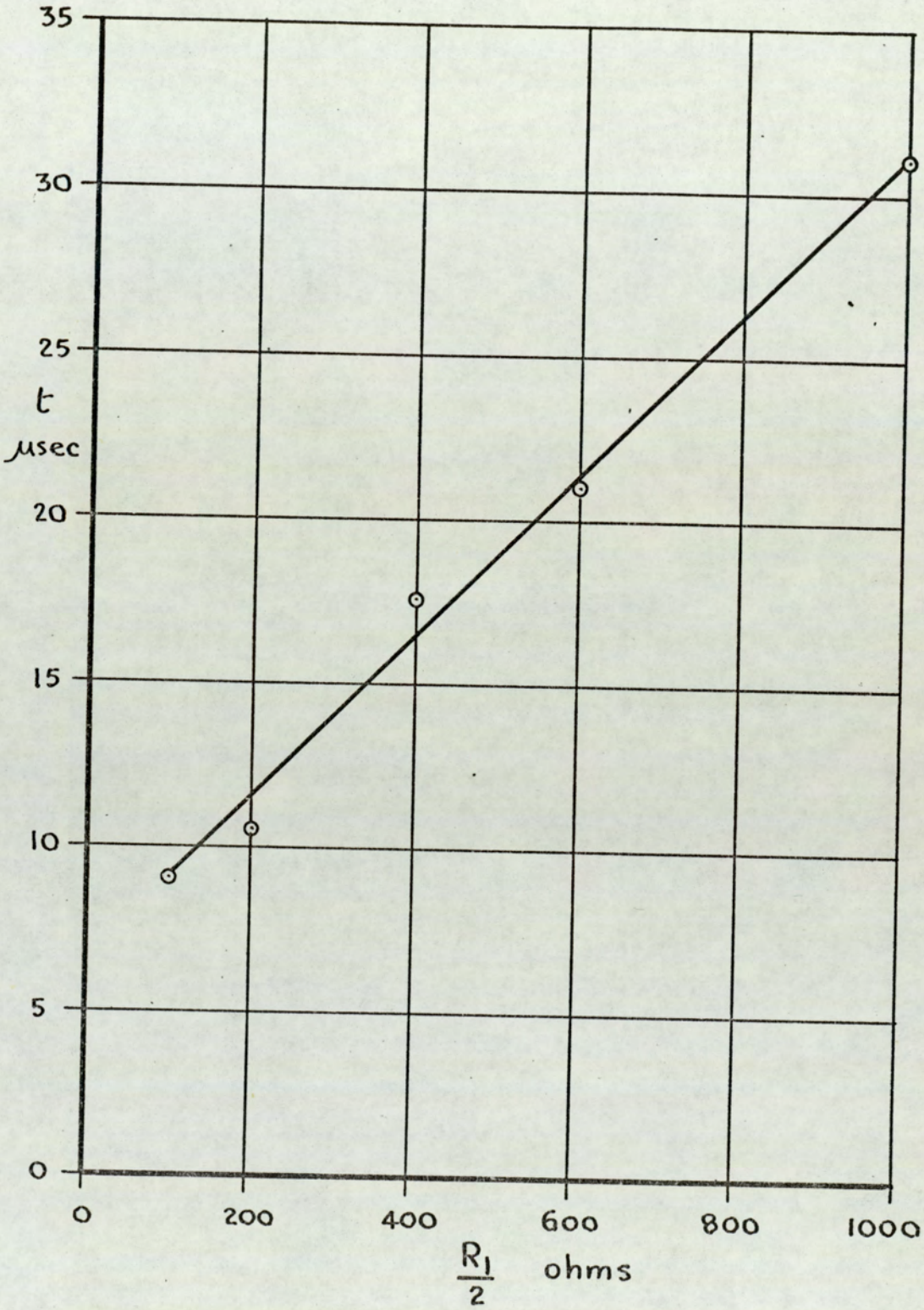


Fig. 33 Transformer delay test

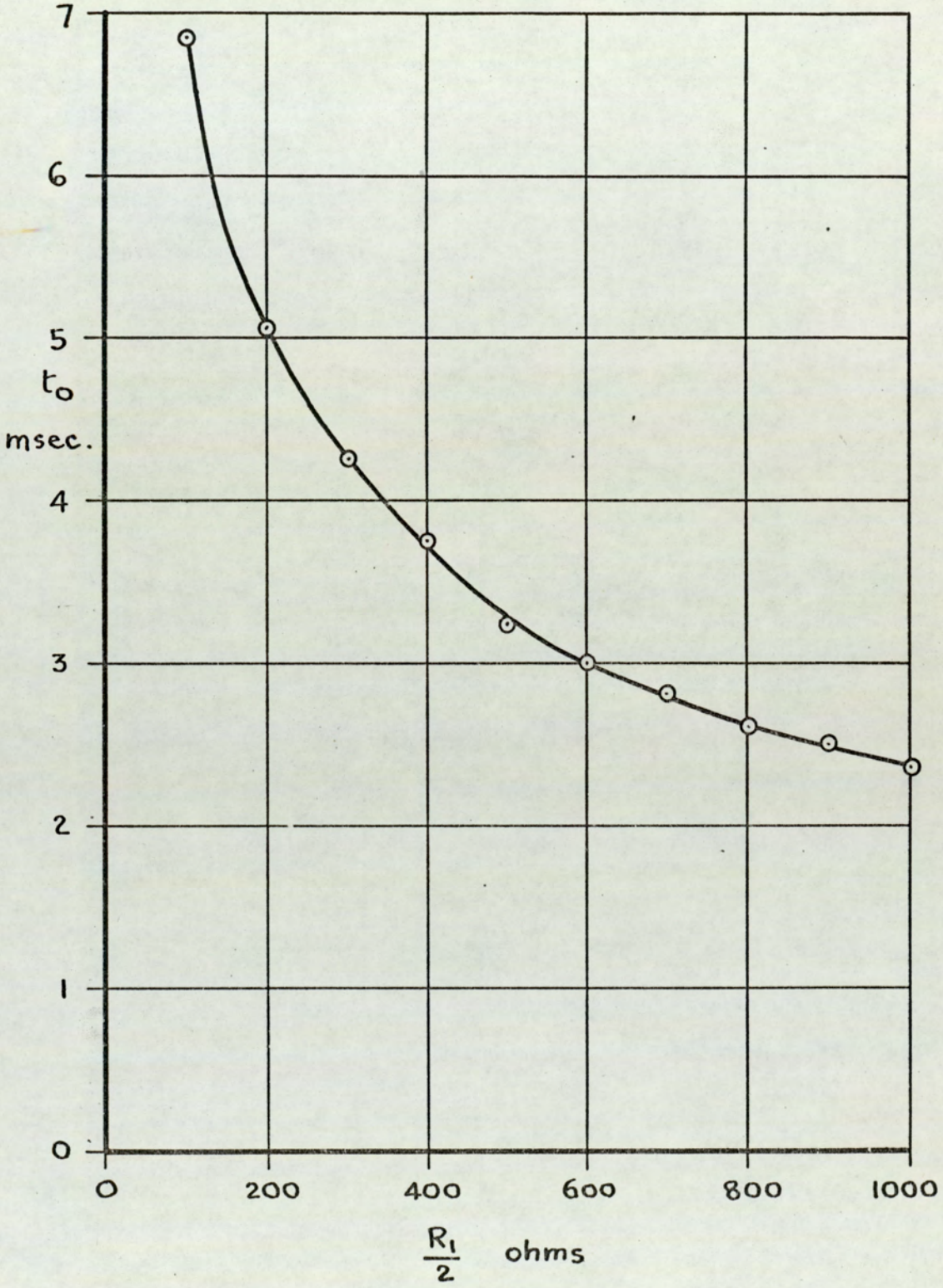


Fig. 35. Transformer overswing recovery time

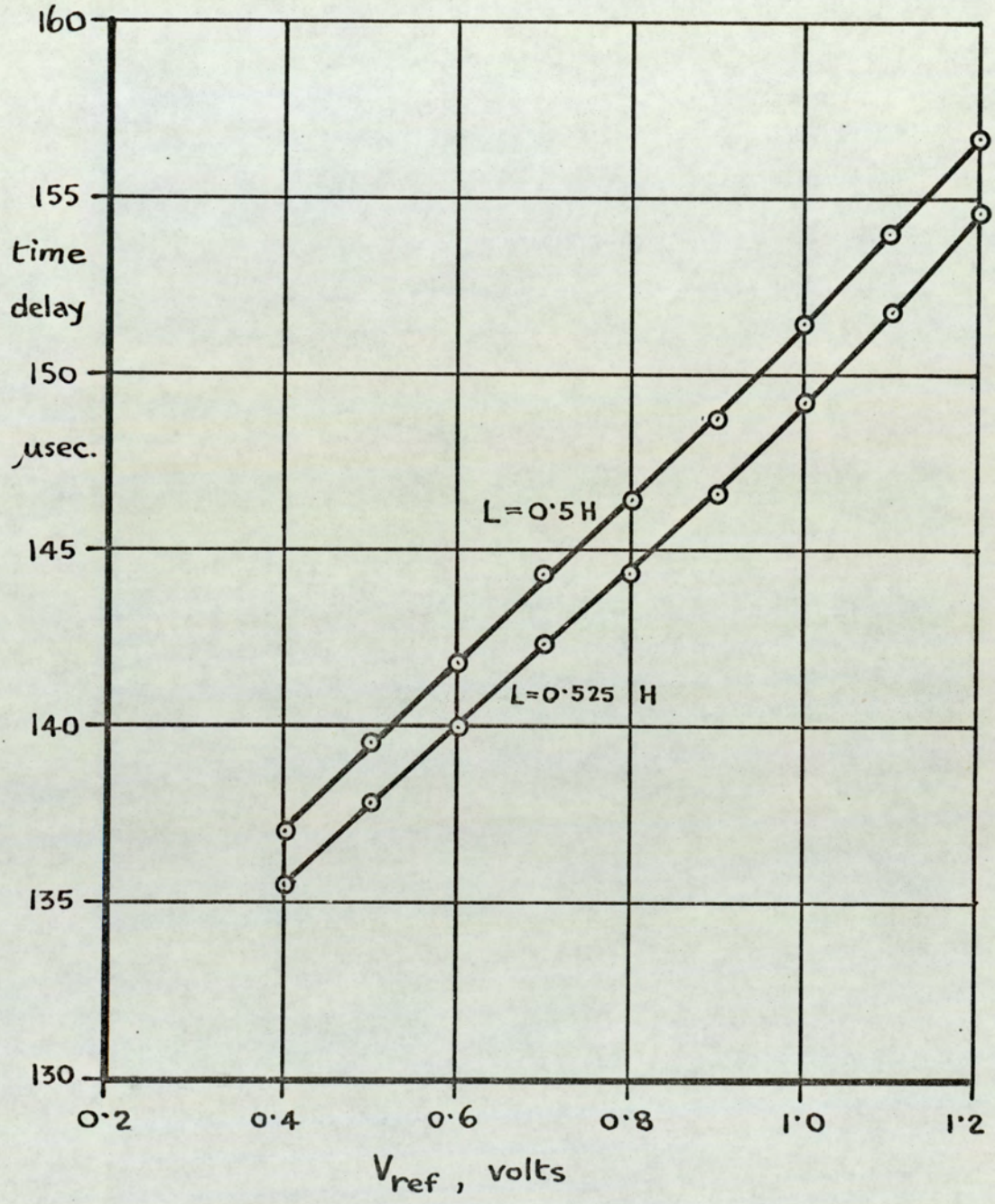


Fig. 36 Effect of transformer inductance L

(Amplitude of voltage pulse across terminals 7, 10 = 3·4 V)

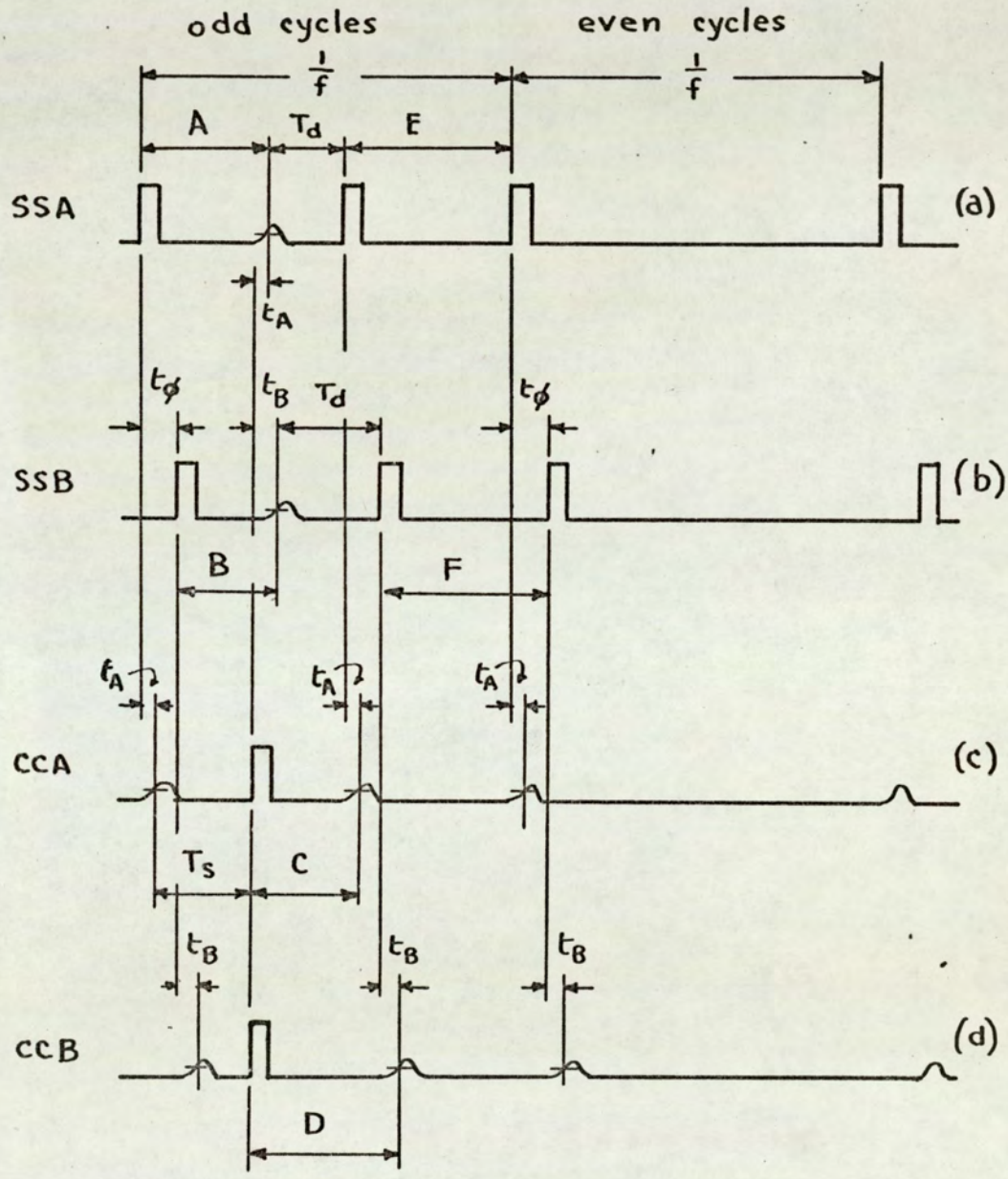


Fig. 37 System timing

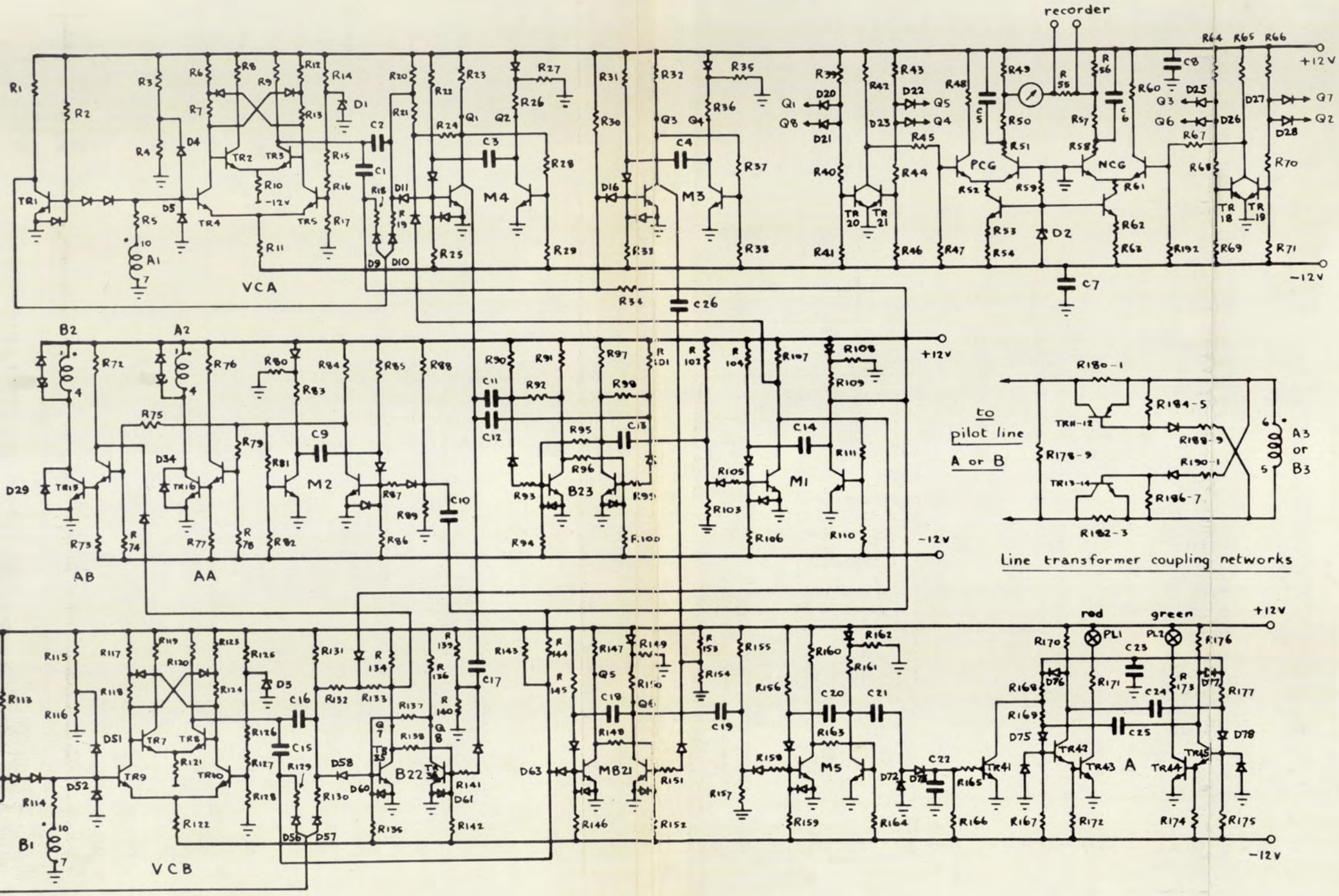


FIG 38

CONTROL CENTRE UNIT CIRCUIT DIAGRAM

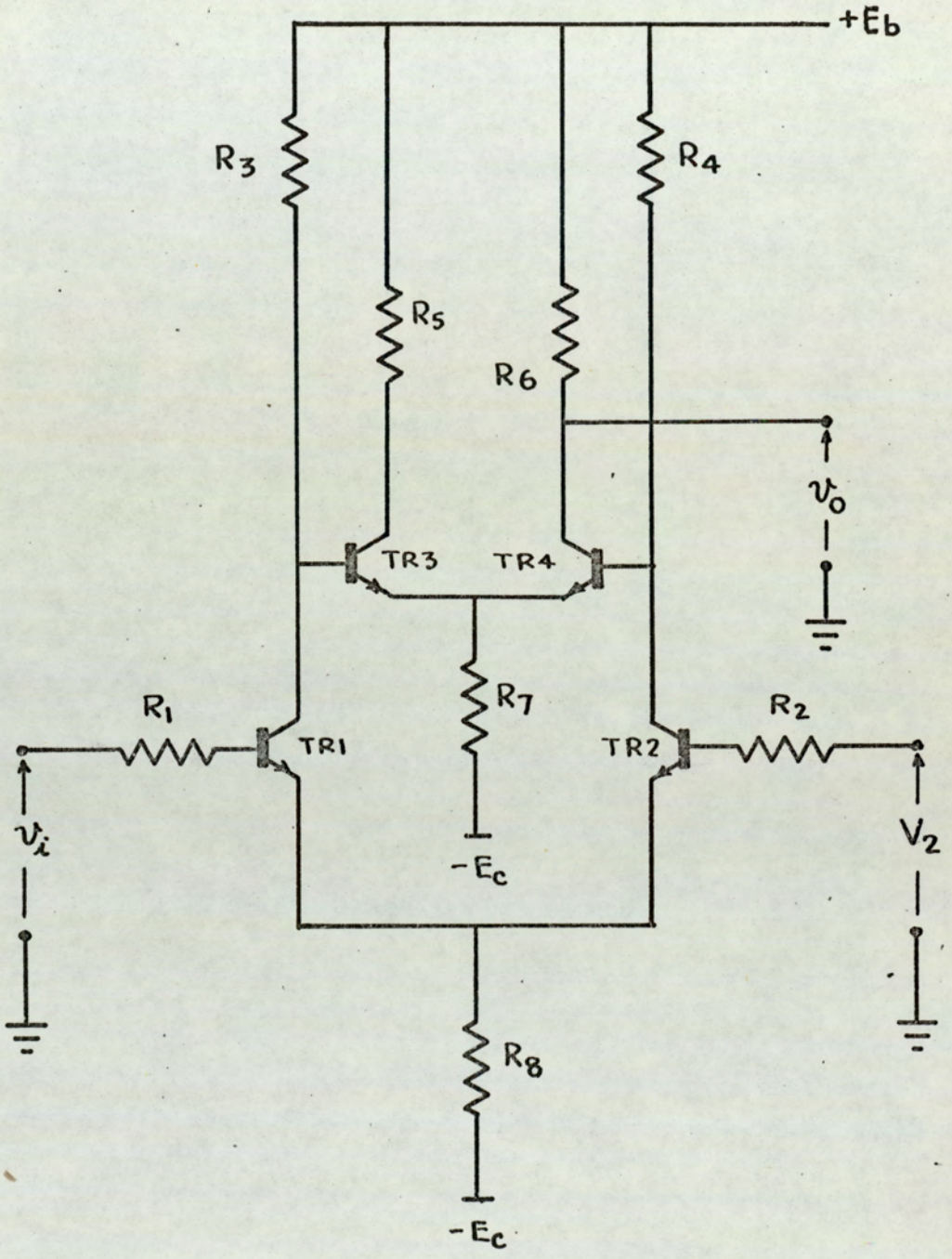


Fig. 39 Voltage comparator

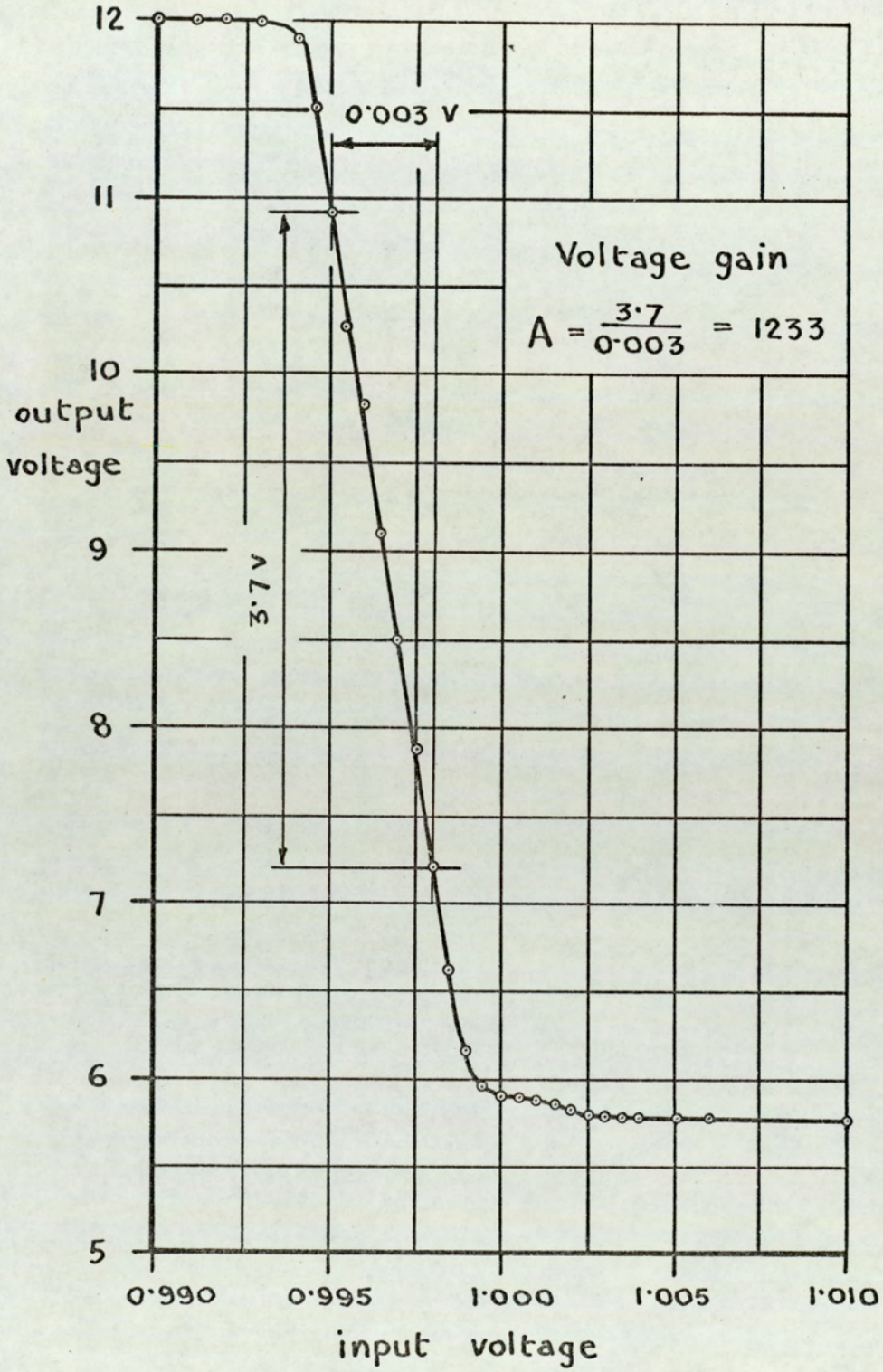


Fig. 40 Voltage comparator gain

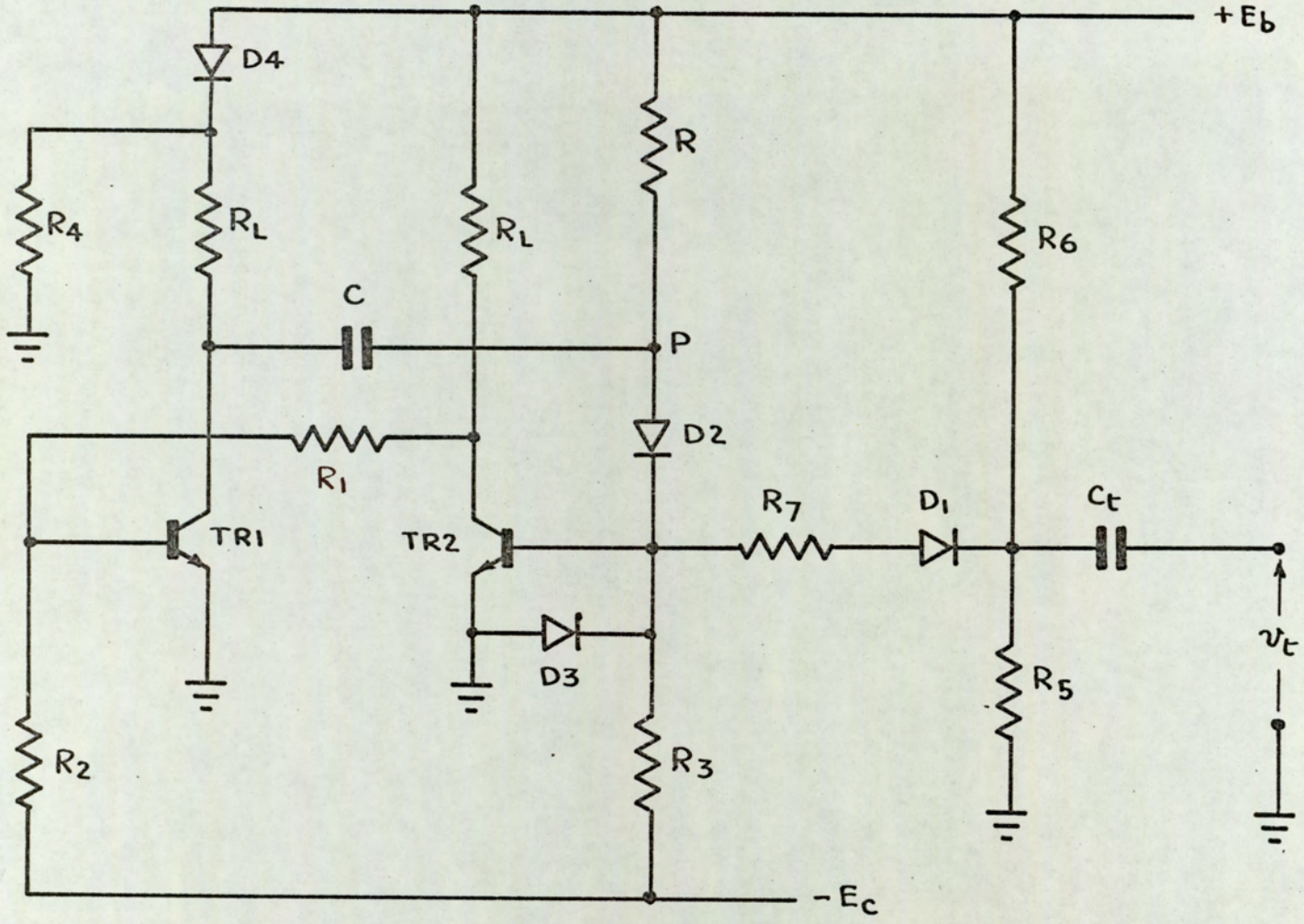


Fig. 41 Monostable multivibrator circuit

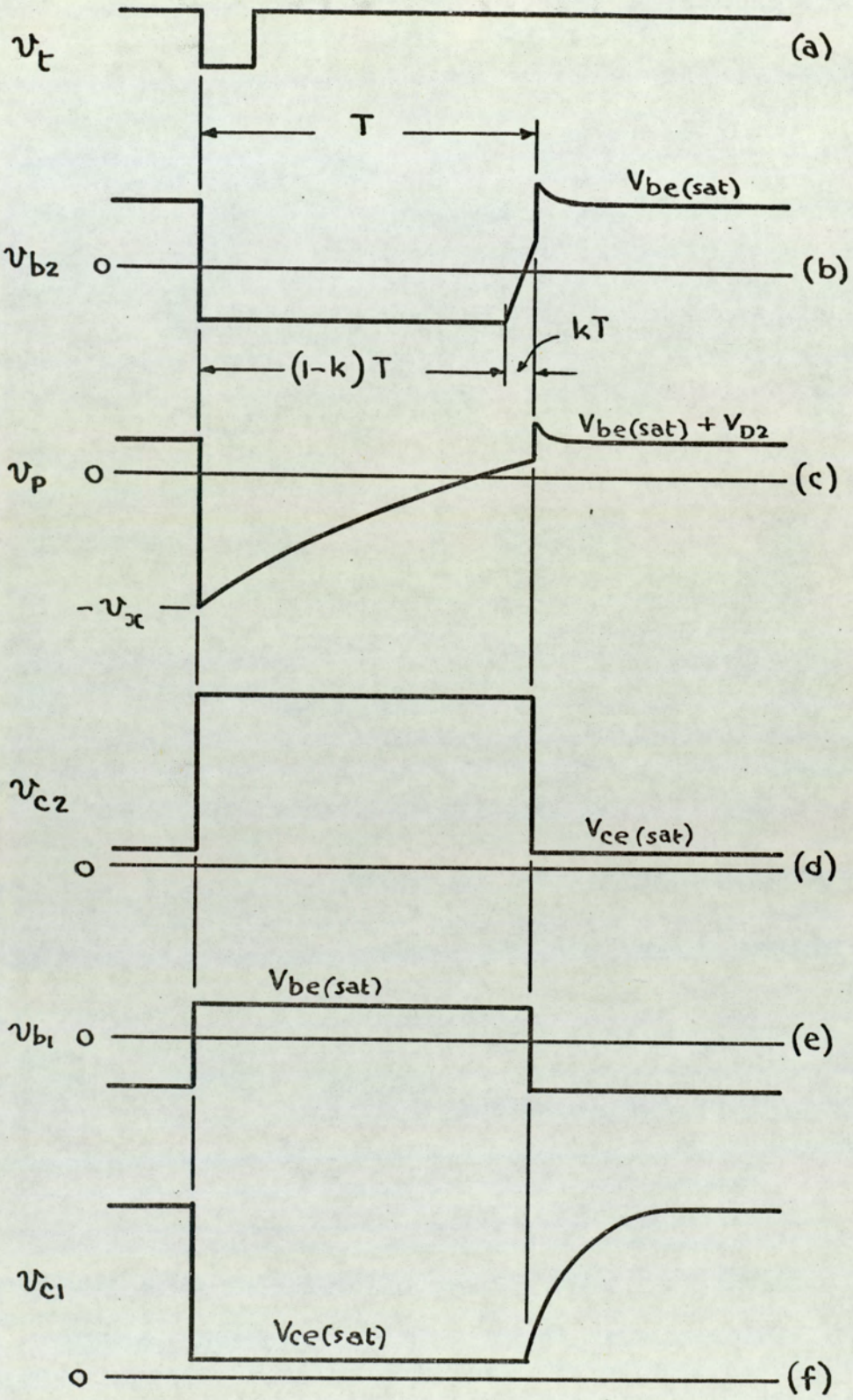


Fig. 42 Monostable multivibrator waveforms

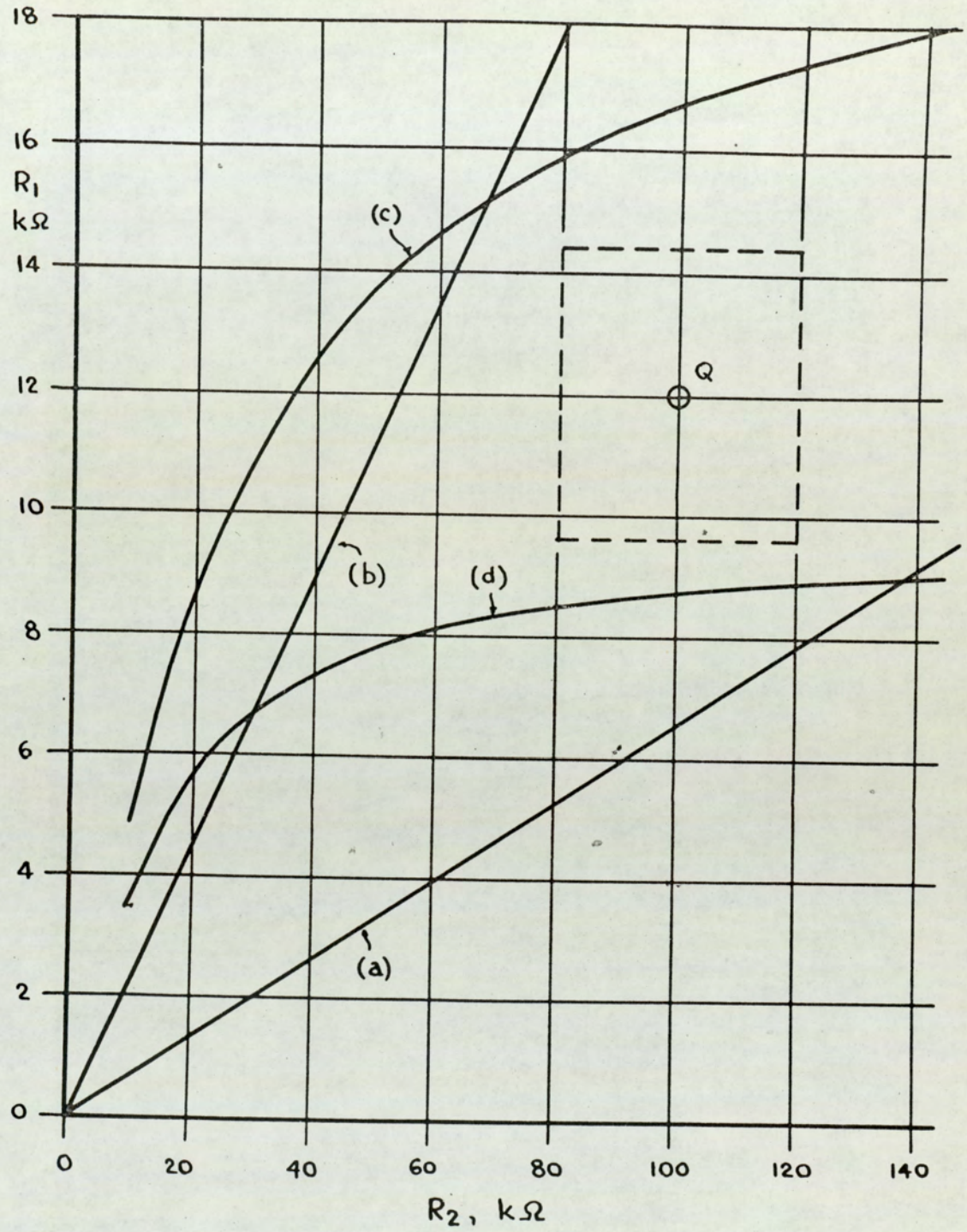


FIG 43

RESISTOR TOLERANCE DIAGRAM

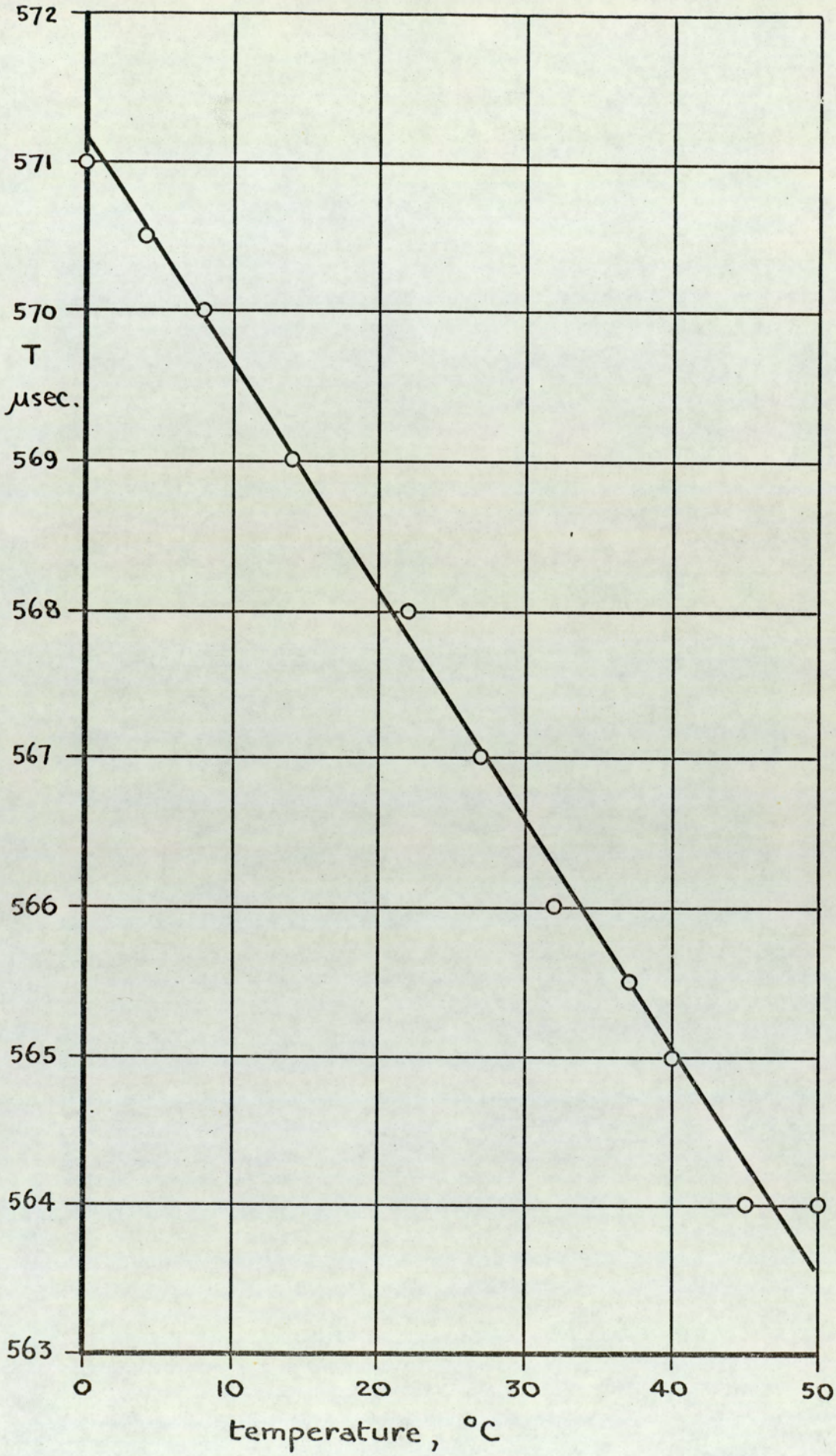


Fig. 44 Multivibrator period v. temperature

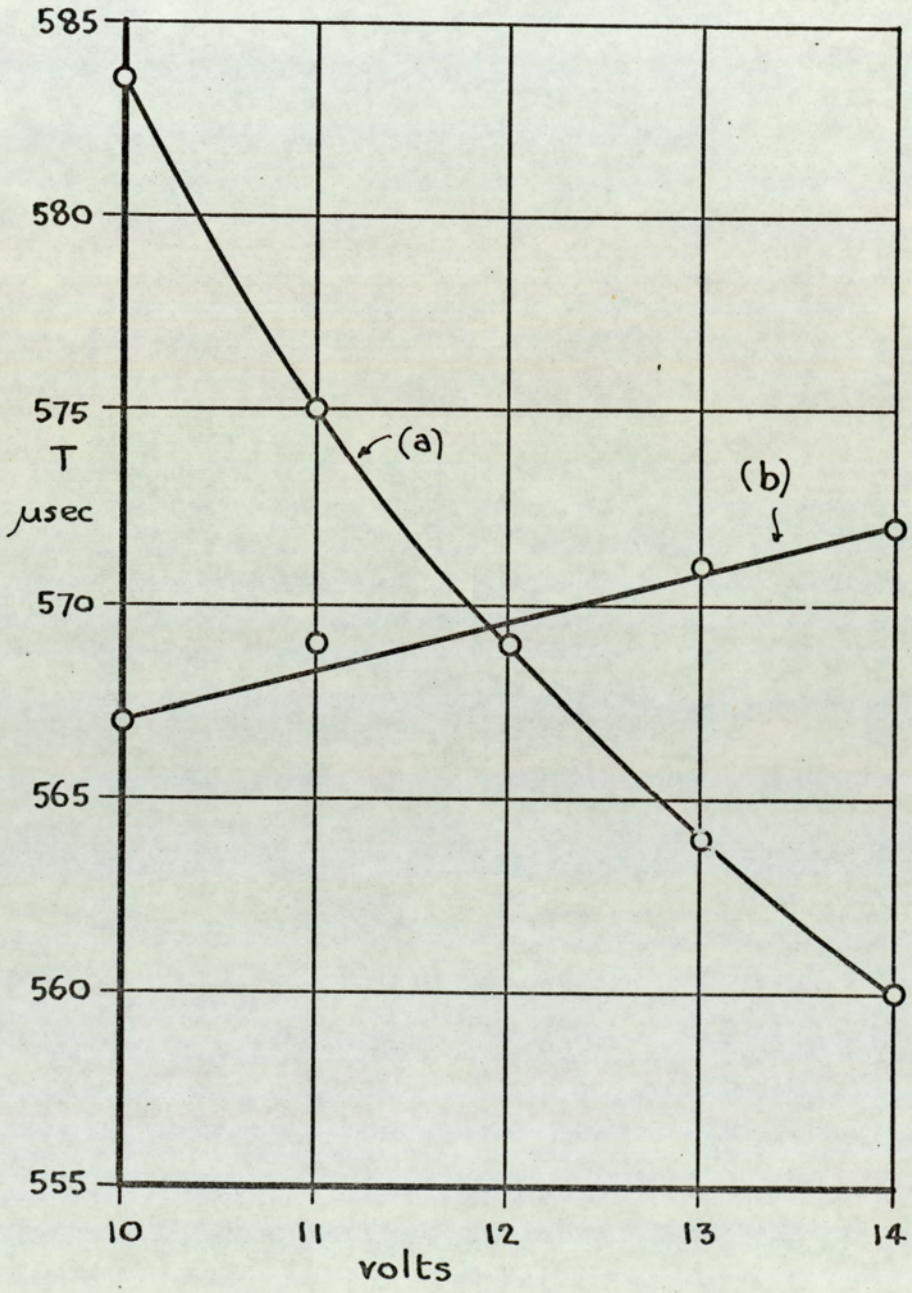


Fig. 45 Multivibrator period v. supply voltages

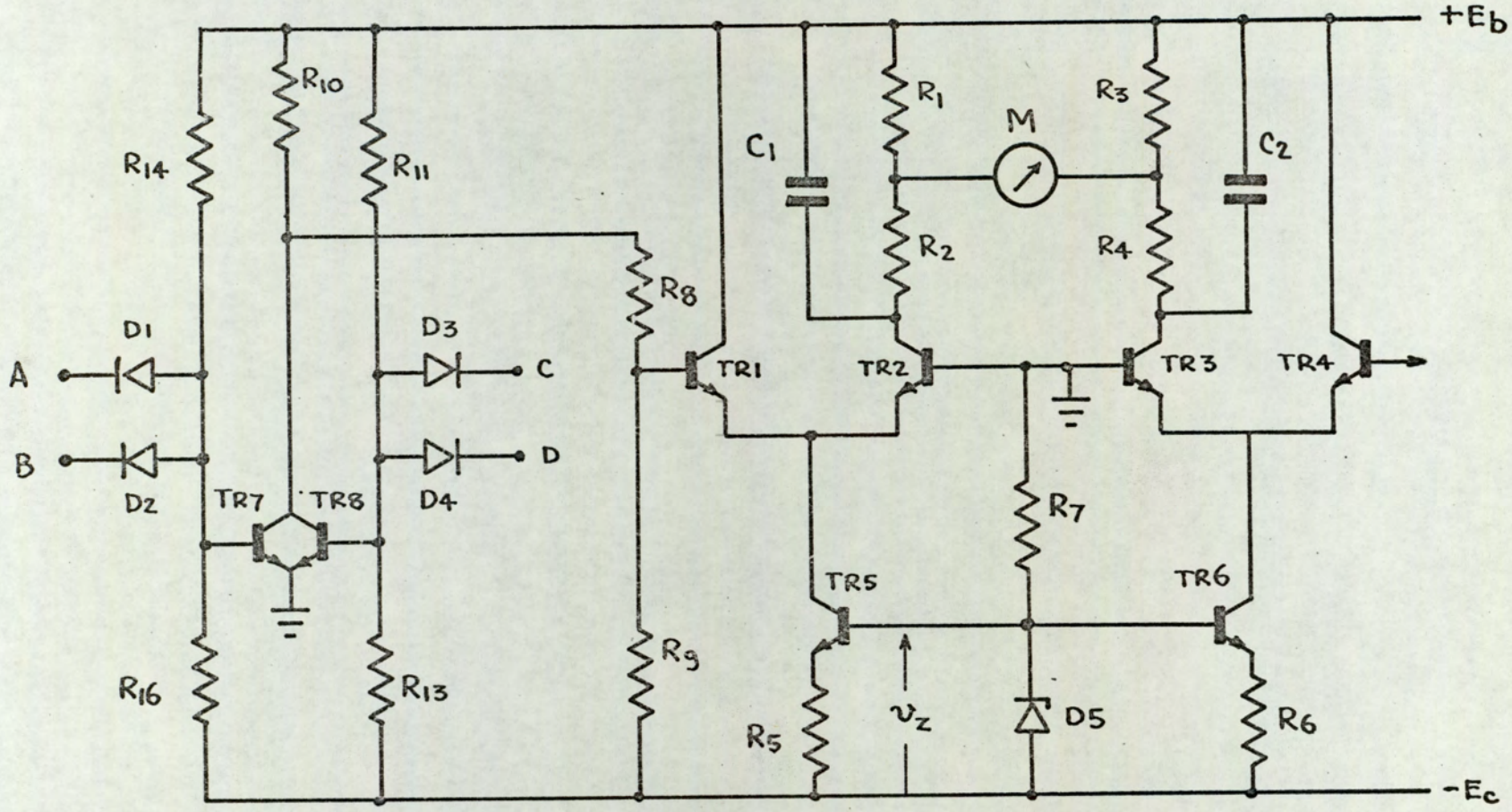


Fig. 46 Meter current generator

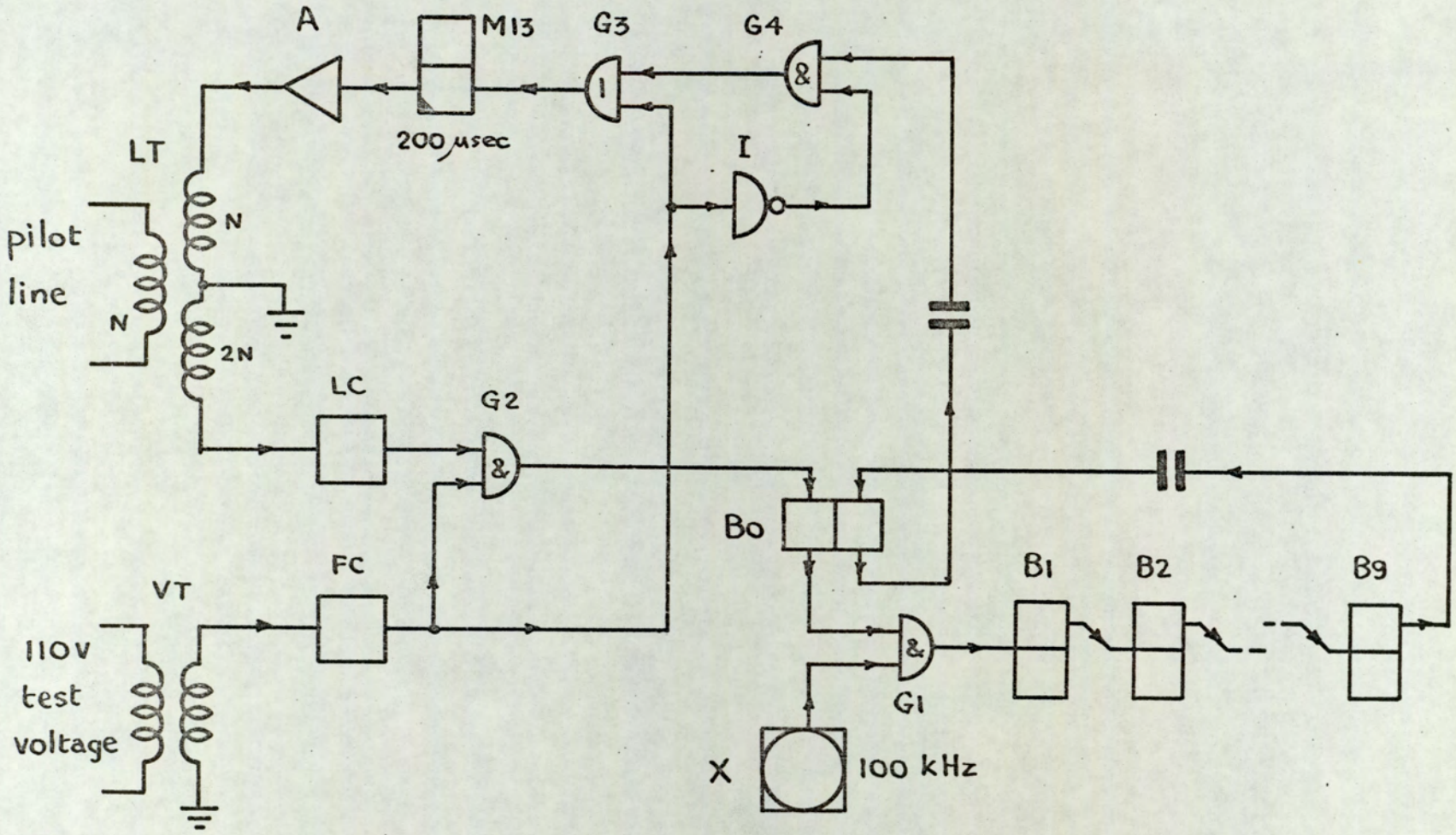


Fig. 47 M.S.E.V. Substation logic diagram

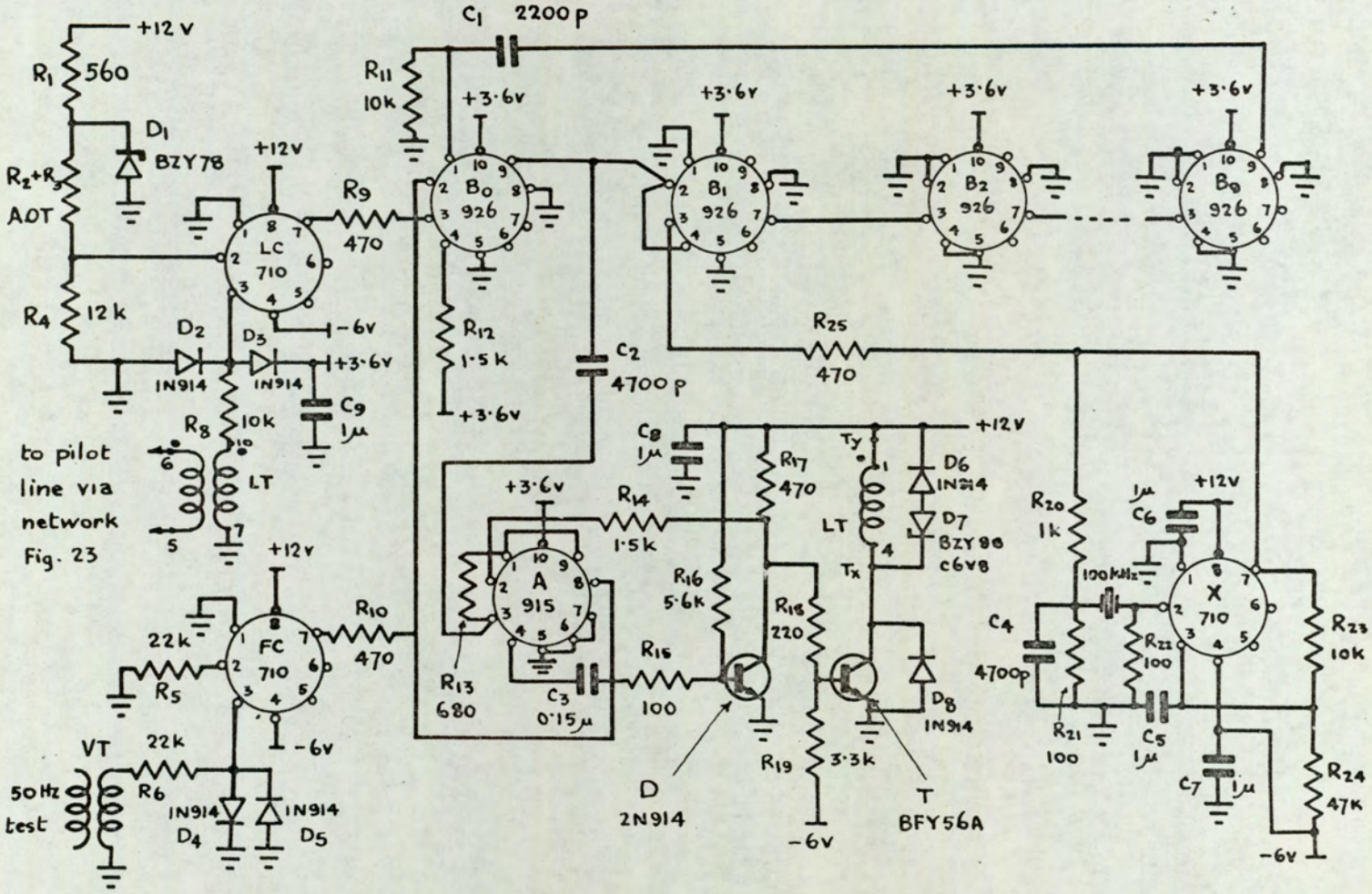


FIG 48

SUBSTATION UNIT CIRCUIT DIAGRAM

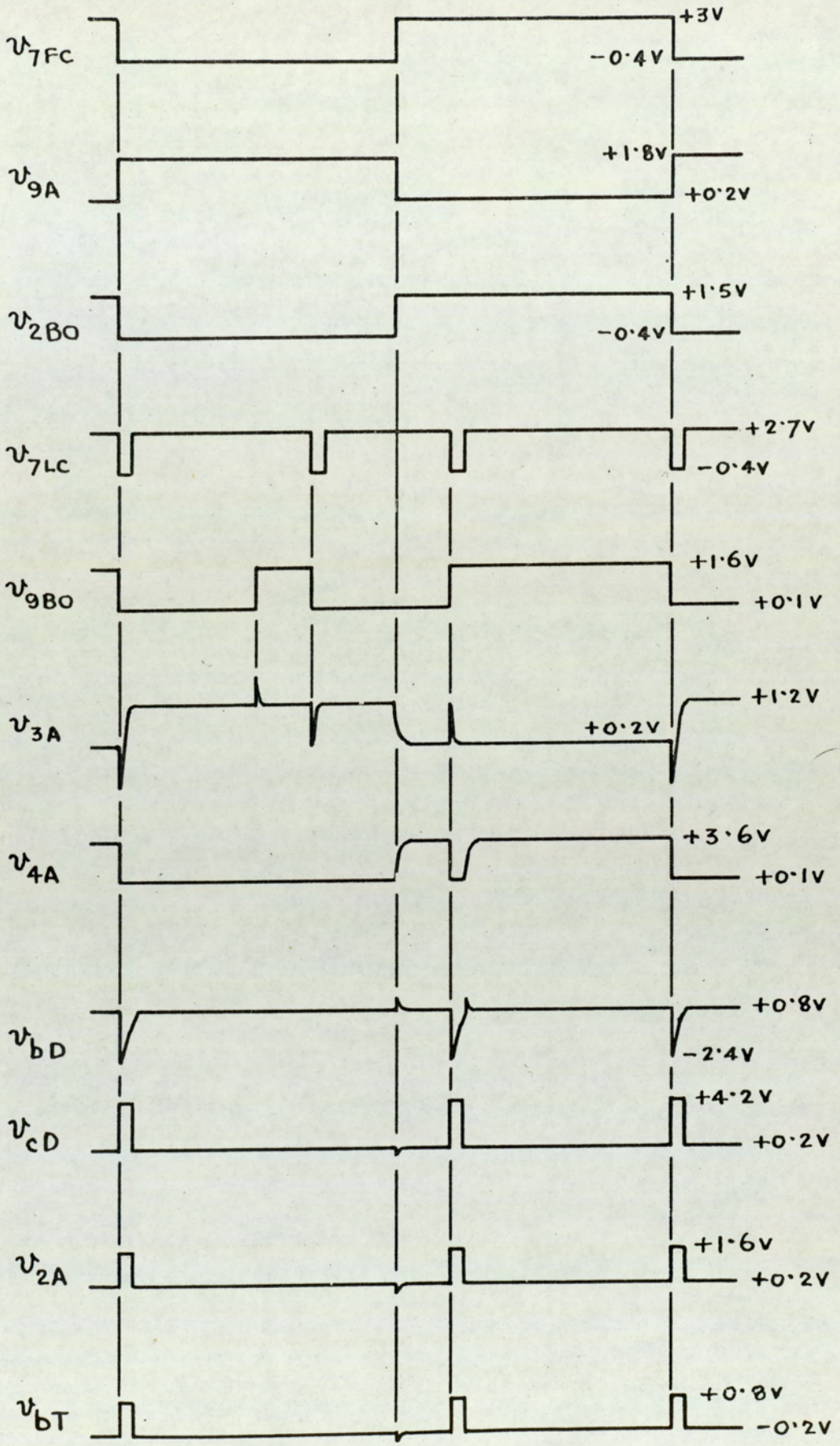


Fig. 49 Substation Voltage Waveforms

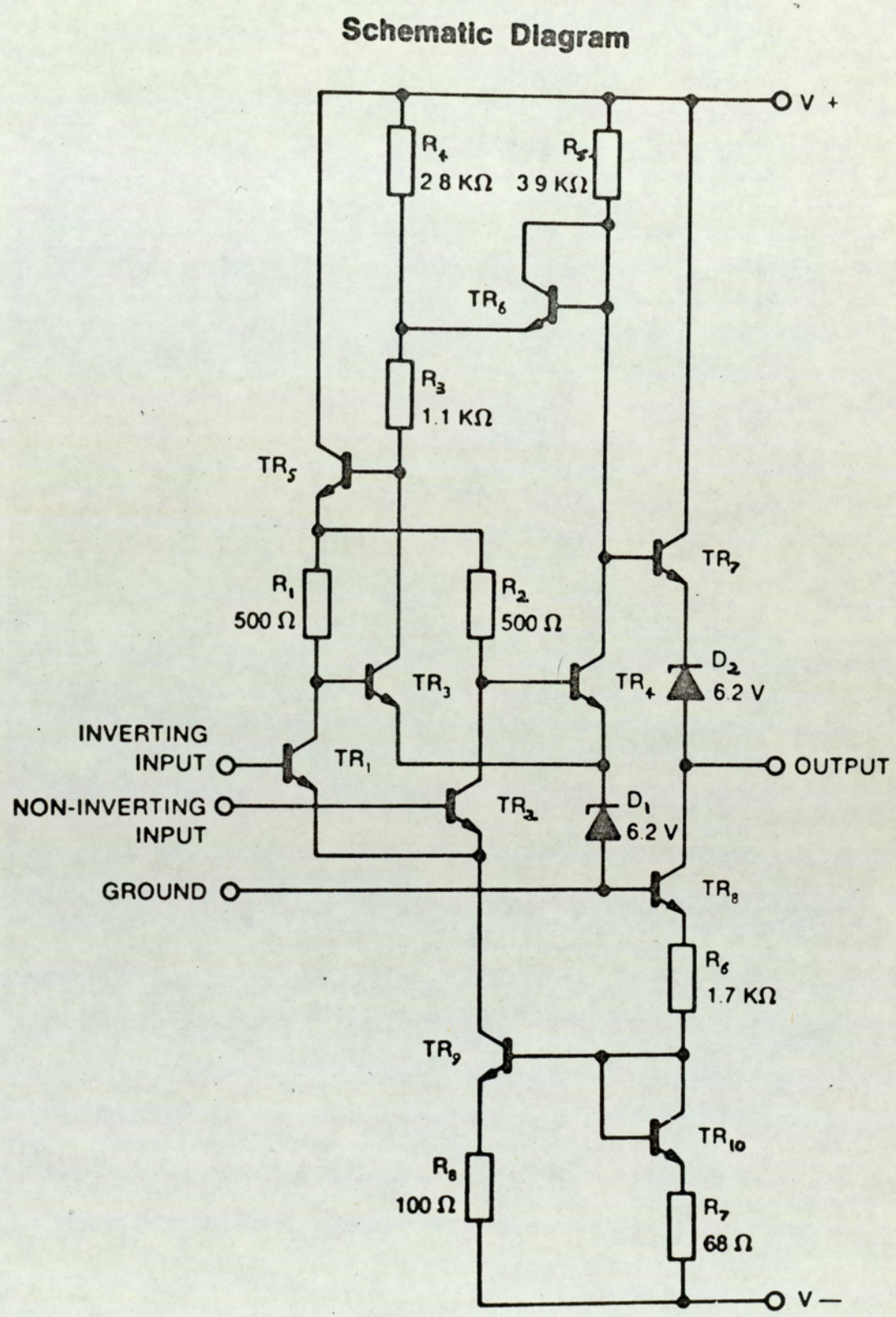


FIG 50. CIRCUIT DIAGRAM OF THE μA710

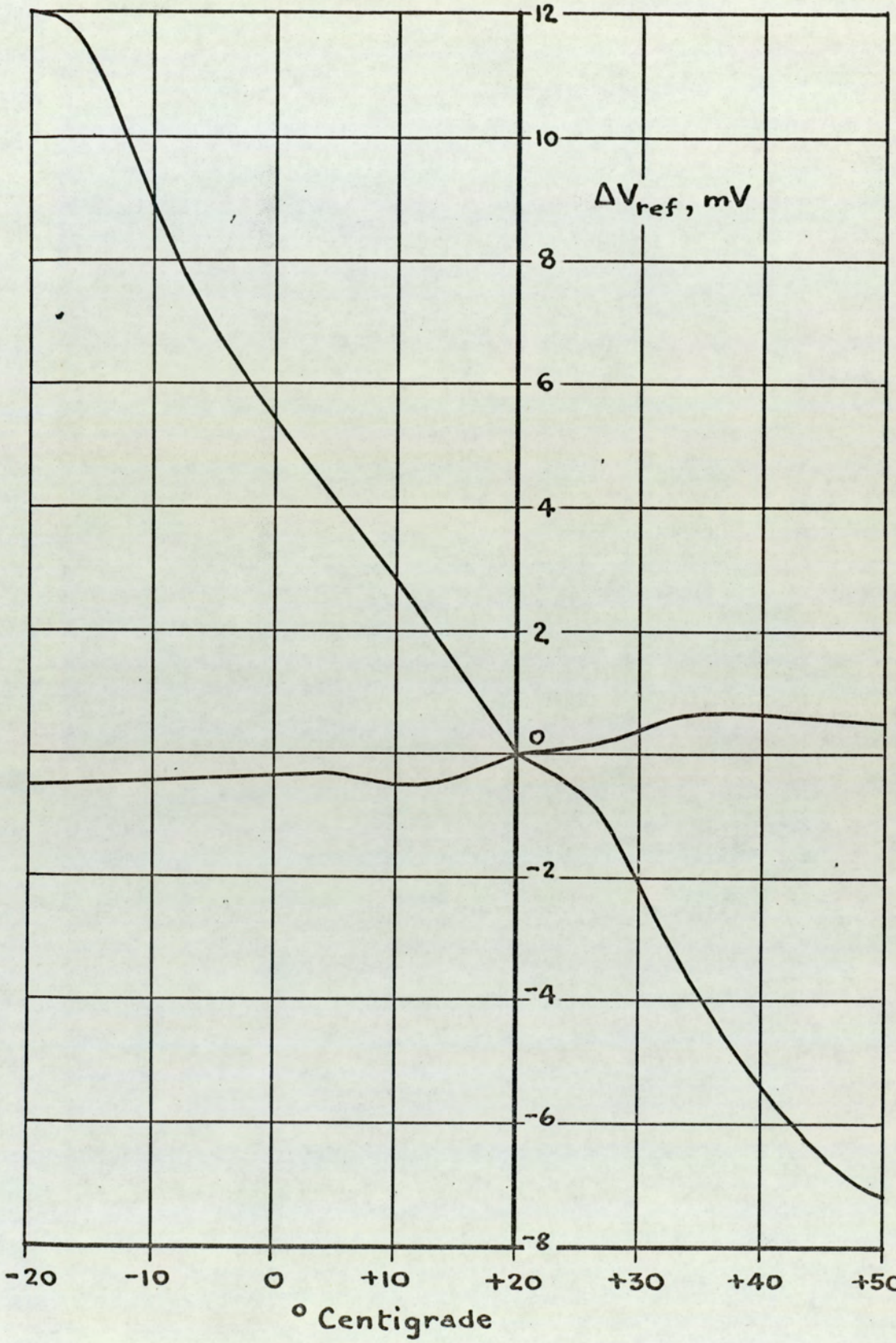
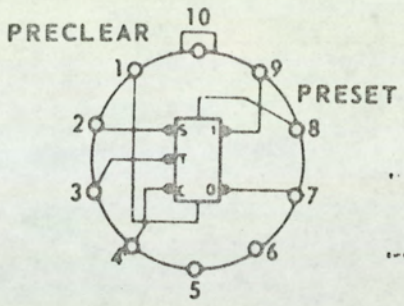


Fig. 51 Limits of ΔV_{ref} for 18 voltage comparators, plotted against temperature

FIG 53

JK FLIP-FLOP ELEMENT



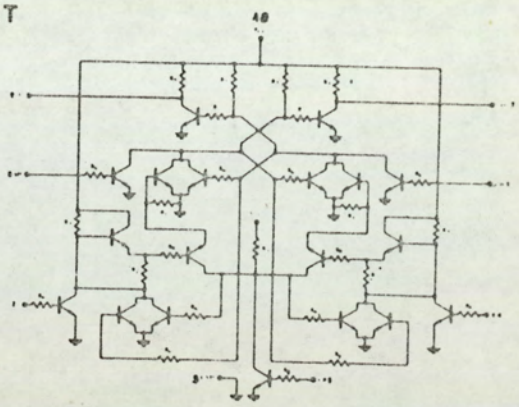
SET (2)	CLEAR (4)	OUTPUT (9)
t = n		t = n + 1
H	H	X^n
H	L	H
L	H	L
L	L	$\overline{X^n}$

H = HIGH

L = LOW

X IS THE OUTPUT STATE AT TIME n

JK FLIP-FLOP SCHEMATIC



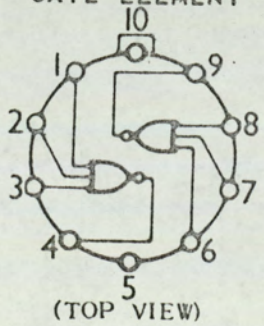
TYPICAL RESISTOR VALUES

$R_1 = 3K\Omega$ $R_3 = 900\Omega$ $R_5 = 640\Omega$ $R_7 = 550\Omega$

$R_2 = 1K\Omega$ $R_4 = 700\Omega$ $R_6 = 600\Omega$ $R_8 = 300\Omega$

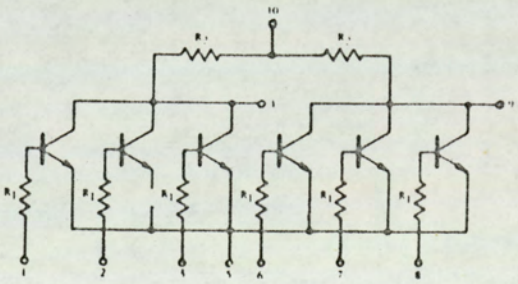
926 LOGIC ELEMENT

DUAL THREE-INPUT GATE ELEMENT



(TOP VIEW)

DUAL THREE-INPUT GATE SCHEMATIC



TYPICAL RESISTOR VALUES

$R_1 = 450\Omega$

$R_2 = 640\Omega$

915 LOGIC ELEMENT

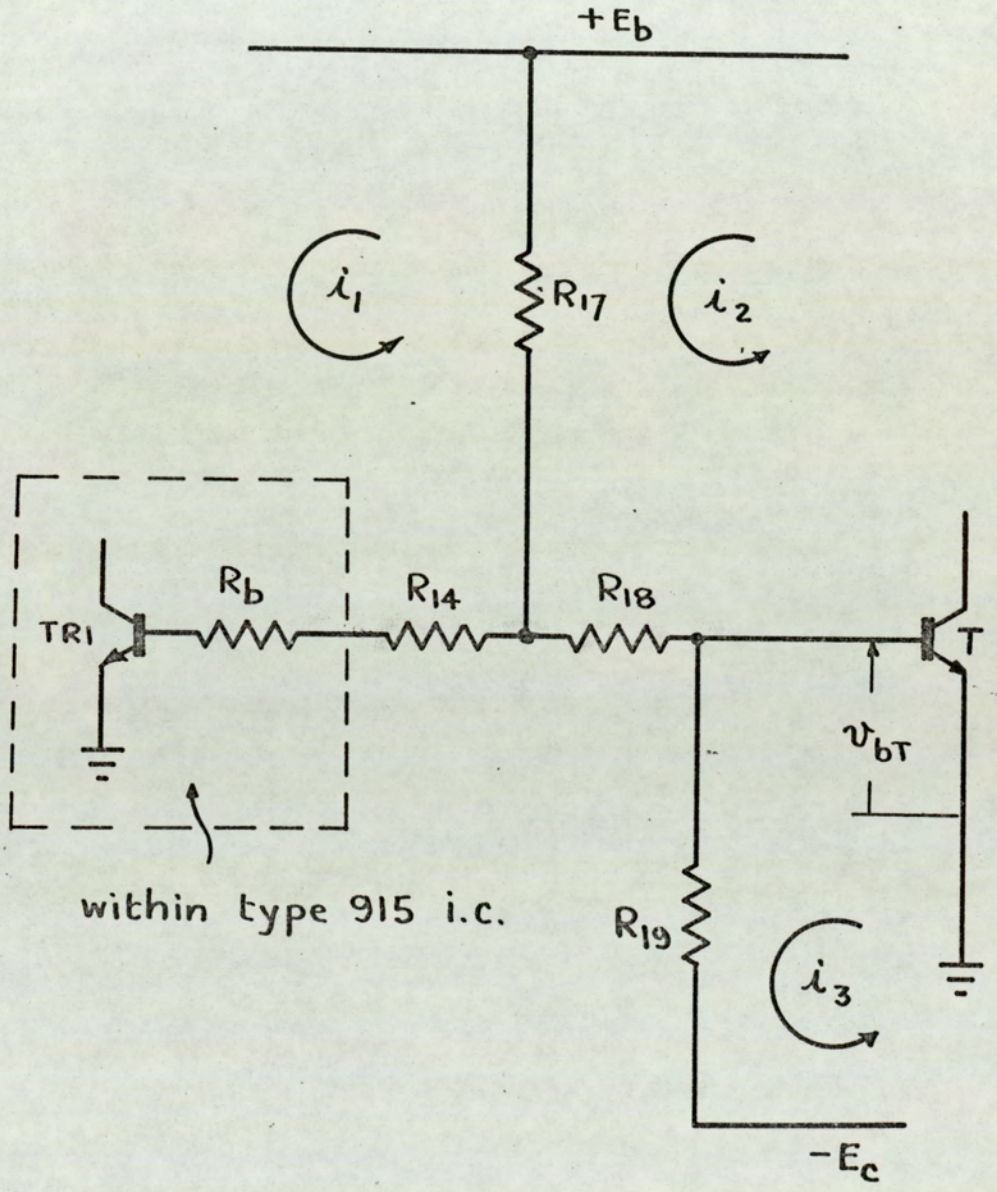


Fig. 54 Pulse generator design

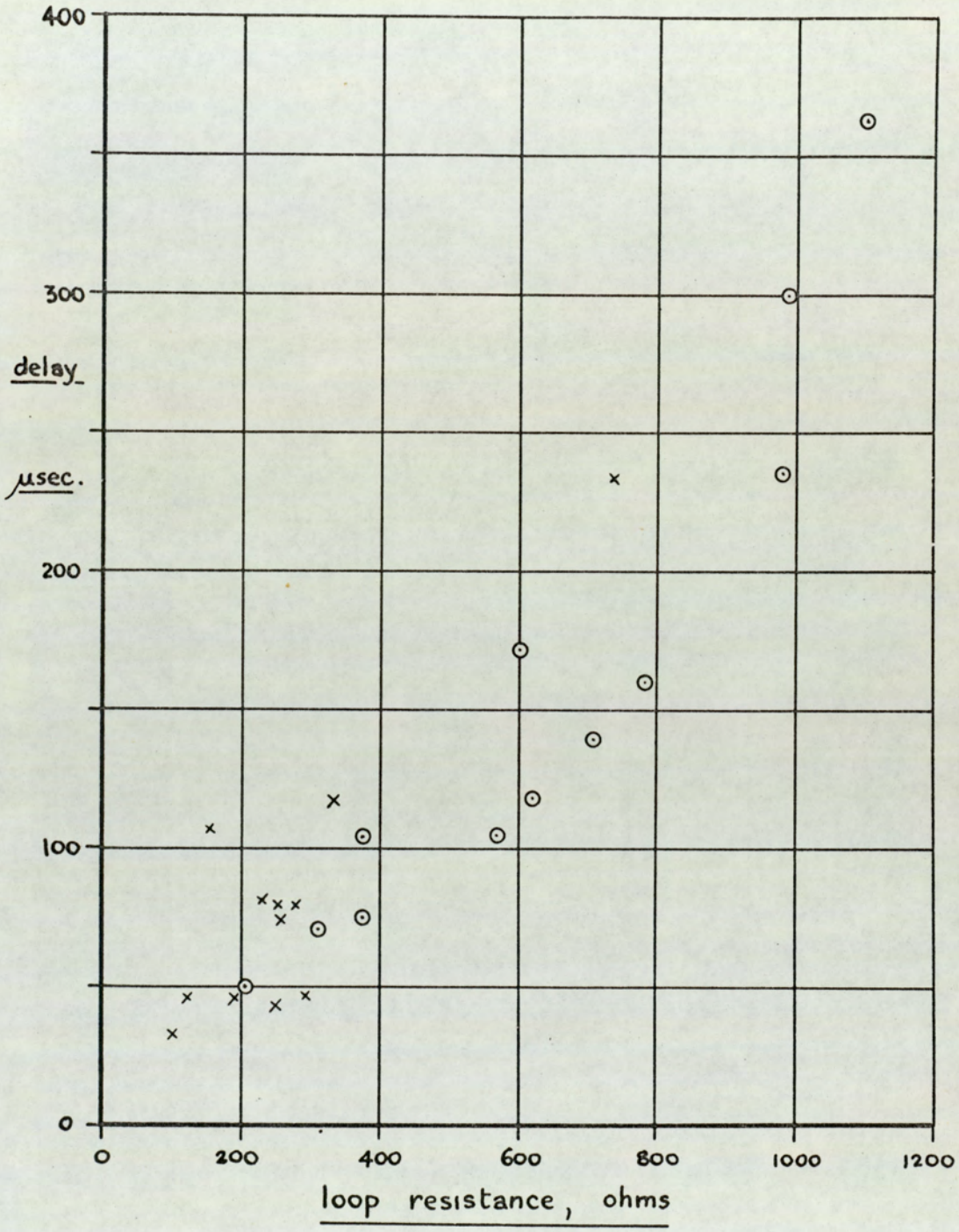
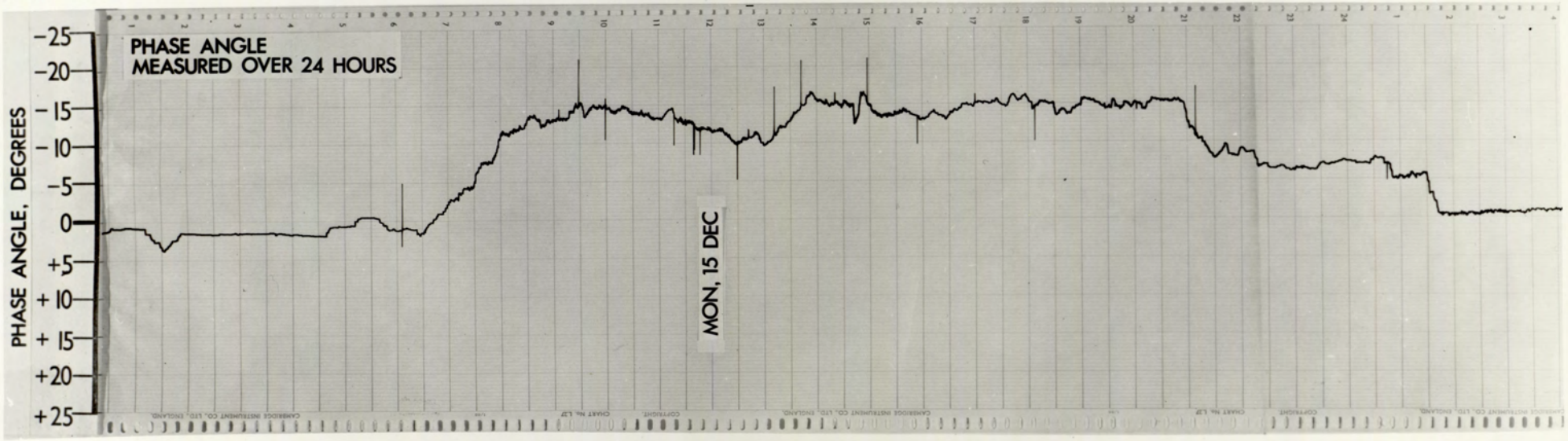


Fig.55

⊙ Lines tested in Laboratory
X Lines installed in Birmingham Area

FIG 56


PHASE ANGLE
MEASURED OVER 24 HOURS
PHASE ANGLE, DEGREES
-25
-20
-15
-10
-5
0
+5
+10
+15
+20
+25
MON, 15 DEC

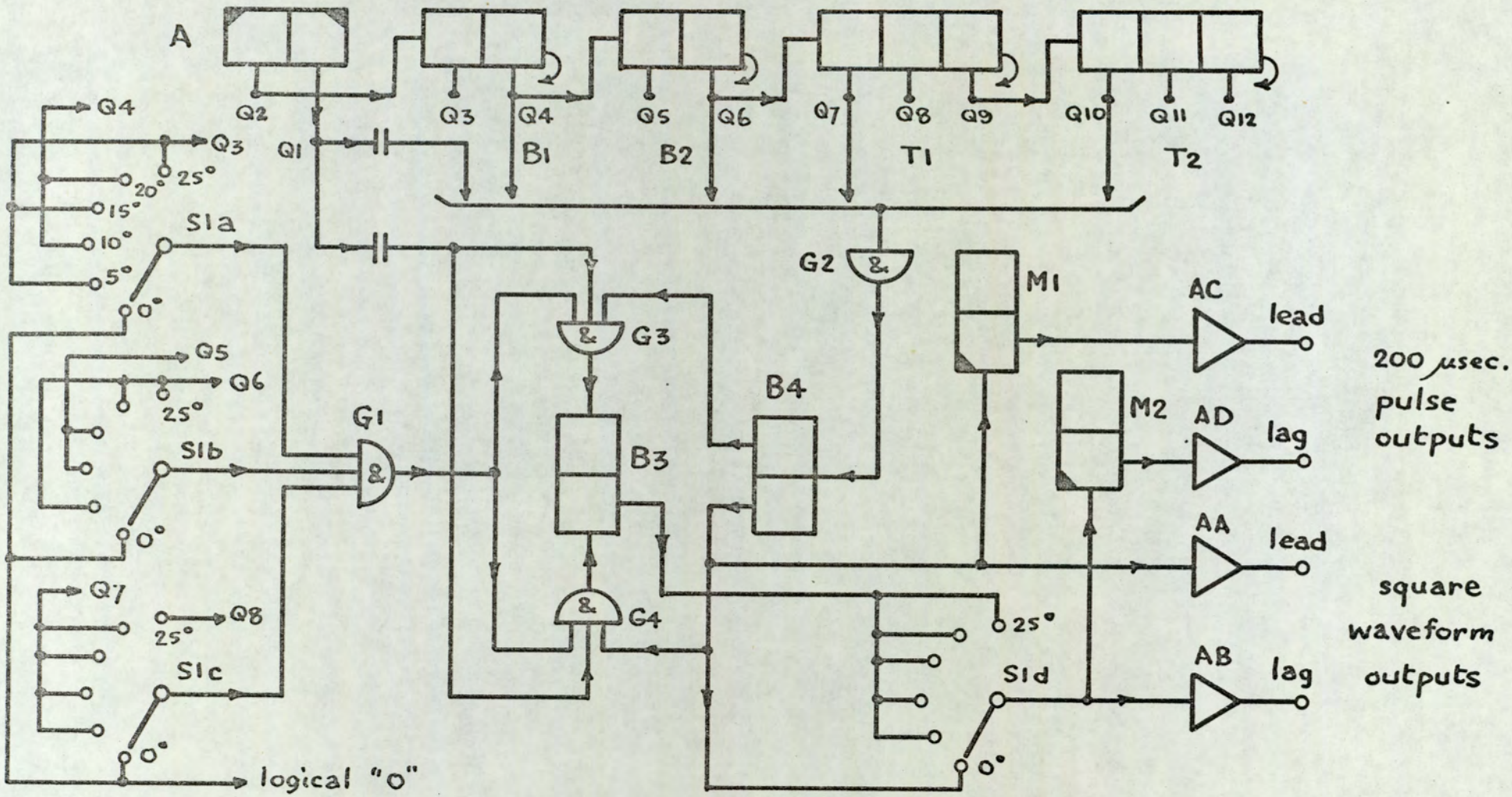


Fig. 57. Calibrator Logic Diagram

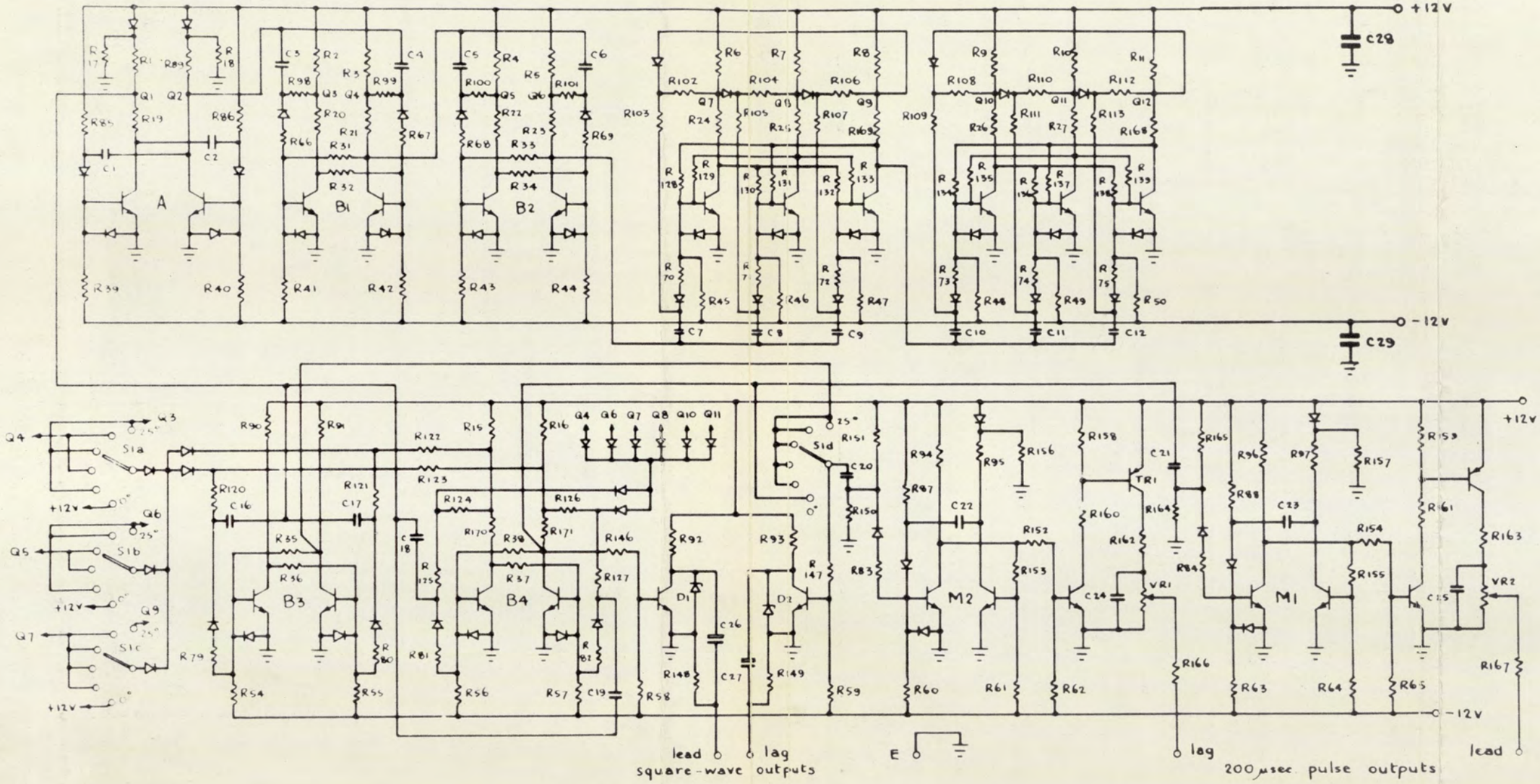


FIG 58

PHASE ANGLE CALIBRATOR CIRCUIT DIAGRAM

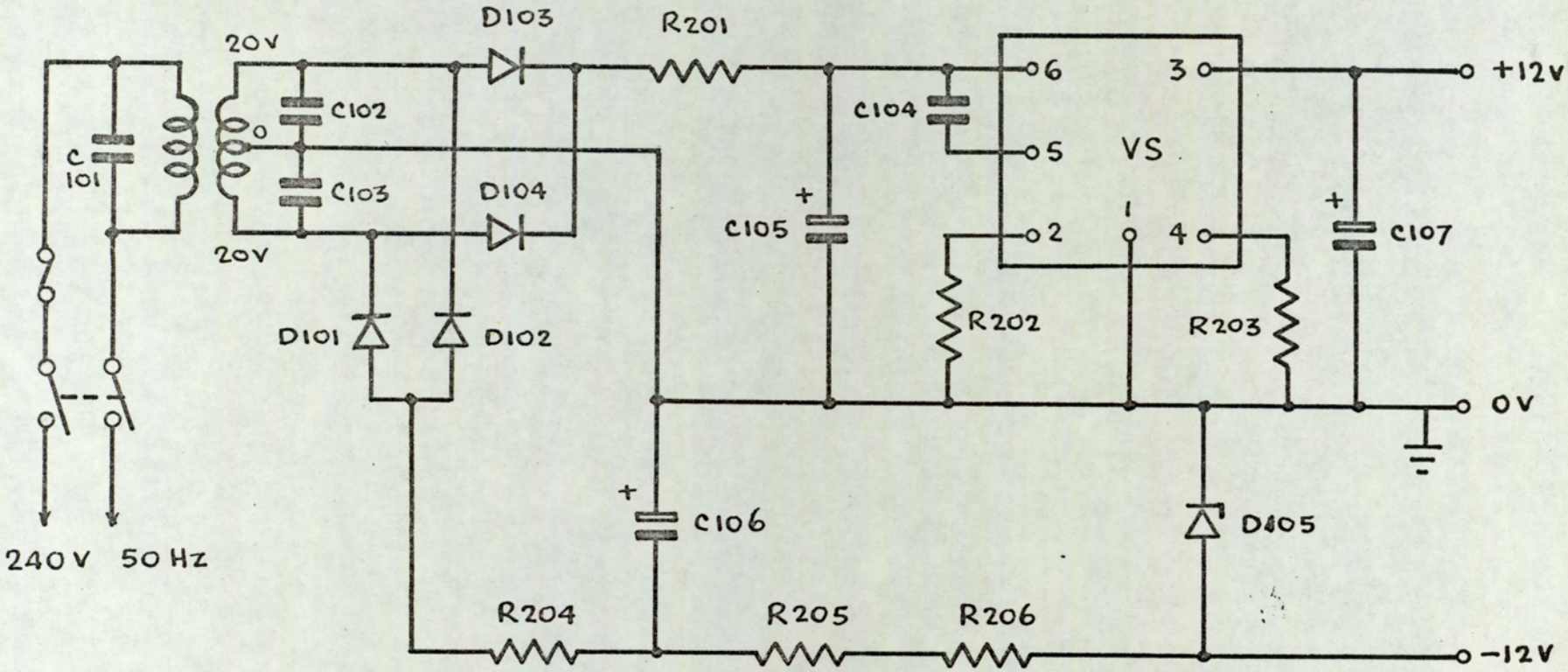


Fig. 59. Calibrator Power Supply

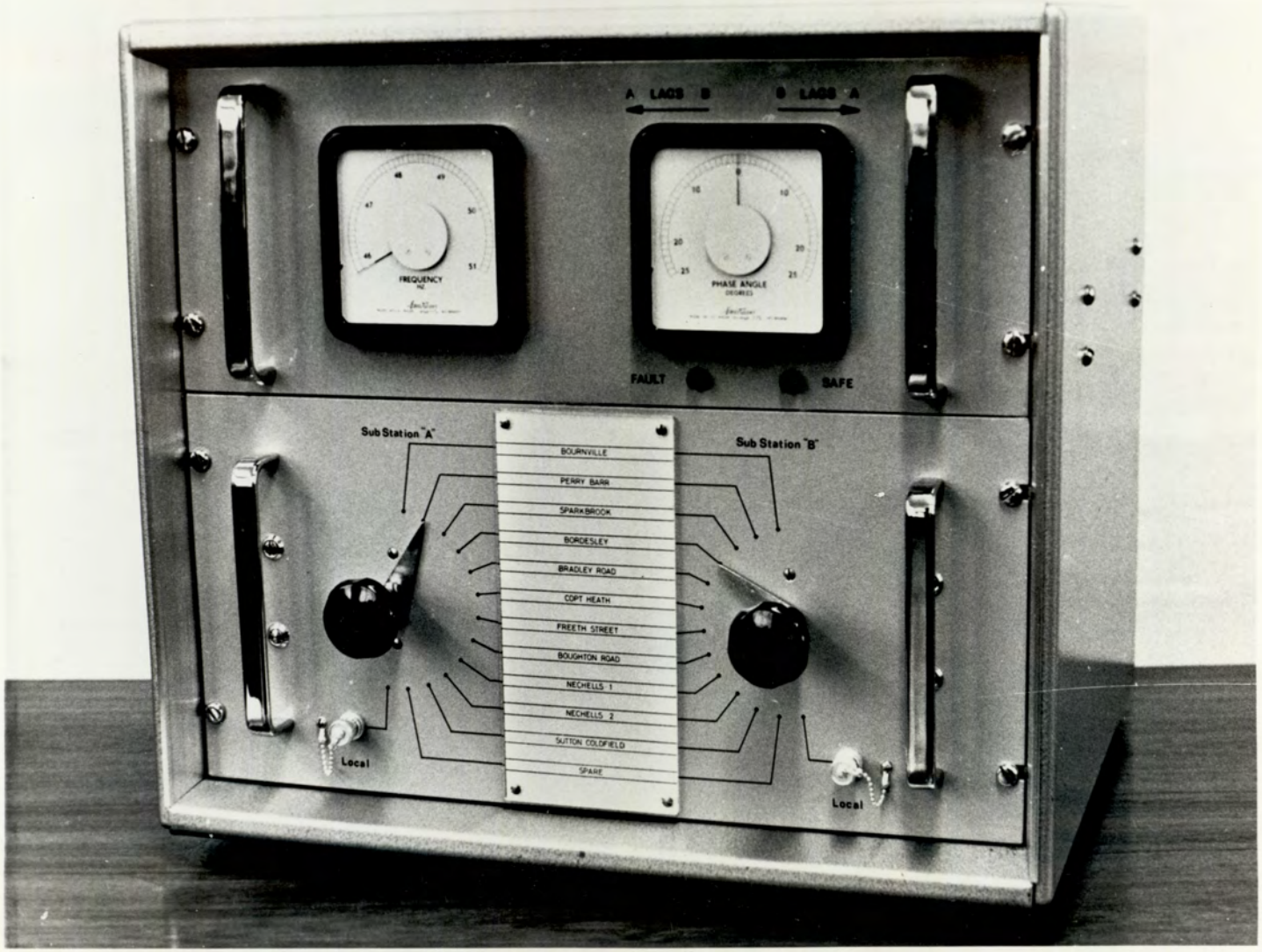


Fig. 60 Control Centre Equipment

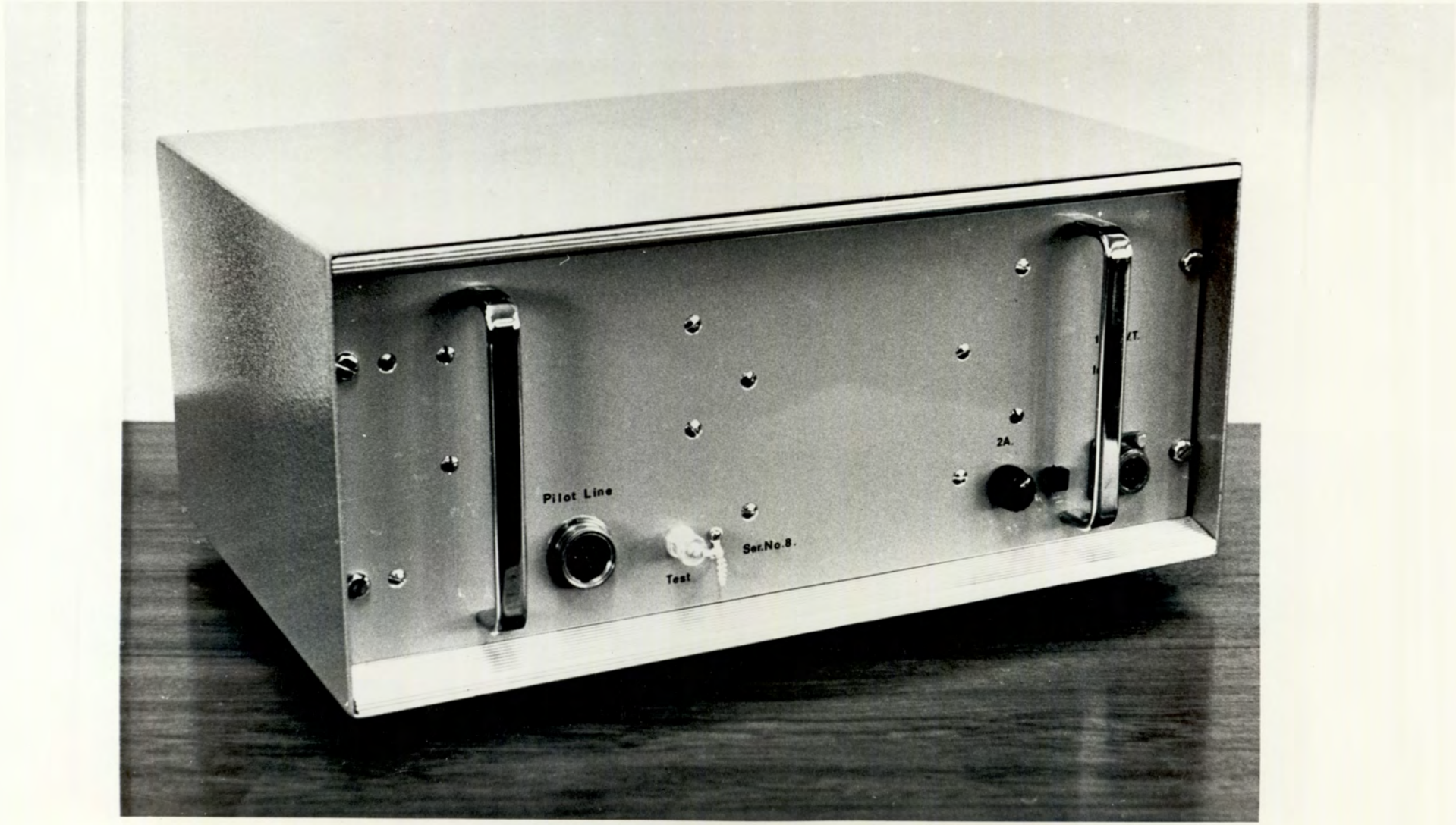


Fig. 61 Substation Equipment

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