Control Strategies for Low Voltage DC Microgrids

Ph.D. Thesis

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Thesis Summary

Increasingly, clean renewable energy sources such as wind power and solar power are supplementing and/or replacing, fossil fuels as inputs to electrical grids. Effective and efficient integration of such diverse energy sources, to their full potential, necessitates changes to the architecture and management of those grids. Microgrids provide an effective means for power distribution from renewable energy sources. DC microgrids are well suited to low voltage applications, and have advantages over AC microgrids, including simpler control, higher efficiency and no reactive power. Conventionally, DC microgrids are operated using a hierarchical control scheme. However, complicated control structures add to the cost of microgrids, and limit their application to electrifying remote and developing areas. This thesis focuses on the control of DC microgrids. A set of control strategies based on a modified hierarchical control scheme is proposed for household applications with power coordination, stability enhancement and plug and play performance.

First, a dual-window DC bus interacting method is proposed as a replacement for conventional communication infrastructure. It utilises the advantages of both droop control and DC bus signalling methods. Droop control has plug and play performance and DC bus signalling has the function of automatic power regulation. Low bandwidth signalling between distributed sources can be achieved by manipulating relationships between droop coefficients. With the proposed DC bus interacting method, coordination and power management of distributed energy sources in the absence of communication infrastructure in a DC microgrid may be achieved.

Second, a passive stabiliser is proposed for the primary controller to compensate non-minimum phase in interface converters. The stability performance of an interface converter in a DC microgrid can be optimised by adjusting the feedforward gain in a passive stabiliser. This affects the quiescent operating point and therefore a modified feedforward controller is used in this system. Consequently, potential instability caused by non-minimum phase can be avoided. As a by-product, the passive stabiliser can reduce the required size of the terminal capacitor.

Third, a novel hierarchical control scheme is implemented in a low voltage DC microgrid bench. The passive stabiliser is applied in the primary layer, droop control in the secondary layer, and a six-bit signal series based on the dual-window DC bus voltage interacting method is applied in tertiary layer for power flow control. The impact of bidirectional power flow on battery banks in the system is discussed based on the terminal input admittance analysis. In addition, the small signal model of terminal output admittance under the proposed the passive stabiliser is built. It shows that the proposed system is stable under all possible working modes based on the minor loop gain analysis. The on-grid and off-grid operation modes are conducted, and seamless transfer between them can be achieved. Especially, the surplus power from PV generations is limited, for the power balance consideration, by the proposed modified MPPT algorithm when the system operates under off-grid mode.

Key words: DC microgrids, DC bus interacting control, passive controller, terminal admittance, plug and play.

Dedication

To my beloved parents,

For their love and support

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Abbreviations

Abbreviations	Full meaning
ac	Alternate current small signal analysis
AC	Alternating current
CC	Central controller
CPL	Constant power load
CPS	Constant power source
CS	Current source
DBI	DC bus interacting
DBS	DC bus signalling
DC	Direct current
DES	Distributed energy source
DG	Distributed generator
DoA	Domain of attraction
DOA	Design-oriented analysis
DS	Distributed source
DSP	Digital signal processor
ES	Energy storage
ESAC	Energy source analysis consortium
EV	Electrical vehicle
GMPMC	Gain margin and phase margin criterion
HPF	High pass filter

HV	High voltage
IC	Interface converter
LBC	Low bandwidth communication
LTI	Linear time invariant
LPF	Low pass filter
MAC	Multi-agent control
MGF	Mason's gain formula
MLG	Minor loop gain
MSC	Master slave control
MV	Medium voltage
NIR	Negative incremental resistance
NMP	Non-minimum phase
OAC	Opposing argument criterion
PCB	Printed circuit board
PLC	Power line communication
PLS	Power line signalling
POCC	Point of common coupling
PoL	Point of load
PU	Per unit
PV	Photovoltaic
RES	Renewable energy source
RESC	Root exponential stability criterion
SISO	Single input single output
SoC	State of charge
SVC	Supervisory control
VLS	Voltage level signalling
VS	Voltage source

Symbols

Chapter 2

i_{ok}	Output current
v'_k	Voltage reference for the controller
v^*_k	Nominal voltage
R^{iv}_k	Virtual resistance (or droop coefficient) based on output current
k	The k-th converter connected in the system.
R^{Pv}_k	Virtual resistance (or droop coefficient) based on output power
Δv	Small variations of bus voltage
v	Bus voltage
Δi	Small variations of input current to the constant power load
i	Input current to the constant power load
P	The power of CPL
G_{vd}	Control to output voltage transfer function of interface converter
Z_o	Output impedance of filter
Z_i	Input impedance of interface converter
Z_N	The input impedance $Z_i(s)$ under the condition that the controller varies the duty cycle to maintain the output voltage variation as much close to zero as possible
Z_D	Input impedance $Z_i(s)$ under the condition that duty cycle is equal to zero
T	Closed loop gain
T_{MLG}	Minor loop gain
G_a	Stable line transfer function of source subsystem

G_b	Stable line transfer function of load subsystem
V_{1a}	Input voltage of source subsystem
V_{2a}	Output voltage of source subsystem
V_{1b}	Input voltage of load subsystem
V_{2b}	Output voltage of load subsystem
Z_{bus}	Total bus impedance

Chapter 4

v_1'	Voltage reference for the control loop of interface converter 1
v_2'	Voltage reference for the control loop of interface converter 2
v_1^*	The nominal voltage (or floating voltage) of interface converter 1
v_2^*	The nominal voltage (or floating voltage) of interface converter 2
i_{o1}	The converter output current of interface converter 1
i_{o2}	The converter output current of interface converter 2
R_{v1}	Virtual resistance (or droop coefficient) of interface converter 1
R_{v2}	Virtual resistance (or droop coefficient) of interface converter 2
v_T^*	Top floating voltage for the control loop voltage reference
v_B^*	Bottom voltage that allowed to reach with the droop coefficient R_v
i_{max}	Maximum allowed output current
P_{max}	Maximum output power
i_{neg}	Negative current over two converters interactions period
v_S	Signal voltage
P_2	Power capability of interface converter 2
P_L	Total load power
i_{Lc}	Dedicated inner loop current reference
v_{bus}^{PU}	Bus voltage in per unit
v_s^{PU}	Signal voltage in per unit
R	Resistance load

Chapter 5

f_s	Switching frequency of Boost converter
s	s domain
L	Converter inductor
C	Converter capacitor
i_L	Inductor current
v	Output voltage/capacitor voltage
v_g	Input source voltage
i_o	Output current after capacitor
d	Duty cycle
d'	The compensation of duty cycle, which is equal to $1 - d$
D	Steady state duty cycle
D'	The compensation of steady state of duty cycle, which is equal to $1 - D$
R	Equivalent load resistance
G_{vd}	Control to output voltage transfer function of converter
G_{id}	Control to inductor current transfer function of converter
G_{vg}	Input voltage to output voltage transfer function of converter/line transfer function of converter
G_{ig}	Input voltage to inductor current transfer function of converter
Δv	Small variations of output voltage
Δv_c	Small variations of inductor current reference in voltage form
Δd	Small variations of duty cycle
i_L^*	inductor current reference
Δi_L^*	Small variation of inductor current reference
Δi_L	Small variations of inductor current
R_f	Current sampling coefficient/resistor
G_{vc}	Transfer function of inductor current reference to output voltage.
K	Passive stabiliser gain
G_p	Passive controller

G'_{vc}	Compensated transfer function of inductor current reference to output voltage.
G_{ci}	Current loop controller/compensator
G_{cv}	Voltage loop controller/compensator
ω_z/f_z	Numerator zero frequency of inner current loop controller
ω_p/f_p	Dominator pole frequency of inner current loop controller
ω_{zv}/f_{zv}	zero frequency of outer voltage loop controller
δ/f_{pa}	Crossover frequency of passive controller
f_N	The frequency that enters negative part in G_{vc}
T_{sp}	Sampling time/period
$\bar{V}$	Steady state value of output voltage
$\bar{I_L}$	Steady state average value of inductor current

Chapter 6

$Y_T^{P\&D}$	Terminal admittance with passive and droop controllers
Y_T^P	Terminal admittance with passive controller
Y_T^D	Terminal admittance with droop controller
Y_T^{dbl}	Terminal admittance with initial double loop controllers
$Y_T^{Bat\_CPL}$	Terminal admittance for battery working constant current/power mode
Y_T^{bus}	Total terminal admittance of DC microgrids
v_{lim}	The voltage that indicates PV step into power limitation mode
v_{PV}	PV input voltage
i_{PV}	PV input current

Chapter 1 Introduction

The increasing use of renewable energy sources requires a more effective and efficient power distribution structure. Microgrids, an effective power distribution structure for renewable energy sources, are an active research topic.

In this Chapter, the increased use of renewable energy sources during the past decade (2007-2017) is analysed from both UK and worldwide perspective. AC and DC microgrids are introduced and compared. In particular, the development and application of DC microgrids are illustrated, which is because DC microgrids form the topic of this thesis. Finally, the motivation for and structure of this thesis are stated.

1.1 Background

Demand for clean energy is increasing. In addition to creating pollution, fossil fuel energy resources are finite. The use of renewable energy sources (RESs), e.g. wind power, solar power, and hydro power, changes the energy consumption structure globally.

Renewable power generations[1] have grown rapidly in the past decade [1], as shown in Figure 1.1 and Figure 1.2. Europe, North America and the Asia Pacific area make the majority of contributions[2] whereas in areas such as Africa, utilisation of RESs is still quite low. Spare population distribution and inactive economy could be reasons for low utilisation of RESs. Since

[1] It mainly refers to wind power and solar power in this thesis.

[2] Data based on BP in the reference [1].

2010, IEEE Smart Village [2] has started their efforts on empowering off-grid villages, and acts as the catalyst for socioeconomic and technological change in remote areas of Africa, India, and the South Pacific.

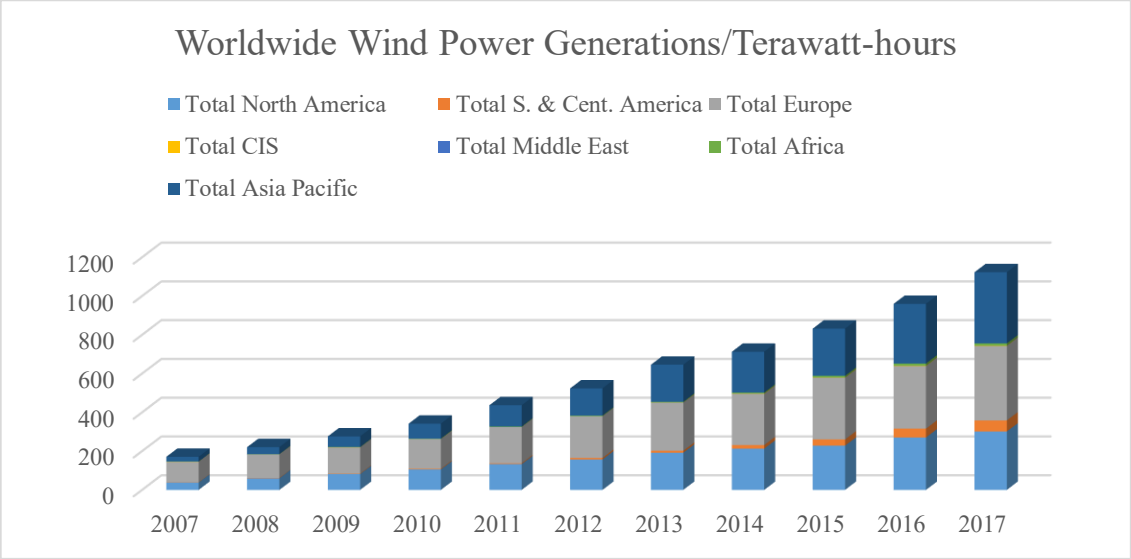


Figure 1.1 Worldwide wind power generations from 2007 to 2017.

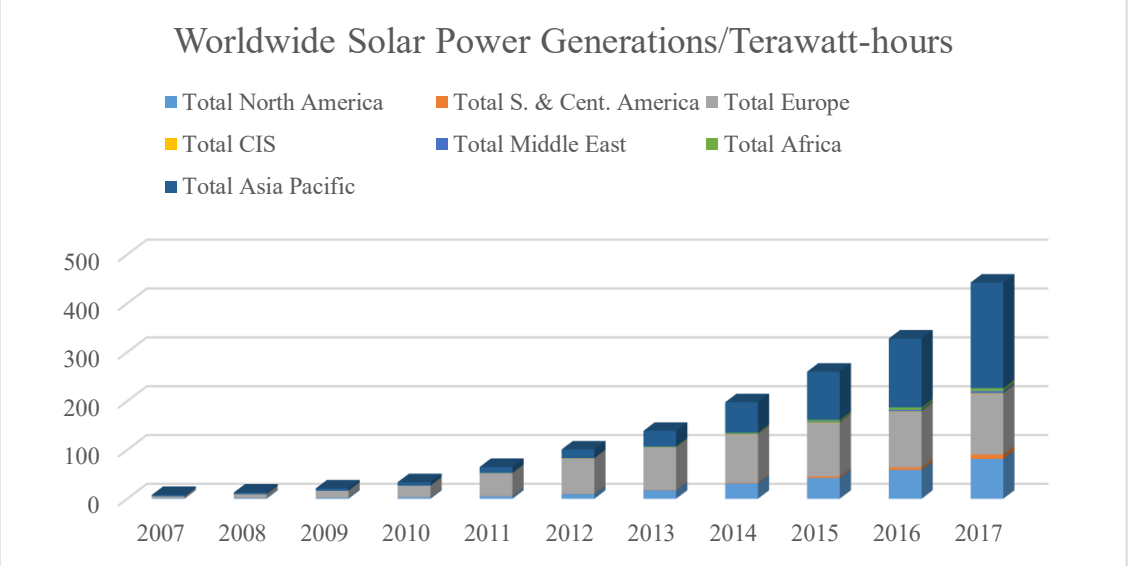


Figure 1.2 Worldwide solar power generations from 2007 to 2017.

In the UK, use of RESs is increasing [3] and their electricity contribution has grown rapidly in the past decade, as shown in Figure 1.3[1]. RESs benefit from developments in power electronic

[1] Data based on UK energy statistics in reference [3].

technology and from cost reductions in power switching devices, PV generations and wind turbines.

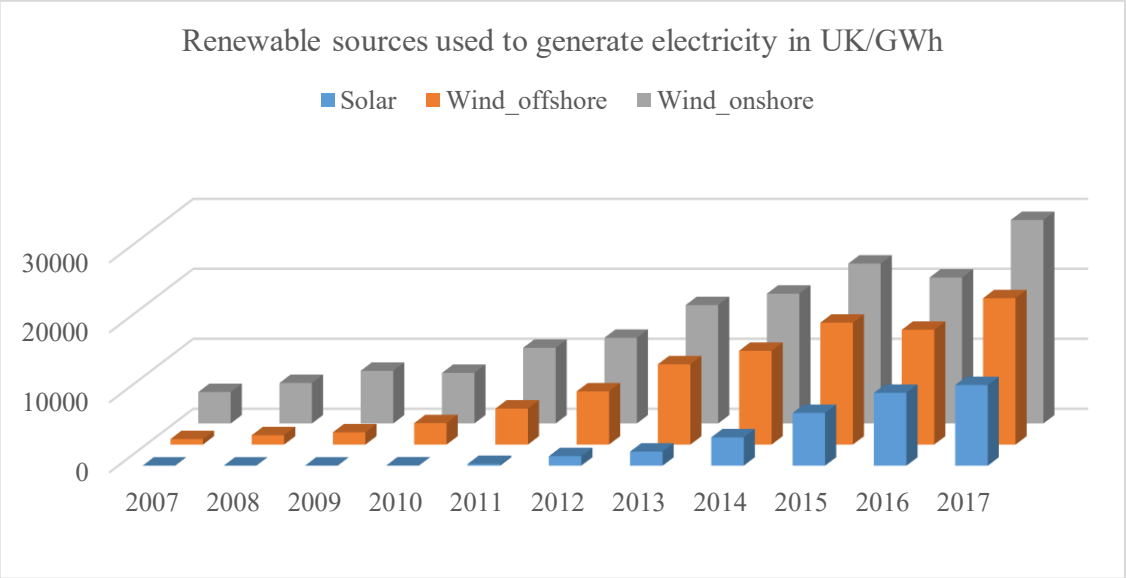


Figure 1.3 Wind and solar energy electricity contribution in UK from 2007 to 2017.

The adoption of distributed RESs requires changes to the conventional power distribution structure, which has only single way power flow. Environmental factors including variation of wind flow and solar irradiance, make power generation by RESs unpredictably intermittent and discontinuous, and thereby influence and stress peak power regulation and management. Typically, RESs are connected to the utility grid through power electronic devices. High frequency harmonics caused by power converters may lower the power quality and interact with filters on the power line so as to threaten the stability of the system.

Driven by above concerns, a new and effective power distribution structure for distributed energy sources is required. Microgrids are proposed in this role.

1.2 Definition and Configuration of Microgrid

The concept of a microgrid is proposed by Prof. Lasseter [4].

> *It assumes a cluster of loads and distributed micro-sources operating as a single controllable system that provides both power and heat to its local area.*

A typical microgrid is shown in Figure 1.4. The distributed energy sources and loads are connected together through the same power line. The microgrids subsystem can then be connected together through point of common coupling (POCC) [5]. They can be connected with the utility grid through an interface converter/inverter.

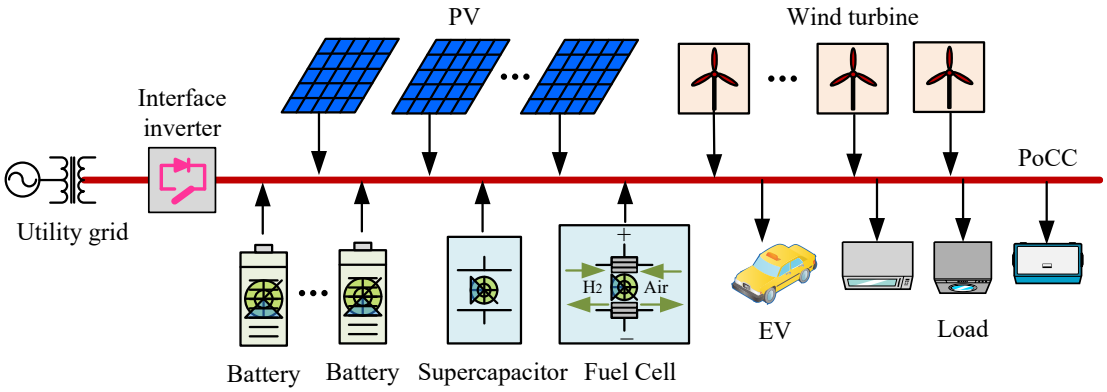


Figure 1.4 A typical microgrid configuration.

A typical low voltage microgrid usually contains the following parts [5][6].

- *Distributed energy sources*

Distributed energy sources (DESs) may include renewable energy sources, such as solar power, wind power, hydro power, biomass power (such as fuel cell), or thermal power.

- *Energy storage*

Energy storage (ES) devices include electrochemical energy storage devices, e.g. lead-acid batteries, lithium-ion batteries, electrical energy storage devices, e.g. supercapacitors and mechanical energy storage devices, e.g. compressed air and flywheels.

- *Interface to utility grid*

The utility grid refers to the mains grid. Microgrid system can operate at the grid connected mode and off-grid mode. Off-grid mode is also called isolated/islanded mode [7].

- *Power load*

Power loads can be uncontrollable, e.g. residential (home appliances) or controllable, which are able to participate in the power management in microgrids, e.g. electrical vehicles (EVs).

1.2.1 AC and DC microgrids

The common power bus in a microgrid may be either AC or DC [8]. The relationship of microgrids with conventional utility grid is shown in Figure 1.5.

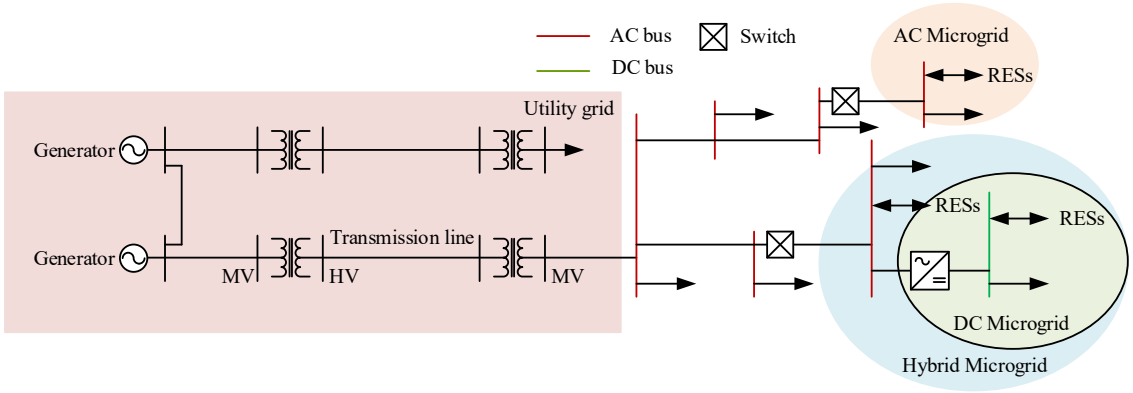


Figure 1.5 Power distribution structure.

Utility grid is still the main composition of current power distribution architecture. Microgrids are used to work as the sub-stream of power distribution to manage the RESs and provide power to the local loads. AC and DC microgrids can be integrated to form hybrid microgrids. An interface converter is required to link the AC and DC buses. This interface converter can naturally link or isolate the DC microgrid without additional switch/breaker.

In past decades, AC microgrids have been widely investigated to line up with the existing power system infrastructure. A typical AC microgrid system is shown in Figure 1.6. The RESs are all connected to the common AC bus through power electronics converters, which enable the stable coupling with AC networks [9]. AC loads can be directly connected to the AC bus while AC to DC converters are needed to power the DC loads.

However, many distributed sources and energy storages, such as PV generations, battery banks, supercapacitors, etc., are naturally based on DC. They need additional DC to AC inverters to regulate their voltage to AC so that they can be connected to the common AC bus. Even for the wind turbines, although they can generate AC output, their frequency varies and is not the same as the utility grid. Consequently, they still need to be converted to DC first and then connected to a common AC bus through inverters. Therefore, configuring a DC bus can save the interface

converters cost and reduce the complexity of the system. Besides, it has no frequency in DC system, which enables DC microgrids free from complex control of frequency and synchronisations. A typical DC microgrid configuration is shown in Figure 1.7. DC loads can be directly connected to the DC bus. An interface inverter is required to link the DC microgrid with the conventional grid.

Compared with AC microgrid, the advantages of DC microgrid are summarised as follows [9][10]:

- Higher efficiency of energy utilization due to the reduction of converters;
- No reactive power, harmonics and synchronisations;
- Easier controls and integration of various DC RESs.

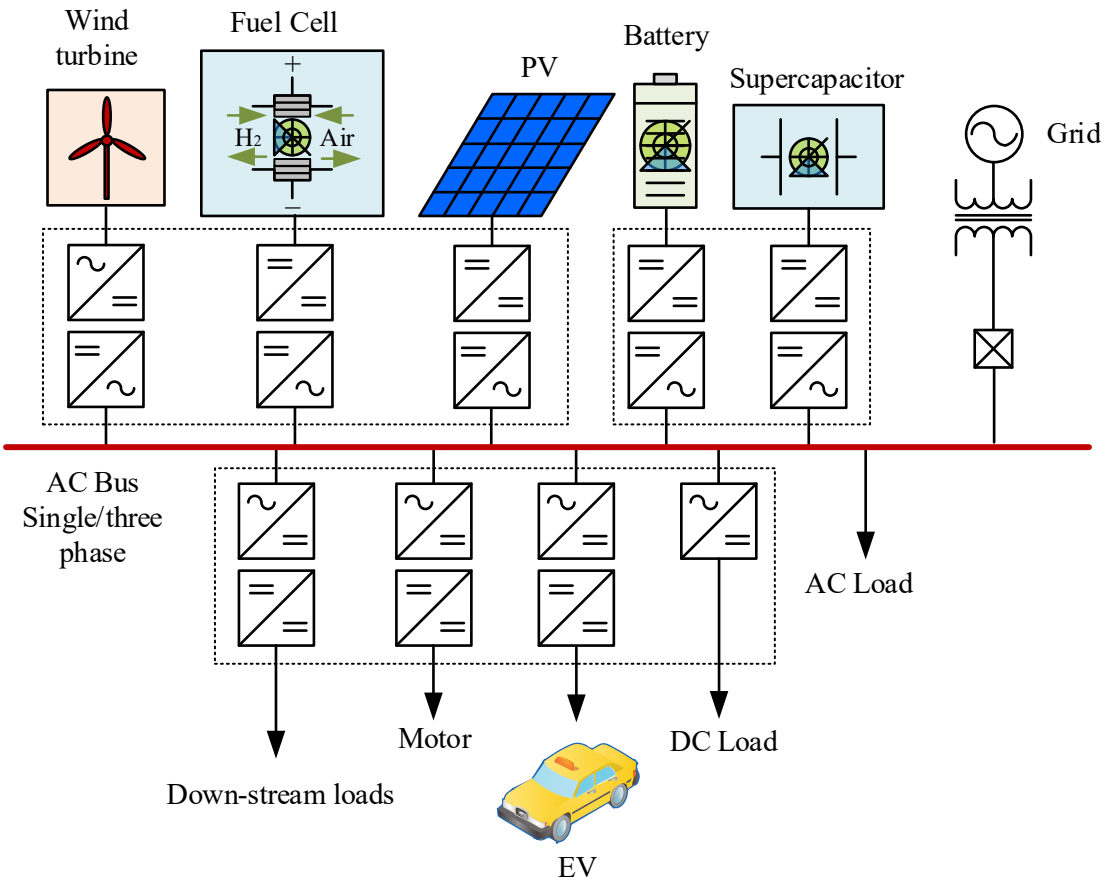


Figure 1.6 A typical AC microgrid configuration.

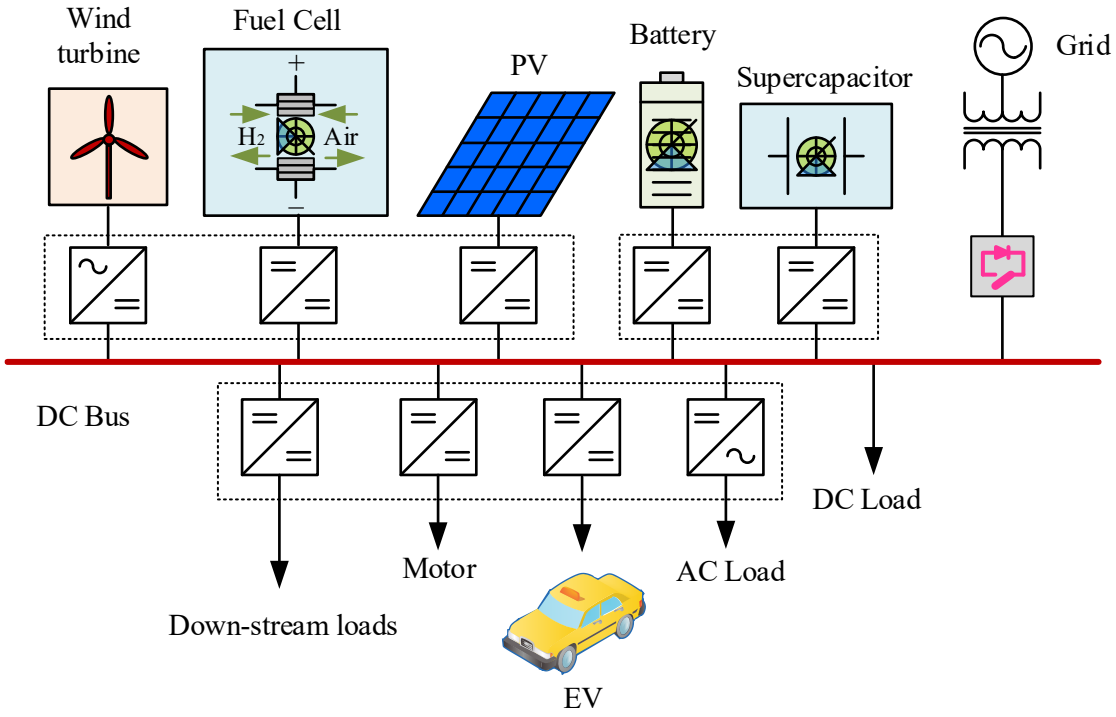


Figure 1.7 A typical DC microgrid configuration.

1.2.2 DC Microgrids— Applications and State of the Art

Much research has been carried out in DC microgrids [11]. In the USA, the concept of Future Renewable Electrical Energy Delivery and Management (FREEDM) [12][13][14] has been proposed for future smart power distribution. In this framework, DC microgrids are an important part.

Many DC microgrid demonstration sites have been developed, e.g. the DC building at Xiamen University, China [15], the intelligent DC microgrid living lab in Denmark [16], Nushima island DC microgrid in Japan [17], the DC microgrid library conducted by Bath University in UK [18], and Burlington DC Microgrid in Canada [19]. Reference [11] provides further examples of DC microgrids. These applications of DC microgrids mainly focus on industrial buildings and remote island electrification. DC microgrids also have application on ships [20][21], aircraft [22] and in data centres [23].

DC microgrid research involves many topics, including control, stability analysis, protection, system structure and communication protocols. The research reported in this thesis focuses on the study of control strategies and stability issues.

DC microgrids commonly use a hierarchical control scheme. A typical hierarchical control scheme can be seen in chapter 2, section 2.1.2. The lower layers are responsible for the dynamic control of interface converters; the upper layers are responsible for the power management/trade with communication infrastructures. The control of DC microgrids tends to realise intelligent and automatic power distribution, which also corresponds to the future trend of smart grids. Configuring DC microgrids with communications infrastructure can make the power management easier, but complex control structures add to the installation costs of DC microgrids. This is difficult for remote area electrification, especially in developing countries, which is one of important applications of DC microgrids. Therefore, reducing the cost of DC microgrids is important for their wider application. One way to reduce the cost is to remove the upper layer communication infrastructure. As a substitute, low bandwidth communications or spare

communications are used for the power management. For cost-effective considerations, power line communications (PLC) are proposed for the communications between the interface converters. In this case, additional external communication links are no longer needed. The signal can be delivered through the power line. However, dedicated signal modulation and demodulation circuits are still required for conventional PLC methods. The advantages and disadvantages of PLC will be discussed in Chapter 2.

Another option is to remove the communication infrastructure and configure the DC microgrids with original droop control or DC bus signalling. The system will then become load adaptive. However, load adaptive methods lack consideration of the characteristics of distributed sources, e.g. battery banks, and depletion and overcharging will shorten battery life spans. Therefore, it is still worthwhile to investigate a method to actively regulate the distributed sources in the absence of communication infrastructures for low cost DC microgrid applications.

Stability is another essential requirement for DC microgrid operations. Stability issues in DC microgrids are about maintaining the bus voltage stable and avoiding black-out. They will be specifically discussed in chapter 2. One potential cause of instability is the interaction of cascaded converters. A load converter (or point of load converter) acts as a constant power load and will introduce negative incremental resistance. It can interact with the former converters or filters to form a negative oscillator. Two methods of stability analysis are small signal linear analysis and large signal nonlinear analysis. Small signal linear methods are based on Middlebrook's minor loop gain theorem and provide design guidance for cascaded converters. The idea of small signal analysis is to linearize a nonlinear system around its quiescent operating point. Large signal nonlinear analysis concerns an area of convergence that is also called domain/area of attraction. The system will always tend to be stable inside that domain. However, nonlinear analysis is complex and requires massive calculations. Besides, it is difficult to guide the conventional controller design and line up with the industrial applications. The author chooses the small signal linear method as the main analysis method throughout this thesis.

Apart from the instability caused by the point of load converters, the source side converters can also interact with each other. Introducing droop control will impact the quiescent operating point and have the potential to destabilise the system. In addition, interface converter described by non-minimum phase transfer functions have the potential to be unstable. Conventional methods to reduce the impact of non-minimum phase interface converters from a control perspective are mainly based on the parasitic resistance of terminal output capacitor while the resistance introduces the voltage ripples. Therefore, it needs proper control methods to deal with the non-minimum phase and adjust the complex operation conditions in DC microgrids.

1.3 Objectives and Structure of Thesis

Motivated by the requirement of cost-effective low voltage DC microgrids, this thesis proposes a novel hierarchical control scheme for the operation of a DC microgrid, and provides solutions to the following problems in a DC microgrid system:

- Coordination of distributed sources in a DC microgrid without additional communication infrastructure;
- Mitigation of the impact of non-minimum phase converter transfer functions to ensure the stable and reliable operation of the system;
- Investigation of interactions between interface converters in DC microgrids and provide stable operation suggestions.
- Solve the power imbalance that could occur in the islanded mode when PV generations supply surplus power.

Each chapter includes a brief introduction and a summary. The structure of this thesis is organised as follows,

In Chapter 2, control strategies/methods and stability assessments of DC microgrids are reviewed. Control methods are reviewed under a hierarchical control scheme, in which the details of droop control, DC bus signalling (DBS) and power line communication (PLC) are analysed.

Other control strategies on top layer control for power management are reviewed as well, such as multi-agent control. As for the stability evaluations, the linear analysis will be the main composition of this thesis for the consideration of controller design and modification. The instability factors are discussed from the source to load interactions and source to source interactions under a single DC bus microgrid. The criteria used for evaluating the system stability are reviewed. Finally, previous stabilization methods in DC microgrids are reviewed and classified.

In Chapter 3, the design of a DC microgrid experimental system is described. This system contains four interface converters. Bidirectional boost converters are used as interface converters. Details of each interface converter are provided.

In Chapter 4, a dual-window DC bus interaction (DBI) method for low-bandwidth communication is proposed. The mechanism and principle of this method are explained. Signal series design procedures based on the mechanism of the proposed method are provided and possible drawbacks are discussed. Finally, the feasibility of the proposed method is validated experimentally in a simple case study.

In Chapter 5, a passive stabiliser for compensating non-minimum phase interface converters is proposed. The non-minimum phase makes the outer loop voltage transfer function in the Nyquist plot have the potential to encircle (-1, j0), which results in instability. The passive theory related to this work is briefly introduced. The detailed analysis and design process of passive stabiliser are provided. Finally, the effectiveness of proposed passive stabiliser is experimentally validated.

In Chapter 6, the proposed dual-window DC bus interacting method in Chapter 4 and passive stabiliser in Chapter 5 are constructed under a hierarchical control scheme for household DC microgrid applications. The stability and interactions of each interface converters are evaluated from terminal admittance based on the minor loop gain analysis. The signal series protocol is designed based on assumed rules. The system state machine is illustrated. Finally, the on-grid/off-grid situations and seamless transfer between them are experimentally validated. Besides, for a

special case in off-grid mode, the surplus power from PV generations are limited based on a modified maximum power point tracking (MPPT) algorithm.

In Chapter 7, conclusions are made, and future work is suggested. The contributions of this thesis to the literature are summarised and author's publications are listed.

An appendix provides PCB design of interface converter and equations' calculations and manipulations involved in Chapter 5 and 6.

Chapter 2 Literature Review

Control strategies and stability issues are the two main topics throughout this thesis. In this chapter, previous studies related to control methods/strategies and stability in DC microgrids are reviewed. The control strategies/methods are reviewed based on their functions and roles in a hierarchical control scheme. This chapter focuses on the review of bottom layer control methods, such as droop control, adaptive droop control, and DC bus signalling, etc. The advantages and disadvantages of each control method will be explored. The DC microgrid stability issues are introduced from three aspects. The first is the instability factors in DC microgrids, such as constant power load. The second is the small signal linear stability criteria for cascaded converters in DC microgrids. Their originality, development and variations are reviewed and illustrated. The third is stabilising methods for DC microgrids. Those methods are reviewed, compared and classified. At the end of this chapter, identified problems in this literature review are summarised.

2.1 Control Strategies in DC Microgrids

Control methods are essential for the operation of a DC microgrid. There are many reported DC microgrid control concepts, such as hierarchical control, supervisory control, centralised control, distributed control, etc. Some of them have the same objectives but are used in different applications; some of them are used in subordination relationships. Before reviewing the specified control methods, it is necessary to explain these control concepts first.

2.1.1 Control Concepts in DC Microgrids

Three concepts are discussed in many papers: centralised control, decentralised control and distributed control. These concepts come from communication networks [24]. Therefore, when they are applied to DC microgrids, the DC microgrid communication infrastructures need to be considered. The control concepts are illustrated as follows.

- *Centralised control*

Centralised control is based on a central controller (CC), which is sketched in Figure 2.1(a). It is easy to implement this control network. However, this network is vulnerable in that the failure of the CC will lead to the collapse of the whole system. It is also called single point of failure.

- *Decentralised control*

Decentralised control avoids the single point of failure problem of centralised control. It can be regarded as the expansion of centralised control, as shown in Figure 2.1(b). However, the destruction of the regional controller (RC) will lead to regional collapse.

- *Distributed control*

Distributed control is a relatively reliable network. Every single point is connected to its neighbours. Single point of failure will not impact the rest of the individuals in the system as is shown in Figure 2.1 (c). Therefore, for any complex network with the goal of high reliability, it is advantageous to make the system more ‘distributed’.

In DC microgrids, some control methods are non-communication based. For example, conventional droop control does not need any additional communication links if the distributed energy sources work under droop coefficient-based power sharing states, yet they are individually reliable. This means that the system can still work well regardless of any single module failure. Therefore, the conventional droop control is a ‘distributed’ control method.

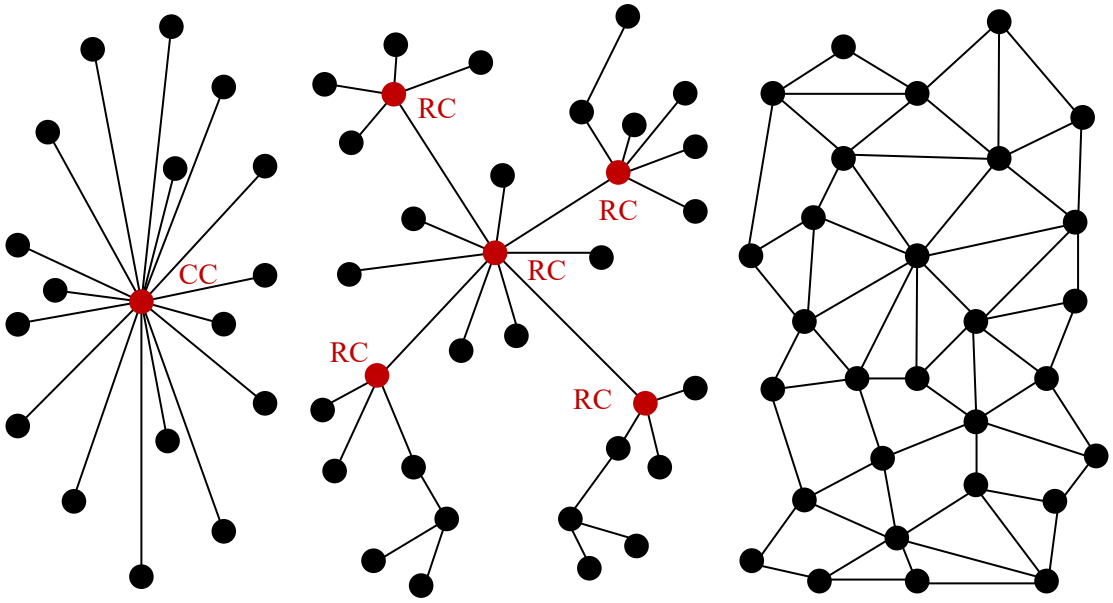


Figure 2.1 Diagram [24] of centralised (a), decentralised (b) and distributed (c) control networks.

2.1.2 Hierarchical Control Scheme

Hierarchical control scheme[1] has been widely applied in microgrids. Paper [8] adjusts the ISA-95 standard [25], which is for enterprise-control systems integration, to microgrids as four control levels or layers, which are shown in Figure 2.2. It has:

- converter control, such as voltage control, current control and double loop control, etc.;
- primary droop control;
- secondary DC bus restorations;
- tertiary power flow or power management control.

Secondary and tertiary control layers need to use low bandwidth communication or sparse communication links.

[1] Control scheme here refers to the control configurations that the DC microgrid system is based on. For example, hierarchical control scheme is the most widely applied control scheme in both AC and DC microgrids, and has different control layers.

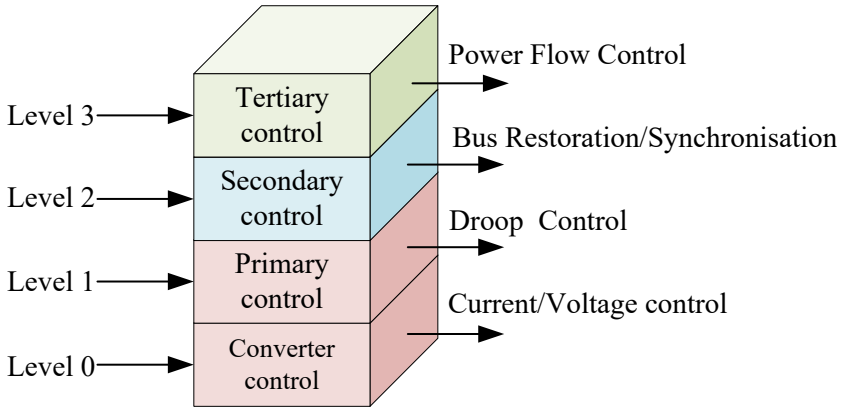


Figure 2.2 Hierarchical control scheme of interface converters in DC microgrids.

The hierarchical control scheme has different types of configuration. For example, a hierarchical control with upper layer cyber networks for microgrid clusters is proposed in paper [26]. Adding advanced communication infrastructure (cyber networks) to the microgrid can make the system operate more intelligently than the conventional distributed system.

The DC microgrid system with hierarchical control scheme can be regarded as either distributed control or centralised control, which is dependent on the configurations of communication infrastructures. The upper layer[1] communications can update the parameters for the bottom layers according to user demands, such as economy, environment, etc. Among the upper control layers, many control strategies have been proposed, such as master-slave control (MSC), supervisory control (SVC), and multi-agent control (MAC) for power sharing and energy management.

Master-slave control (MSC) [27][28][29] is used for power sharing between parallel connected converters. The master module provides the current reference for the rest of the slave modules. It has advantages over small-scale distributed power systems (DPS) based on its convenience, cost-effectiveness and easy implementation. However, this method suffers from the problem of single point of failure just as the centralised networks. A method [28] has been proposed to avoid single point of failure. An additional diode array is added to controller for selecting a master module whose output current modules is maximum, which is shown in Figure

[1] The upper layer control refers to controls that do not interfere with converter dynamics; the bottom layer control refers to the dynamic control of interface converters.

2.3. The maximum current will eliminate the corresponding current reference loop; then the inner loop controller will start the voltage regulation. Therefore, even if the master module collapses, the next maximum output current module will automatically work as the master module. This makes the system more 'distributed' than the conventional MSC.

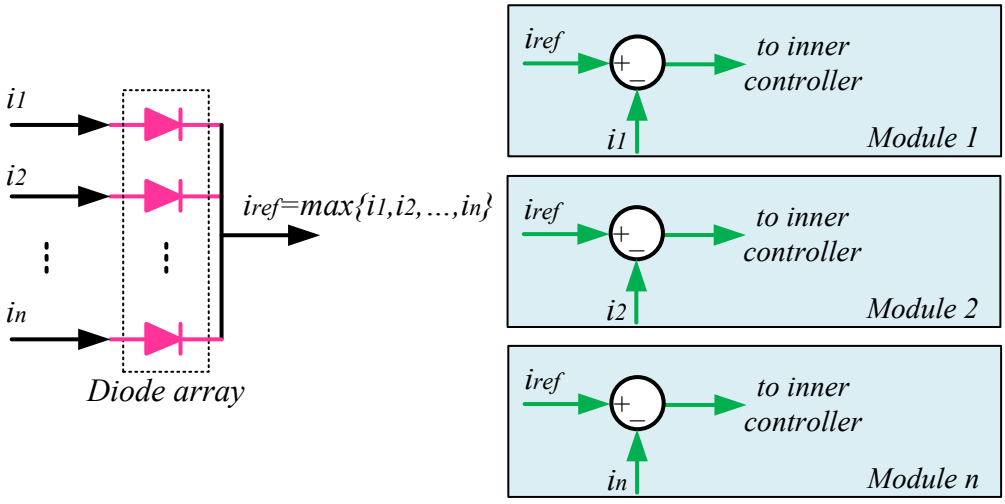


Figure 2.3 Modified MSC with diode array.

The later development of MSC in DC microgrids comes from an idea in conventional MSC. The master is responsible for maintaining the DC bus voltage, and the slave modules are responsible for the power sharing [30]. Since it must have an interface converter to work as a voltage source to maintain the DC bus voltage, it is usually assigned to the grid connected converter. The master module is operated as the voltage source, and the slave modules are operated as current sources, as shown in Figure 2.4. This control scheme leads to accurate power sharing compared with droop control, which will be further discussed in the next section.

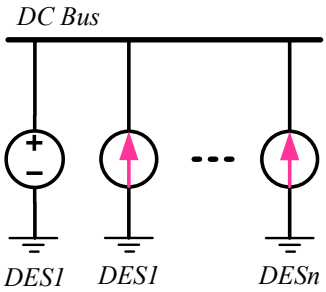


Figure 2.4 Master-slave control for distributed power systems.

Supervisory control (SVC) [31] is applied in the upper layer control of a microgrid system where the system parameter information will be processed and data exchange will be carried out. It provides the optimisation control supervisions to the lower control layers. A mixed concept of supervisory control and multi-agent control methods is proposed in paper [32]. Multi-agent control (MAC) [33] uses peer to peer (P2P) control for the power management of microgrids. The communication links lie between each neighbourhood; therefore, the system is configured in a 'distributed' way. The MAC control [34][35][36][37] uses sparse communication links/networks to regulate the energy storage system in microgrids, which makes the system networks reliable.

The upper layer controls mainly target the energy management in DC microgrids. Their optimisation objectives are based on external factors, while the most important part involving the power electronics control and system performance is made up of the bottom layer controls, such as voltage/current control, droop control and DC bus voltage regulations, etc. Applying communication infrastructure to DC microgrids adds to cost and complexity. Therefore, many methods are proposed for the power management of DC microgrids without additional communication infrastructures, such as DC bus signalling and power line communications.

The next three sections will review the control methods applied in DC microgrids without additional communication infrastructure. Their working mechanism will be introduced, and their applications and roles in a hierarchical control scheme will be set forth.

2.1.3 Droop Control and Variations

Droop control, also known as adaptive voltage positioning [38][39], is one of the most popular control methods applied in microgrids. Unlike the AC system[40], there is no frequency in the DC system. The voltage droop in DC microgrids is introduced by output current multiplying virtual resistances (or output power multiplying droop terms). As for an ideal tightly regulated interface converter, the output impedance tends to be zero. This means that when there are two distributed energy sources are connected in parallel (as is shown in Figure 2.5), there is a large

circulating current between them if a tiny terminal voltage difference exists. Therefore, virtual resistance is introduced to avoid this situation.

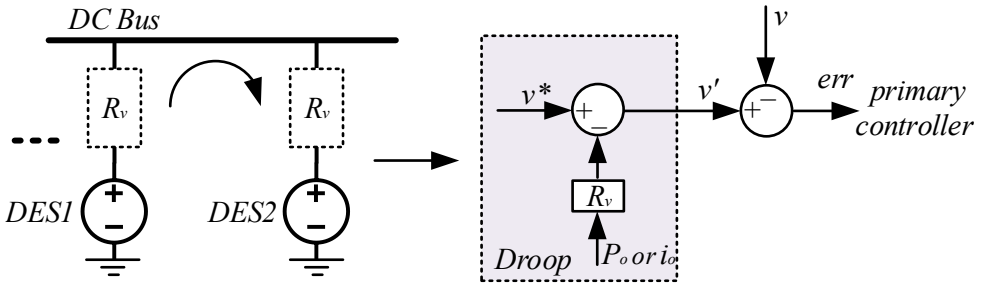


Figure 2.5 Equivalent circuit of two paralleled distributed energy sources.

A typical droop curve combination for two parallel-connected interface converters is shown in Figure 2.6, and they can be written as equation (2-1) and equation (2-2).

$$v_k' = v_k^* - i_{ok}R_k^{iv} \tag{2-1}$$

$$v_k' = v_k^* - P_{ok}R_k^{Pv} \tag{2-2}$$

where v_k^* is the nominal voltage; v_k' is the voltage reference for the controller; i_{ok} is the output current and P_{ok} is the output power; R_k^{iv} is the virtual resistance (or droop coefficient) for output current; R_k^{Pv} is the power droop factor and output power based droop control; k is the k-th converter connected in the system.

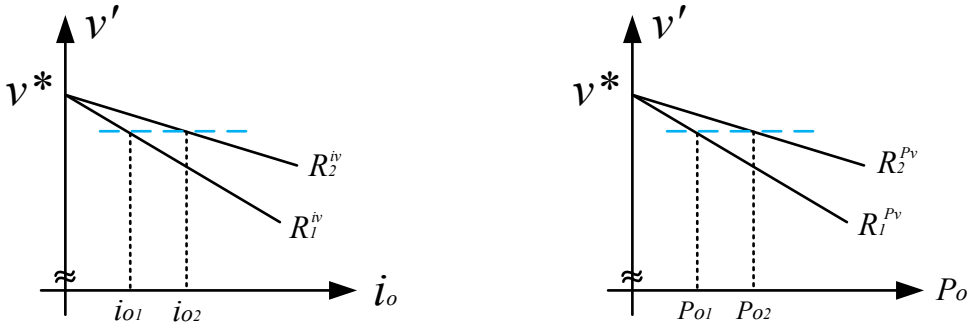


Figure 2.6 Droop curves in DC microgrids; (a) output current based droop control; (b) output power based droop control.

When multiple distributed energy sources are connected to the common DC bus, the power sharing between them thus can be adjusted by virtual resistances. In other words, the virtual

resistances are responsible for the power sharing between these distributed sources. Noticing the droop curves in Figure 2.6, these parameters can be varied by upper control layers with communication infrastructure, such as R_k^{iv} and v_k^*. Based on this idea, many adaptive droop control methods [41][42][43] are proposed to manage the power distributions in DC microgrids.

However, droop control has several drawbacks. First, the voltage droop introduced by droop control is not desired in some applications requiring constant bus voltage. Second, the values of the droop coefficient affect the accuracy of the power/current sharing. Ideally, the power sharing can be proportionally achieved using virtual resistance. However, for the applications with long power lines, the line resistance cannot be neglected, and this will degrade the accuracy of the power sharing.

Based on the above analysis, much research work has been done to overcome these drawbacks.

First of all, paper [44] uses a low bandwidth communication (LBC) to realise the DC bus voltage restoration by adding the additional values to the voltage reference, as shown in Figure 2.7. It also points out that a large droop coefficient can provide more accurate current sharing. However, a larger voltage droop will be introduced as a trade-off. Large voltage droop makes shift of quiescent operating point, and system stability might be affected. Related work using low bandwidth communication can be found in papers [45][46][47]. Paper [48] introduces the neighbour terminal voltage to the local controller to achieve DC bus restoration.

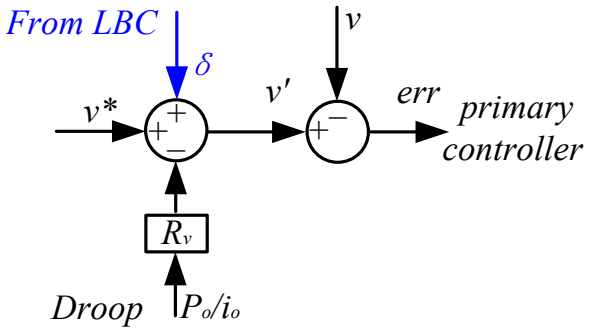


Figure 2.7 Bus restoration with low bandwidth communications.

Secondly, regarding the improvement of current/power sharing accuracy, paper [49] proposes a method to automatically adjust the droop coefficient according to the load such that when the

load is large, accurate current sharing can be achieved. Paper [50] addresses the circulating current sharing issues of two paralleled interface converters by introducing droop index control. Similarly, a droop index method based on the PV power was proposed in paper [51] to achieve accurate current sharing. Paper [52] introduces secondary control to remove the voltage droop and achieve accurate current sharing by voltage shift and slope adjustment.

Taking line resistance into consideration, paper [53] proposes a droop-based control strategy to achieve accurate current sharing for different working modes, such grid-connected mode and off-grid mode. In addition, papers [54][55] implement droop control under hierarchical control schemes in DC microgrids, in which the proportional current sharing was achieved through communications, and line impedance is no longer a problem. Apart from proportional current sharing, average current sharing is applied in [56]. In addition, some other methods [57] with nonlinear droop coefficients are proposed for meeting power regulation requirements. The fuzzy logic controllers are also applied to achieve accurate current/power sharing in papers [58][59][60].

To sum up, conventional droop control cannot actively optimise current sharing between distributed sources; it only provides a mechanism to achieve power sharing. Much research work has been conducted to modify the droop control method. For energy management, upper layer communication or signalling is required.

Droop control has advantages in regulating energy storage systems, such as battery banks or supercapacitors. The virtual resistance can be adjusted by the battery state of charge (SoC). Paper [61] proposes a double-quadrant SoC based droop control method to regulate battery power in the case of overuse. Similar SoC based droop control methods have also been proposed in papers [31][60][62] for coordinating multiple battery banks, multiple supercapacitors [63][64], and hybrid energy storage [65][66]. A frequency-based droop control for hybrid energy storage systems with function separation is proposed in paper [67], so that the energy storage system can dynamically respond to various situations.

After reviewing the above previous research work, it can be concluded that droop control is applied in the bottom layer control from a hierarchical control scheme perspective, which is directly related to converter dynamics.

2.1.4 DC Bus Signalling

DC bus signalling (DBS) [69][70] is a method that uses different DC bus voltage levels to achieve signalling between distributed sources. This method is developed from voltage level signalling [71]. Voltage level signalling (VLS) is a discontinuous form of voltage droop that allows sources to be scheduled in a certain working voltage window. VLS method is different from the purpose of voltage droop, which is to provide power sharing with minimal voltage deviations on the common DC bus. Large voltage deviations are allowed in VLS since the system is designed to operate within a specified voltage window.

The mechanism of VLS method is to utilise the inner current loop saturation to realise the voltage droop. When the system load increases, the distributed source will step into the current saturation mode, so the DC bus voltage decreases as the load increases until it reaches the next working voltage window to wake up another distributed source to supply the load. This mechanism is similar to MSC shown in Figure 2.4. DC bus voltage stays constant until the inner current loop reaches the saturation limit, which is shown as the solid line in Figure 2.8. However, VLS has its limitations. When new distributed sources are connected to the system, new working voltage windows need to be assigned for their operations. For a system with many distributed sources, the number of working voltage windows will be large.

VLS becomes DBS method by adding the droop loop to each working voltage window, which is shown as the dashed line in Figure 2.8. In this case, when new distributed sources are connected, they can work under the previous working voltage window by droop control with power sharing. Therefore, the power from the original distributed source can be shared with new distributed sources. Meanwhile, the number of working voltage windows can be reduced.

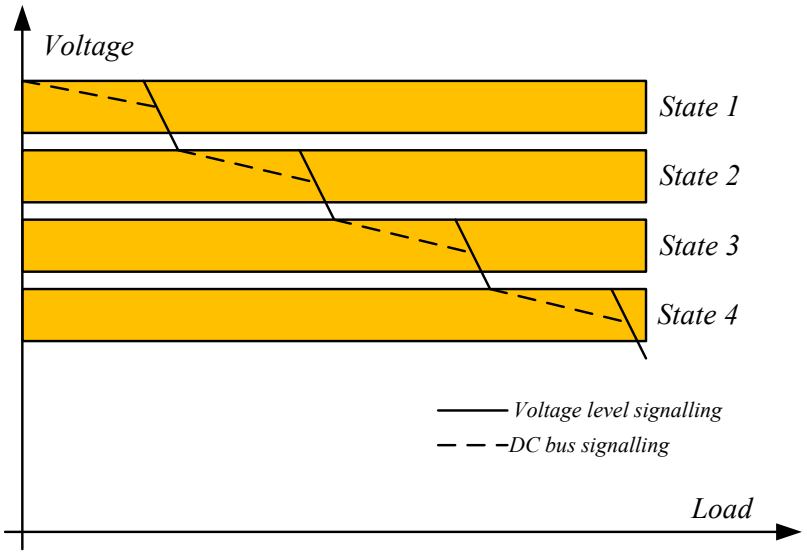


Figure 2.8 Diagram for voltage level signalling and DC bus signalling control methods.

Based on the working mechanisms illustrated above, the control block diagram of the DBS method is shown in Figure 2.9. The advantage of the DBS control method is that it can regulate the distributed source in the DC system automatically without external communication infrastructure. However, the signalling is load-dependent. In other words, the load's power consumption will determine the system's working state.

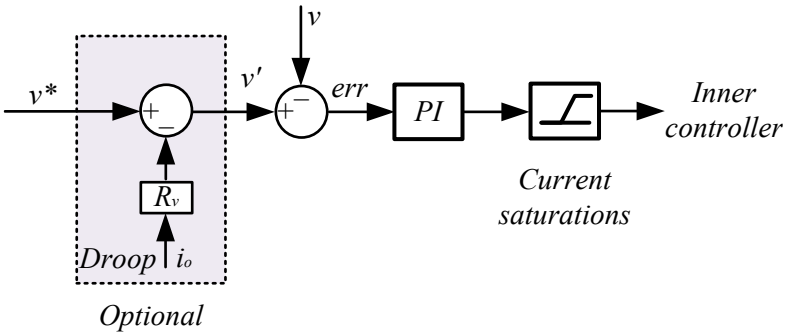


Figure 2.9 Control blocks for DBS method.

Based on the conventional VLS and DBS methods, many mode-adaptive DBS control methods [72][73][74][75][76] have been applied in DC microgrids. The mechanism of the mode-adaptive DBS control method is shown in Figure 2.10. Like conventional DBS methods, only one interface converter is used to operate as the voltage source to maintain the DC bus voltage. The working states of each distributed source vary between the voltage source and current source.

Apart from the mode-adaptive DBS methods, the conventional DBS method is also extended to other applications, such as solid state transformers [77] and SoC-based battery coordination [78]. In these cases, multiple-mode transitions are also involved.

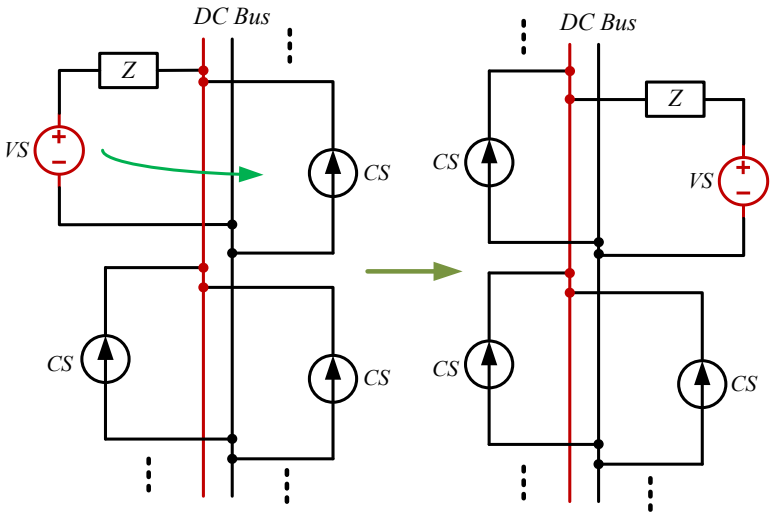


Figure 2.10 Mechanism of mode-adaptive DBS droop control methods.

DBS control method can be applied above droop control layers, which can also be seen from its working principles. Certainly, it is flexible to adjust this method with additional communication infrastructure on the upper control layers.

2.1.5 Power Line Signalling/Communication

Power line signalling/communication (PLS/PLC) is different from droop and DBS control methods. Literally, the communication signals are delivered through power lines. Power line communication does not participate in the dynamic control of interface converters; it is a method that replaces conventional communication infrastructure.

The mechanism of a typical PLC method [79] is to inject dedicated signals into the power line, where the signals carry the information that is used to change or modify the parameters in the lower control layers. This is shown in Figure 2.11.

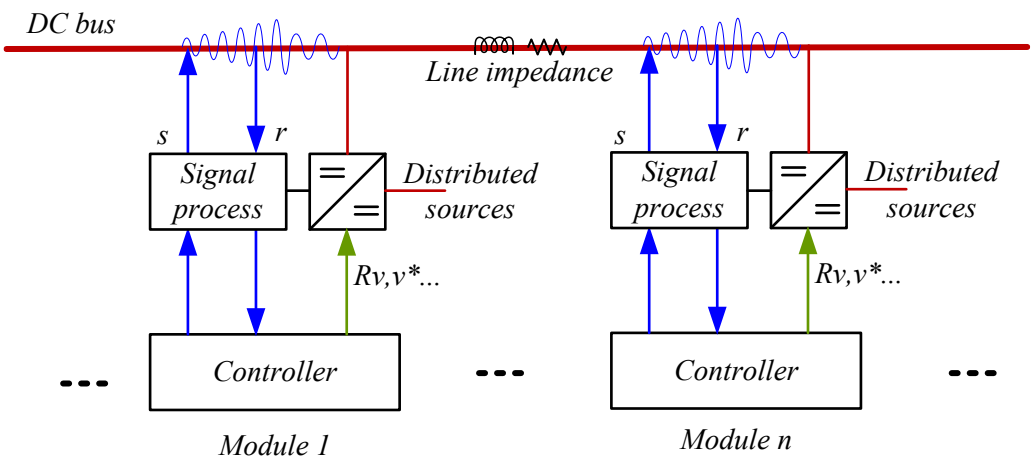


Figure 2.11 The mechanism of power line signalling/communication.

Compared with conventional communication methods, PLC does not need dedicated communication links. However, circuits to create and process signal are still required. The injected signals can affect the power quality of the DC bus, and the signals can be dramatically influenced by line impedance.

Apart from the conventional PLC methods, some modified PLC methods [80][81] are proposed, which utilise the inherent output voltage ripple of the interface converters as the signal carrier to achieve power line communication. The output voltage ripple frequency of interface converter can be varied by setting different switching frequencies. Several different modulation technologies are applied, such as frequency shift keying [82][83][84], power/signal dual modulation [85], Direct Sequence Spread Spectrum and phase shift keying [86]. Compared with the conventional PLC method, these methods do not need additional circuits to inject signals into the power line. Due to the inherent ripple contained in the interface converters, the effect on power line quality is avoided. However, the received signals still need to be processed by both hardware filter circuits and software signalling demodulation. The digital signal process, such as (sliding) discrete Fourier transformation (DFT), adds to the complexity of this method, such as on programming.

2.2 Stability Analysis in DC Microgrids

Stability is essential for DC microgrids, and stable operation is the premise of upper layer controls. In a DC microgrid with multiple converters, the dynamics of interface converters are no longer individually self-dependent. The interactions of these converters affect system performance and stability. As for a single DC bus topology, which is one of the most applied topologies in DC microgrids [87], the dynamics and interactions of the system can be divided into two parts, which are source to load (S2L) interactions and source to source (S2S) interactions,. Stability issues will be explored from these two perspectives.

2.2.1 Stability Analysis Methods

There are two main methods applied in stability analysis: small signal linear methods and large signal nonlinear methods. Linear methods are mainly based on small signal analysis [88]. Tools that can be used to evaluate system stability are eigenvalue [89], Nyquist plot, Routh-Hurwitz stability criterion, etc.

Large signal nonlinear methods are used to deal with the complex nonlinear problems in DC microgrids. The nonlinear tools are mainly based on Lyapunov related nonlinear techniques. Unlike small signal analysis, the system stability is unknown except near the quiescent operating point. The large signal nonlinear methods can estimate the attraction region of the stable operating point that is also named domain of attraction (DoA), which is depicted in Figure 2.12. If the operating point inside the DoA, the system always tends to be stable, otherwise the operating point outside the DoA tends to make the system divergent. When using the nonlinear method, a Lyapunov function needs to be ascertained. There are several ways to find this function. Brayton and Moser [90][91] propose a method to find the Lyapunov function for electrical systems that have capacitors and inductors. Based on this approach, paper [92] uses this Brayton-Moser-based mixed potential criterion to evaluate the performance of CPL. A method based on Takagi-Sugeno multi-modelling method [93] to determine/estimate the DoA is proposed in paper [94].

As a sub-stream of the nonlinear control theorem, passive theory is also applied in the large signal stabilisation of interface converters. Paper [95] proposes a passivity-based integral control for Boost converters. The creation of storage function in this paper is power related. Some other passivity-based nonlinear controls for interface converters can be found in [96][97]. In addition, passive theory has applications in the frequency domain, and facilitates the analysis of linear systems, which will be further discussed in section 2.2.3.

Further information on large signal nonlinear analysis can be found in the references [94] and [98].

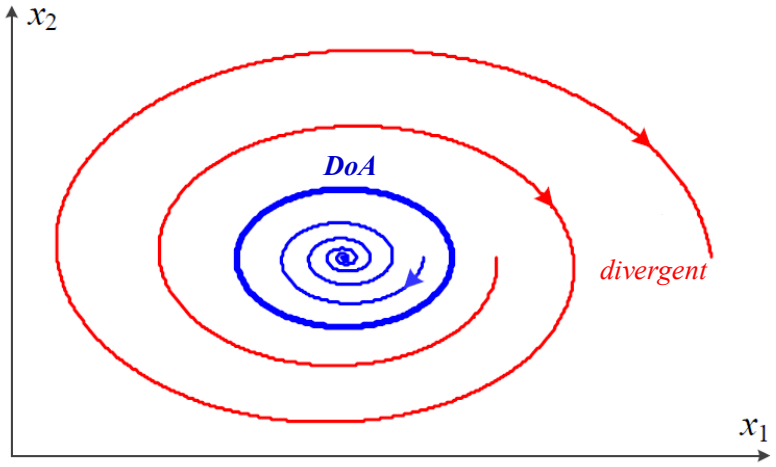


Figure 2.12 Domain of attraction for large signal nonlinear stability criteria.

Even though large signal nonlinear analysis has advantages over the uncertain complex system, and gives conservative stability boundaries, it is difficult to guide conventional controller stability designs. Conventional controller stability designs in industrial applications are mainly based on small signal linear models. Therefore, the linear methods and stability criteria will be specifically discussed.

2.2.2 Instability Factors in DC Microgrids

The interactions of interface converters in a DC microgrid are shown in Figure 2.13. The interactions in the system can be divided into source to load (S2L) and source to source (S2S) interactions.

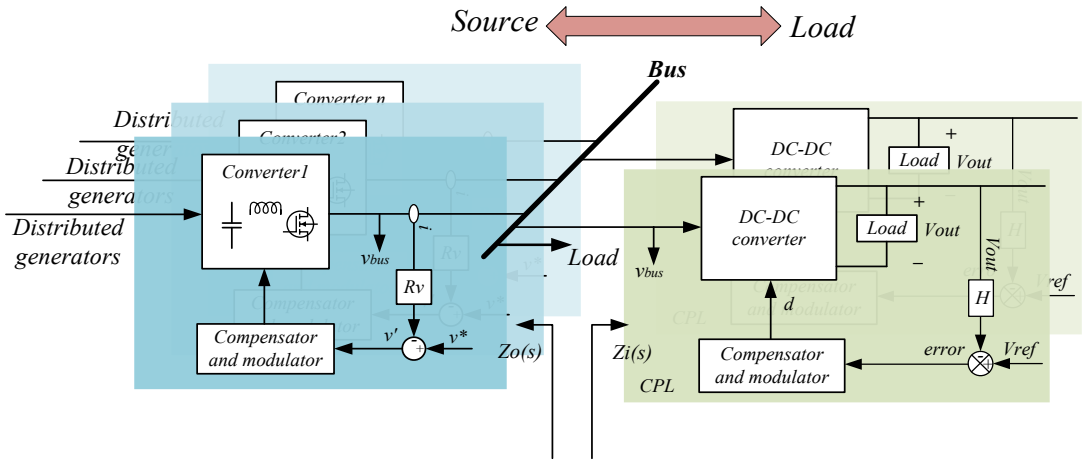


Figure 2.13 Discrimination of the sources and loads in a DC microgrid.

For the S2L interactions, constant power load (CPL) is one of the most widely studied unstable factors in DC microgrids because both the source and load are tightly regulated converters. The downstream converter, also known as point of load converter, reacts as negative incremental resistance (NIR) in dynamics. A diagram of NIR is depicted in Figure 2.14.

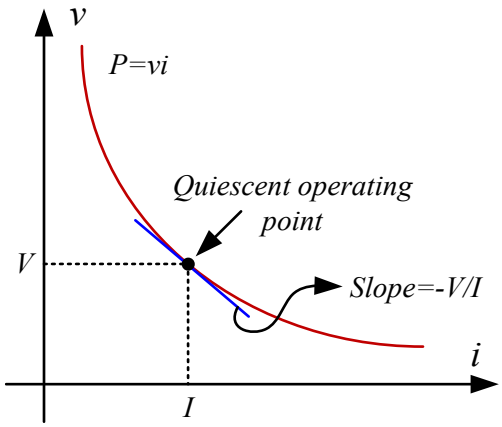


Figure 2.14 Diagram for showing negative incremental resistance caused by constant power load.

The power is constant for a CPL and can be written as equation (2-3).

$$P = vi = VI \tag{2-3}$$

where P is power. If small variations are superimposed on the DC bus voltage Δv and terminal output current Δi on equation (2-3), then equation (2-4) can be attained.

$$P = (V + \Delta v) \cdot (I + \Delta i) = VI + V\Delta i + \Delta vI + \Delta v\Delta i \tag{2-4}$$

By combing equation (2-3) with equation (2-4), and neglecting the second order ac terms, the dynamic terminal resistance can be calculated.

$$\frac{\Delta v}{\Delta i} = -\frac{V}{I} = -R \tag{2-5}$$

The imposed NIR interacts with the upper stream filters to form a negative resistance oscillator [99], so further threatening the stability of a cascaded system.

The other type of interaction is S2S interactions. S2S interactions can be analysed from the source and the paralleled power sharing sources. Regarding the source itself, the instability could be introduced by the non-minimum phase (NMP) in the interface converter transfer functions, such as Boost converter, Buck-Boost, fly-back converters, etc. The physics [100] of NMP is that the output value tends to go in the opposite direction of the intended value. As for the paralleled power sharing sources, the research about them mainly discusses the issues of stability performance after introducing droop control since the interface converters in DC microgrids are usually implemented with droop control. Stability evaluations regarding the impact of droop coefficients can be found in references [101][102][103][104].

2.2.3 Linear Stability Criteria

As mentioned in section 2.2.1, linear analysis of stability in a distributed system is mainly based on small signal analysis, which means linearizing a nonlinear system at a steady state operating point with small signal disturbance. Linear stability analysis in DC microgrids is mainly developed from Middlebrook's theory [105][106][107], which is initially for input filter design of tightly regulated power converters. The system is shown in Figure 2.15.

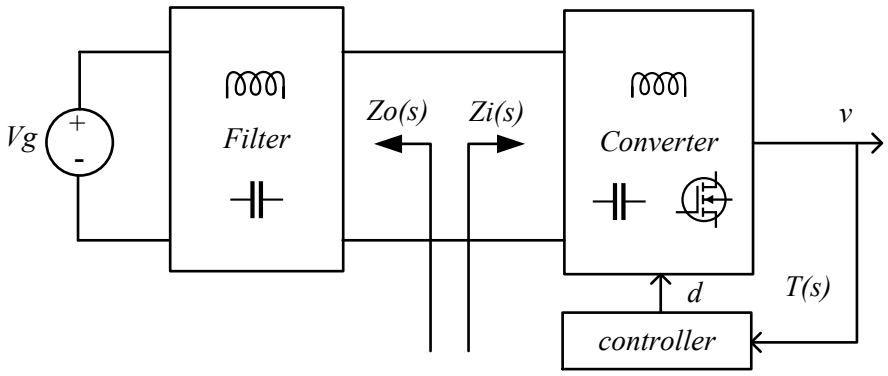


Figure 2.15 Impedance interaction with input filter.

With the introduction of an input filter, the plant transfer function is altered to equation (2-6).

$$G_{vd}(s) = \{G_{vd}(s)|_{Z_o(S)=0}\} \cdot \frac{1 + \frac{Z_o(s)}{Z_N(s)}}{1 + \frac{Z_o(s)}{Z_D(s)}} \tag{2-6}$$

where G_{vd} is the duty cycle to output voltage transfer function; $Z_o(s)$ is the output impedance of filter; $Z_N(s)$ is equal to the input impedance $Z_i(s)$ under the condition that the controller varies the duty cycle to maintain the output voltage variation as much close to zero as possible; $Z_D(s)$ is equal to the input impedance $Z_i(s)$ under the condition that duty cycle is equal to zero.

Considering the closed control loop gain $T(s)$, the converter input impedance $Z_i(s)$ can be expressed by the following equation (2-7).

$$\frac{1}{Z_i(s)} = \frac{1}{Z_N(s)} \frac{T(s)}{1 + T(s)} + \frac{1}{Z_D(s)} \frac{1}{1 + T(s)} \tag{2-7}$$

By applying the output impedance of filter $Z_o(s)$ on equation (2-7), then the impedance ratio T_{MLG} can be attained as equation (2-8).

$$T_{MLG} = \frac{Z_o(s)}{Z_i(s)} = \frac{Z_o(s)}{Z_N(s)} \frac{T(s)}{1 + T(s)} + \frac{Z_o(s)}{Z_D(s)} \frac{1}{1 + T(s)} \tag{2-8}$$

Therefore, if $Z_o(s)$ is designed to be much smaller than $Z_N(s)$ and $Z_D(s)$ (or $Z_o(s) \ll Z_N(s)$ & $Z_o(s) \ll Z_D(s)$), which is called impedance inequality, the previous system dynamics will not be affected by the introduced filter. Based on this idea, the input filter can be replaced by the interface converters, which is commonly seen in distributed DC systems or DC microgrids.

A cascaded interface converter system is shown in Figure 2.16. The two interface converters are designed to be individually stable.

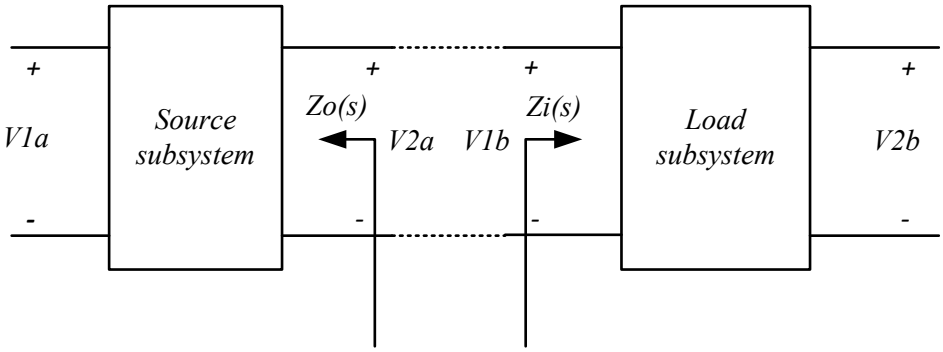


Figure 2.16 Interaction of a cascaded interface converter system.

$G_a = \frac{V_{2a}}{V_{1a}}$ is defined as the stable line transfer function of the source subsystem, and $G_b = \frac{V_{2b}}{V_{1b}}$ is defined as the stable line transfer function of the load subsystem. The interactions of the S2L converters can be analysed from equation (2-9).

$$G_{ab} = \frac{V_{2b}}{V_{1a}} = \frac{V_{1b}G_b}{\frac{V_{2a}}{G_a}} = \frac{G_aG_b}{\frac{V_{2a}}{V_{1b}}} = \frac{G_aG_b}{\frac{V_{2a}}{V_{2a}\frac{Z_i}{Z_o+Z_i}}} = \frac{G_aG_b}{1+\frac{Z_o}{Z_i}} = \frac{G_aG_b}{1+T_{MLG}} \quad (2\text{-}9)$$

where $T_{MLG} = \frac{Z_o}{Z_i}$ is the minor loop gain (MLG).

Due to the fact that G_a and G_b are stable, the system stability is then determined by T_{MLG}. If the Nyquist contour of T_{MLG} does not encircle the point (-1, j0), then the stability of the cascaded system can be guaranteed. In addition, the interactions of two interface converters are also reflected by the term $\frac{1}{1+T_{MLG}}$. If $T_{MLG} \ll 1$, which is equivalent to $Z_o(s) \ll Z_i(s)$, then the interactions of the cascaded system are small. In other words, the two subsystems are more 'individual'.

Based on the minor loop gain analysis, many stability criteria are proposed, which will be listed in the following discussion. The initial one is Middlebrook's stability criterion. Middlebrook proposes a forbidden circle that is contained in the unit circle, as shown in Figure 2.17 with a black solid line circle. The impedance ratio (T_{MLG}) must be limited in the forbidden

circle so that the Nyquist contour of T_{MLG} will never encircle the (-1, j0). This stability criterion gives good guidance to engineers from the design-oriented analysis (DOA). If the impedance of one side is known, then the other side's impedance can be determined easily to enable stable operations. However, it can be seen that this criterion is quite conservative because in some cases, the system can be stable when T_{MLG} traverses the forbidden circle. In order to limit the Nyquist contour of T_{MLG} within the forbidden circle, the terminal filters are always designed to be bulky, which is also not cost-effective.

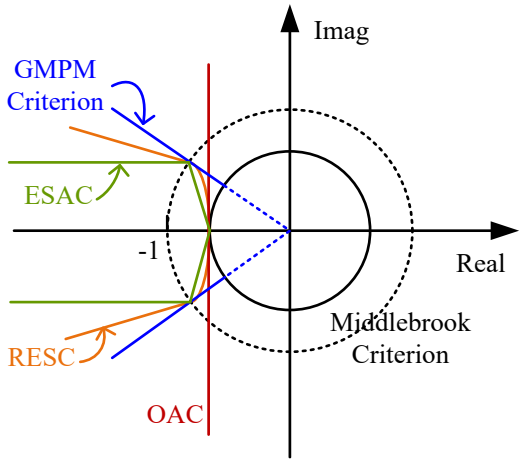


Figure 2.17 Various criteria for stability boundary.

Gain margin and phase margin criterion (GMPMC) [108] was proposed many years later after Middlebrook's criterion to extend the forbidden region. This criterion allows the Nyquist contour of T_{MLG} to lie outside the forbidden circle. In other words, it allows the impedance inequality to be negative over some frequencies while promising enough gain and phase margin. This criterion releases the forbidden region boundary, which also provides the path for later forbidden region extension; as a trade-off, both magnitude and phase information are required from the perspective of design-oriented analysis. Paper [109] tries to apply this criterion to multiple load subsystems. However, paper [110] proves that it could fail when individual load impedances are not proportional. The opposing argument criterion (OAC) [110][111][112] is then proposed to overcome this issue. This criterion shows only a vertical line intersecting the real axis with the gain margin far from (-1, j0) so the Nyquist contour of T_{MLG} will not encircle that point. Similarly,

this criterion also needs to know the magnitude and phase information of both source and load subsystems. Sudhoff *et al.* further extends the forbidden region and proposed the energy source analysis consortium (ESAC) [113][114] and the root exponential stability criterion (RESC) [115]. He points out that all the criteria are affected by the component grouping, which means that a stable system may violate the stability criterion with a different component grouping, and he states that the proposed EASC gains more immunity from the component grouping.

Table 2-1 Comparisons of minor loop gain based stability criteria.

Stability criterion	Conservativeness	Comments
Middlebrook	Very conservative	Initial stability criterion; effective tool from DOA
GMPMC	Less conservative	Extended stability criterion; not very effective on multiple load subsystems
OAC	Medium conservative	Overcomes the difficulty in GMPMC
ESAC	Less conservative	Smallest forbidden region
RESC	Less conservative	Developed from EASC; more robust from a numerical perspective

All these criteria and forbidden regions are summarized in Figure 2.17, and the comparisons and comments related to these criteria are listed in Table 2-1. Further reading of other researchers' comments on stability criteria can be found in paper [116].

In DC microgrids, the system usually involves more than two cascaded converter interactions. When a large number of converters are introduced in the system, how does this affect the system's terminal impedance? Some research [117][118] addresses this question.

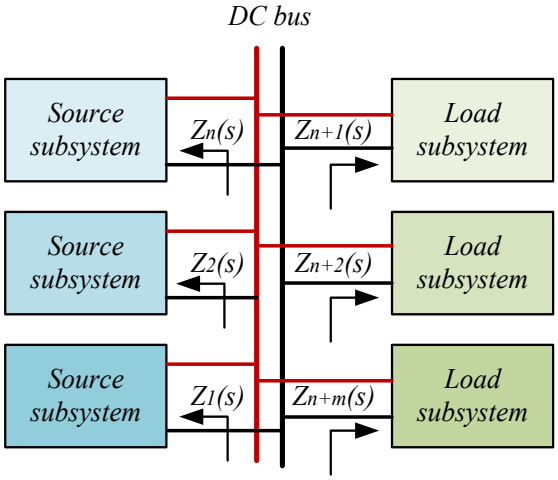


Figure 2.18 System impedance analysis.

It is found that the total terminal source impedance will become smaller if more parallel sources are connected, as is shown in equation (2-10),

$$Z_s = \left(\frac{1}{Z_1} + \frac{1}{Z_2} + \cdots + \frac{1}{Z_n}\right)^{-1} = \left(\sum_{i=1}^{n} \frac{1}{Z_i}\right)^{-1} \tag{2-10}$$

Similarly, the total load impedance is written in the equations (2-11).

$$Z_L = \left(\frac{1}{Z_{n+1}} + \frac{1}{Z_{n+2}} + \cdots + \frac{1}{Z_{n+m}}\right)^{-1} = \left(\sum_{j=1}^{m} \frac{1}{Z_{n+j}}\right)^{-1} \tag{2-11}$$

Therefore, an intuitive conclusion can be drawn based on the MLG criteria that more sources in the system can stabilise the system, and greater load in the system tends to make the system more unstable.

Apart from the minor loop gain-based stability analysis, passive theory [119] is also considered an effective method to analyse the stability issues of DC microgrids. As mentioned, passive theory has been used in nonlinear analysis. In this case, the sectionalisation of source impedance and load impedance is no longer needed. This is shown in Figure 2.19. The total DC bus impedance is then written in equation (2-12).

$$Z_{bus} = \left(\sum_{i=1}^{n} \frac{1}{Z_i} + \sum_{j=1}^{m} \frac{1}{Z_{n+j}} \right)^{-1} \tag{2-12}$$

This criterion [120] points out that if the total bus terminal impedance satisfies two conditions: (1) $Z_{bus}(s)$ has no right half plane (RHP) poles; and (2) $Re\{Z_{bus}(j\omega)\} \geq 0, \forall\omega$, then the terminal impedance is passive. From the above conditions, it can be seen that the passive impedance stability criterion is more conservative than the conventional MLG analysis. The impedance lies whole RHP in Nyquist plot, and the margins are also difficult to be given [118]. This method is further developed in [121]. In this paper, the total DC bus impedance is divided into individual terminal impedance for the passive evaluations. It can be easily proved that as long as the individual terminal impedance is passive, then the whole system terminal impedance is passively bounded, and the system is thus stable.

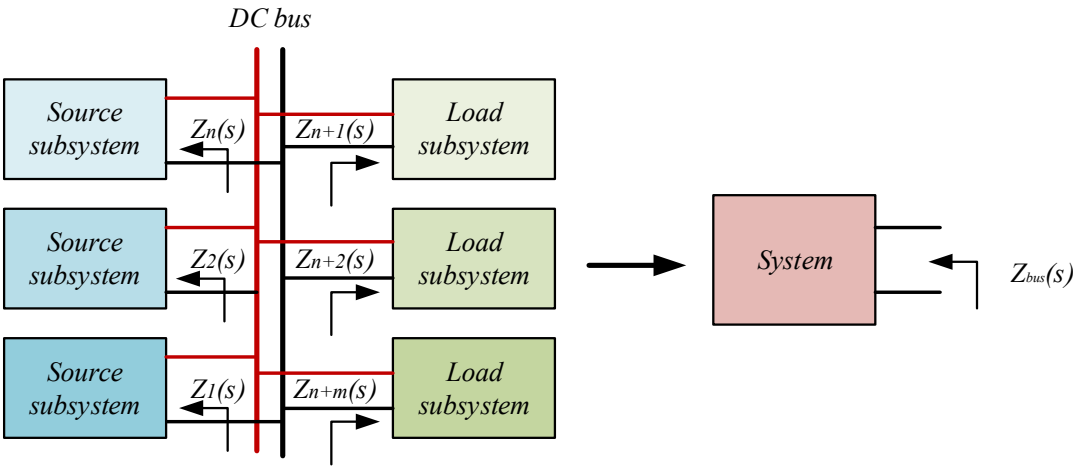


Figure 2.19 Total bus impedance analysis.

2.2.4 Stabilisation Methods in DC Microgrids

Based on the above stability criteria, many methods are proposed to stabilise DC microgrid systems with respect to impedance analysis. They can be broadly divided into two types.

The first type is to cope with CPLs, and it uses two methods: passive filter and active controller stabilisations. Passive filter stabilisation methods are mainly based on Middlebrooks' stability criterion and its extensions. Passive filter damping methods can be found in

[122][123][124][125][126]. The damped filters are designed to decouple the dynamics of two cascaded converters. However, the damped filters are normally designed to be bulky. This adds to the cost and reduces the flexibility of system installations.

The second method is active stabilisation. The terminal impedance is affected by the controllers; it thus can be shaped actively by altering or modifying the controllers. Current feedforward control to enhance the stability can be found in paper [127]. Input voltage feedforward active compensation methods can be found in paper [128]. In addition, active controllers based on the passivity for shaping the terminal impedance can be found in paper [118]. Other active controller designs can be found in [129]. Paper [130] uses many methods to mitigate the system oscillations such as damped filters, load shedding, additional energy storage, etc. Compared with damped filter design, active stabilisation methods avoid the additional passive components. However, it lacks universality for stabilising the system.

The second type is to cope with NMP converters and there are two general groups of techniques [131] to cope with NMP converters. The first one is the power stage related techniques. For example, operating a Boost converter at the discontinuous conduction mode does not exhibit the non-minimum phase [132]. Magnetic coupling [133][134] is used to eliminate the NMP, while this method modifies the converter topology and adds additional elements. The second group of techniques is the control related techniques. The parasitic resistance in the output capacitor [131][135][136][137] is used to adjust the position of positive zero on the transfer function, yet it also magnifies the voltage ripple. In terms of dealing with the NMP, it lacks the general methods to line up with double loop control.

Stability studies on droop control can be found in many papers. A frequency-dependent virtual impedance stabilisation method is proposed in [138][139]. A low pass filter-based virtual impedance is introduced, so high frequency oscillation can be avoided. On the other hand, stability analysis with droop control at lower frequency stability performance is analysed in paper [140]. Inspired by virtual resistance, introducing a virtual inductor for stabilising CPL in the DC system can be found in paper [141]. An output voltage feedforward active compensation method based

on passivity is proposed in paper [121]. However, the droop control loop is altered in this case and lacks universal representation. A comparative study on droop stability performance with different droop curves is conducted in paper [142].

Other methods such as DC electric spring [143][144][145] are also used for stabilising the system. This method was developed from the mechanical spring that is used for the mitigation of vibrations. Similarly, the "DC electric spring" can be used for damping the oscillations of a DC bus. It maintains the functions of the energy storage systems; meanwhile, the input side resistance can also adjust the input source variations.

2.3 Conclusions and Problem Statements

In this Chapter, the control strategies applied in DC microgrids are reviewed and compared. Droop control is one of the most widely applied control methods. However, it has drawbacks, such as voltage deviations and current sharing accuracy issues. From the perspective of a hierarchical control scheme, droop control lies outside the double loop controller and participates in the converter dynamics. The parameters of droop control, such as virtual resistance and floating voltage, can be modified by the upper layer's communication links for power management. DBS method can be used to regulate the distributed generations without additional communication infrastructure. However, this method is a load adaptive method, which means that the states of the distributed sources themselves are not considered. This means that the signalling processes are passive. As a substitute for communication links, PLC methods realise communication through the power line. Even though this method does not need conventional communication links, it still needs dedicated circuits to achieve the functions of signal modulations and demodulations. In addition, the signals over the power line can be affected by the power level of the system and line impedance. The signals also require complex analysis algorithms, such as (sliding) discrete Fourier transformation. It is still a challenge for cost-effective DC microgrids to be applied a proper control strategy without additional communication infrastructures.

Secondly, the stability issues in DC distributed systems or DC microgrids are reviewed and compared. A typical unstable factor in DC distributed systems is the negative impedance introduced by the constant power load. One efficient way to deal with the two stage interactions is to conduct impedance analysis. It can provide the design guideline for the stability design of a DC distributed system. This case has been widely studied. Regarding source side stability issues, however, the terminal impedance introduced by droop control is not clearly derived. In addition, the techniques dealing with the NMP still lack adjustability with respect to DC microgrid applications.

Chapter 3

Introduction of DC Microgrid Bench

This Chapter introduces a DC microgrid bench for experimental validation of the work presented in this dissertation. The hardware design of bidirectional boost converters for this bench is presented in detail.

Interface converters are the link between renewable energy sources, energy storage and a DC bus within a DC microgrid. Energy storage plays an important role in DC microgrids, especially in islanded operation. Bidirectional converters are therefore necessary for some of the distributed sources, such as battery banks for connection to the microgrid.

3.1 Low Voltage DC Microgrid Bench

The DC microgrid experimental bench used in this research is shown in Figure 3.1. and the configuration of this bench is shown in Figure 3.2. This DC microgrid bench comprises an interface converter setup, a PV emulator, battery banks, a DC power supply, an electronic load, a computer control panel and resistors. Among them, the PV emulator and the electronic load can be controlled and monitored by the laptop. Therefore, various PV generation and load conditions can be emulated.

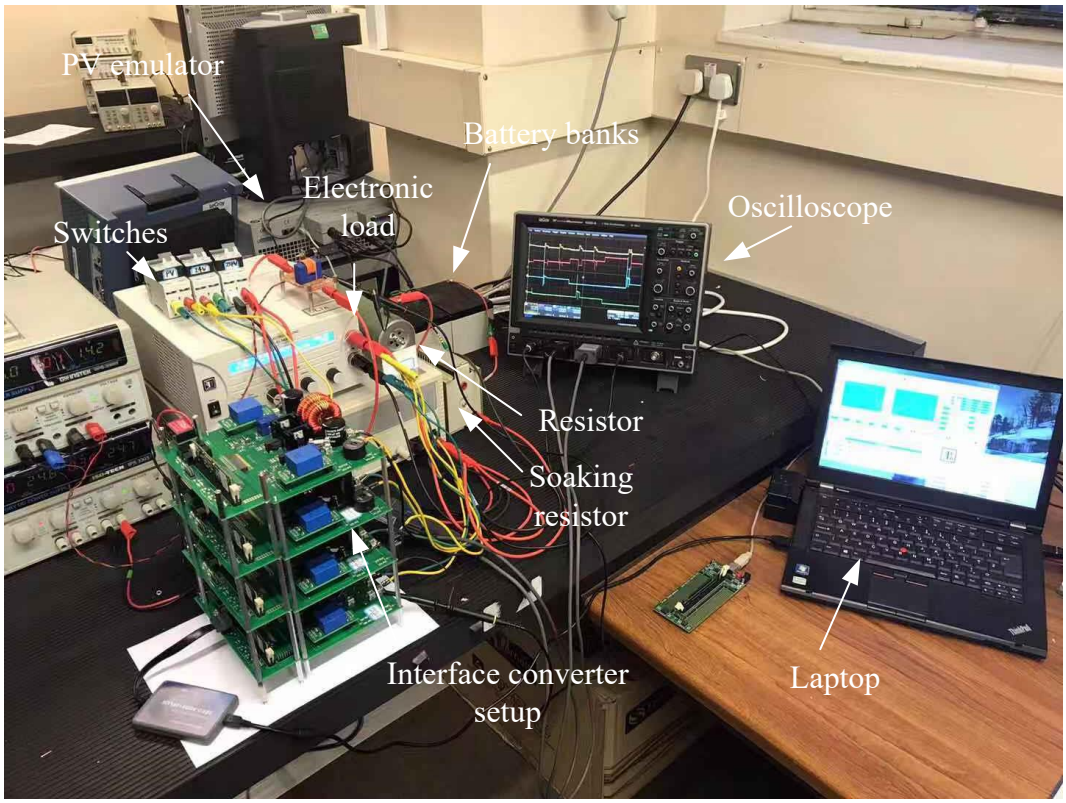


Figure 3.1 An overview of DC microgrid bench.

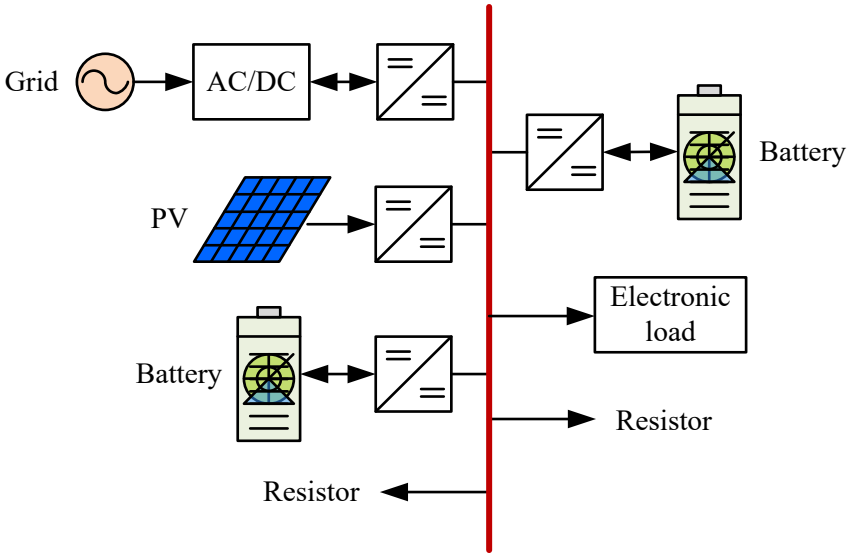


Figure 3.2 Configuration of DC microgrid bench.

Interface converters are the bridge that links distributed sources and the common DC bus. In this research, a bidirectional boost converter is designed for this low voltage DC microgrid bench.

The connection details of each distributed source will be introduced in section 3.3.

3.2 Design of interface converters

The interface converter contains two parts: power board and control board. The control and power boards are galvanically isolated. A block diagram of the interface converter is shown in Figure 3.3.

Based on the configuration in Figure 3.3, the front view of the interface converter is shown in Figure 3.4(a), and the whole setup of interface converters is shown in Figure 3.4(b).

In Figure 3.4(a), the functions of each area are listed in Table 3-1.

Table 3-1 Specification of interface converter.

Area	Function	Area	Function
①	Main power circuit	④	MOSFET driver circuit
②	Voltage and current transducer	⑤	Auxiliary power module
③	Analog signal process circuit	⑥	Micro-controller card

The detailed schematic and PCB layout of the interface converter can be found in Appendix A1.

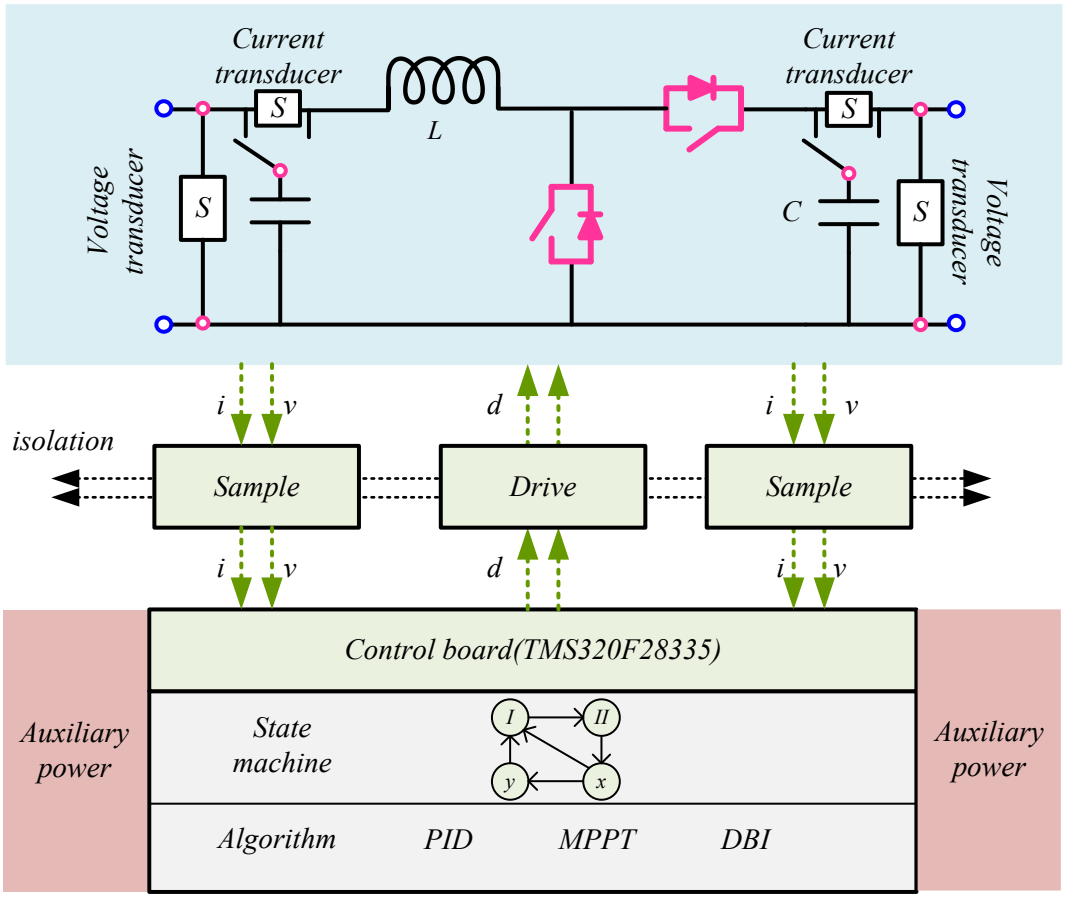
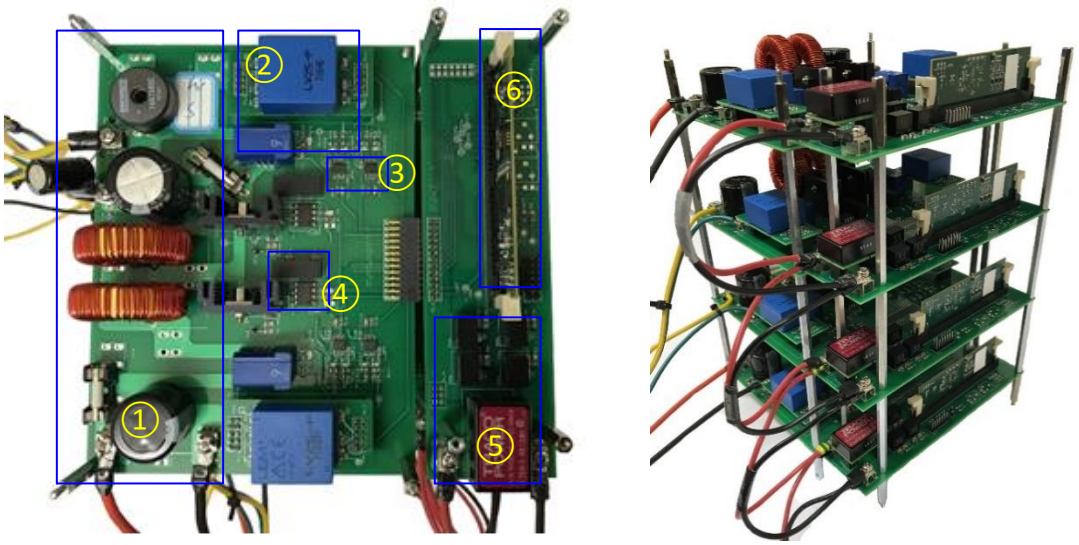


Figure 3.3 Block diagram of the interface converter.



(a) (b)

Figure 3.4 Prototype of low voltage DC microgrids. (a) the front view of interface converters; (b) setup of interface converters for DC microgrids.

3.2.1 Power Board

The power board contains the main power circuit, MOSFET gate drivers, and current/voltage sampling circuits.

The main power circuit is shown in Figure 3.3. A bidirectional boost converter topology is used. It can be noticed that a switch is put between the capacitor and current transducer. The current transducer can sample the current either the current before the capacitor or after the capacitor. The purpose of this design is to make the power board compatible for future considerations of multiple DC microgrid connection. In this research, the input (left) current transducer is used to sample the inductor current. The output (right) current transducer is used to sample the load current.

Current and voltage signals are sampled by isolated transducers and processed by analog circuits. Their circuits are shown in Figure 3.5 and Figure 3.6. The sampled current and voltage signals will be processed by a differential amplifier and voltage follower. Finally, the signals will be sent to the micro-controller card.

MOSFET drivers are powered dedicatedly by isolated power modules. The MOSFET drive circuit is shown in Figure 3.7.

The values of all passive components are provided in the appendix A2.

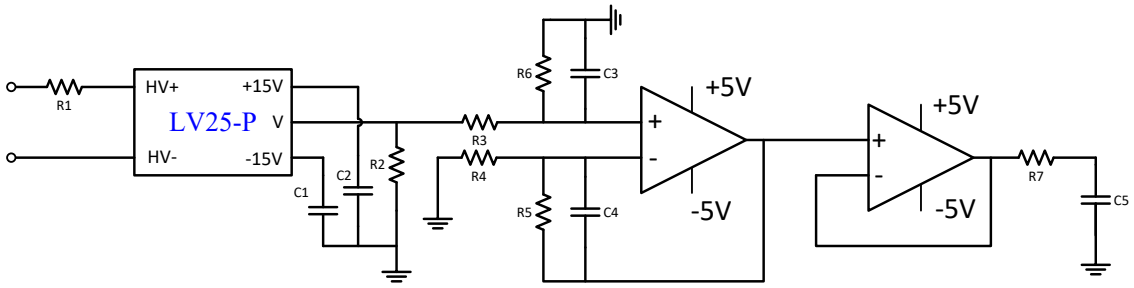


Figure 3.5 Voltage sampling circuit.

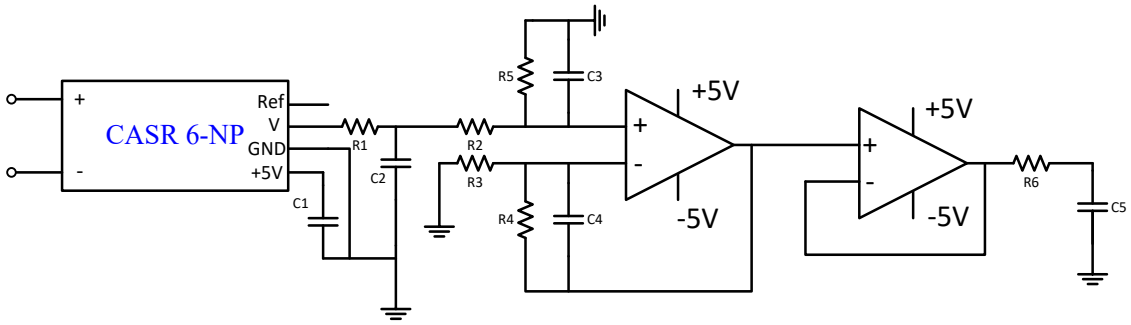


Figure 3.6 Current sampling circuit.

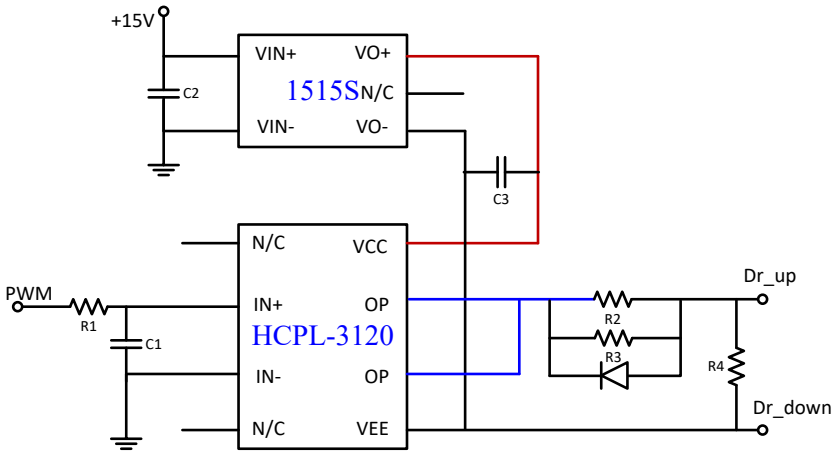


Figure 3.7 MOSFET drive circuit.

The components in the power board are listed in Table 3-2.

Table 3-2 Component list of power board.

Components	Types	Voltage required
Current transducer	CASR 6-NP	$+5V$
Voltage transducer	LV25-P	$\pm 15V$
MOSFET	FDP42AN15A0	N/A
PWM driver	HCPL-3120	$+15V$
PWM driver power supply	TMA 1515S	$+15V$
Amplifier	LM224	$\pm 5V$

3.2.2 Control Board

The control board contains auxiliary power supplies and a micro-controller (digital signal processor (DSP) TMS320F28335).

Auxiliary power is regulated by the TRACO power modules with 12V/5W output. Then it is converted to $\pm 15V$ and $\pm 5V$. They are created respectively by two identical power modules with back-to-back connections, which is shown in Figure 3.8. $\pm 15V$ are used to the supply the voltage transducer and MOSFET driver power module and drivers. $\pm 5V$ are used to supply the amplifiers, current transducer and micro-controller card.

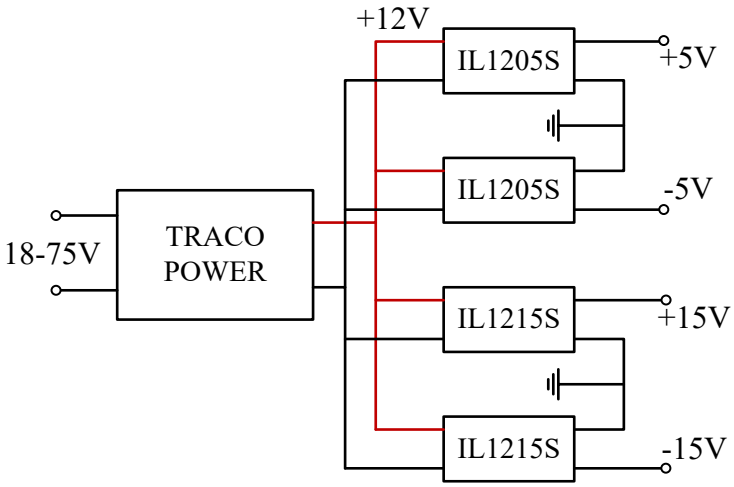


Figure 3.8 Auxiliary power circuit.

The components in the control board are listed in Table 3-3.

Table 3-3 Component list of control board.

Components	Type
Auxiliary power	TRACO POWER TEN 5-4812WI
	IL 1205S
	IL 1215S
Control card	TMS320F28335

3.3 Configurations of Distributed Sources

The experimental setup contains four interface converters. One is used as the grid connected converter, two are connected to rechargeable lead-acid battery banks, and another is connected to a PV panel.

The DC microgrid system is connected to an AC grid via a DC power supply. In order to simulate the grid connected cases, the connections in Figure 3.9 are applied. The DC power supply is used to connect the AC grid and provide power to the DC microgrid. The DC power supply cannot absorb power, so a soaking resistor *R* is parallel connected to the power supply to consume power. When the DC microgrid has surplus power to feed back to the grid, it can be consumed by the soaking resistor, or equally, the power from the DC power supply is reduced.

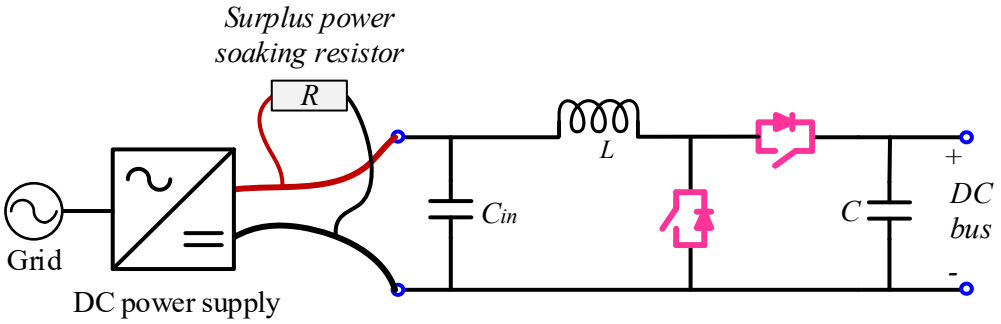


Figure 3.9 Emulated grid connections.

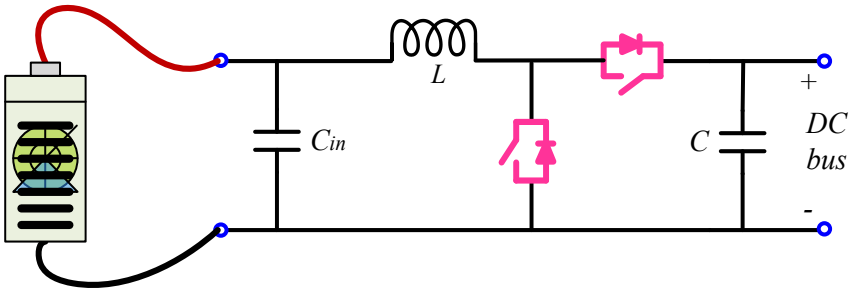


Figure 3.10 Battery connections

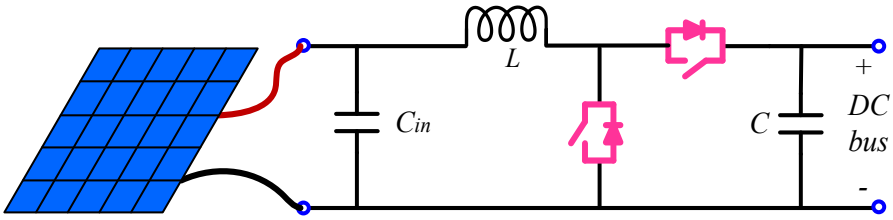


Figure 3.11 PV panel connections.

Two 12V lead-acid batteries are connected in series to form 24V, which is the input voltage of the interface converter. The connection of energy storage is shown in Figure 3.10. Using battery banks as energy storage is necessary for the operation of a DC microgrid, especially for the off-grid mode. It has two groups of battery banks in the experimental system. They are regulated respectively by the interface converter 2 and the interface converter 3.

The PV connection is shown in Figure 3.11. Different from previous two situations, PV only has single power flow. Therefore, it works as a Boost converter to inject the power into the DC microgrid.

The parameters and values of the simulated grid converter are listed in Table 3-4.

Table 3-4 Parameters for the converter connections.

DC power supply	Input: 110~240VAC, 50/60Hz Output: 0~60VDC Power rating: 1.2kW
Battery banks	Rechargeable lead-acid battery 12V, 24Ah; Number: 2
PV	PV output voltage: 0~40V Power rating: 150W
Decoupling (input) capacitor (C_{in})	$470\mu F$
DC converter inductor (L)	$240\mu H$
DC converter output capacitor (C)	$470\mu F$
Soaking resistor (R)	10Ω
Power rating the DC/DC converter	250W
DC converter topology	Bidirectional Boost converter

3.4 Conclusions

In this Chapter, a low voltage DC microgrid test bench for the experimental work of this research is introduced. The detailed design of interface converters is introduced. The configuration and connections of interface converters with different types distributed sources are illustrated.

Chapter 4 Dual-window DC Bus Interacting Method for DC Microgrids

Conventional droop control and DBS methods are load-adaptive methods. Droop control can be used to achieve plug and play performance. Multiple-mode DBS methods have the advantage of accurate power sharing, but they have limited ability in regulating a large number of distributed energy sources. Although PLC methods can achieve low bandwidth communications without additional communication links, they still need additional modulation and demodulation circuits. A novel information exchange method is thus proposed for cost-effective DC microgrids, which is called DC bus interacting (DBI) method. DBI method can realise low speed signalling to manage the power between distributed energy sources. It does not need any additional communication links and does not need the modulation and demodulation circuits required in PLC methods. DBI method utilises the following advantages: plug and play performance of droop control, power sharing of voltage source and current source mode, and voltage signalling in conventional DBS method.

In this Chapter, the mechanism and principle of the proposed DBI method for two-way signalling between distributed energy sources are presented. The design and implementation of the DBI method is illustrated. Finally, a simple case study is provided, and the experimental results demonstrate the feasibility of the proposed DBI method for DC microgrid controls.

4.1 Mechanism of DC Bus Interacting Method

The proposed DBI method [149] realises signalling by altering the working mode between voltage source and current source. It has two working periods: plug period and play period[1]. The mechanism of the DBI method is illustrated in Figure 4.1.

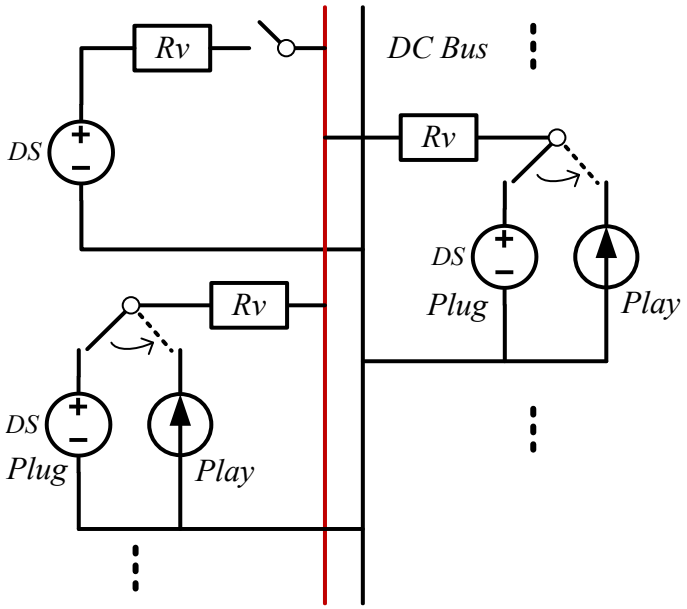


Figure 4.1 General mechanism of proposed DBI method.

- In the plug period, low speed signalling is required such that the plugged distributed source can be registered by the master module[2]. It must have at least an interface converter to maintain the DC bus voltage in DC microgrids, such as the grid-connected interface converter. The rest of the other distributed sources can either work under voltage sources with droop control or current sources. In this thesis, they work as current sources for the consideration of power sharing accuracy.
- In the play period, accurate power management can be achieved by making distributed sources work as current sources, such as SoC based charging/discharging for battery

[1] Plug period refers to the moment when a distributed source is plugged-in; play period refers to the state that a distributed source normally works in.

[2] The master module works as a voltage source to maintain the DC bus voltage; the slave module works as a current source to supply or absorb power from the DC microgrid.

banks and maximum power point tracking (MPPT) for PV generations. If the distributed sources need to send the signal again, they need to be switched to voltage source to interact with the master module to regulate the common DC bus voltage with designed signal series. The signal series here means that the DC bus voltage will be regulated to a dedicated signal form for signalling. This will be further discussed in section 4.4.

The distributed source works between the voltage source and the current source to interact with other sources through the common DC bus to achieve signalling. This is how the author names this method the DC bus interacting method.

4.2 Discussion of Droop Curves

During the plug period, the distributed source is working as a voltage source to regulate the DC bus voltage with signal series, as is shown in Figure 4.1. Conventional droop control cannot realise the signalling; some manipulation is required to achieve signalling on the conventional droop control.

In this research, it is assumed that there are only two distributed sources interacting each time in a DC microgrid. The equivalent circuit of this two-node system is shown in Figure 4.2.

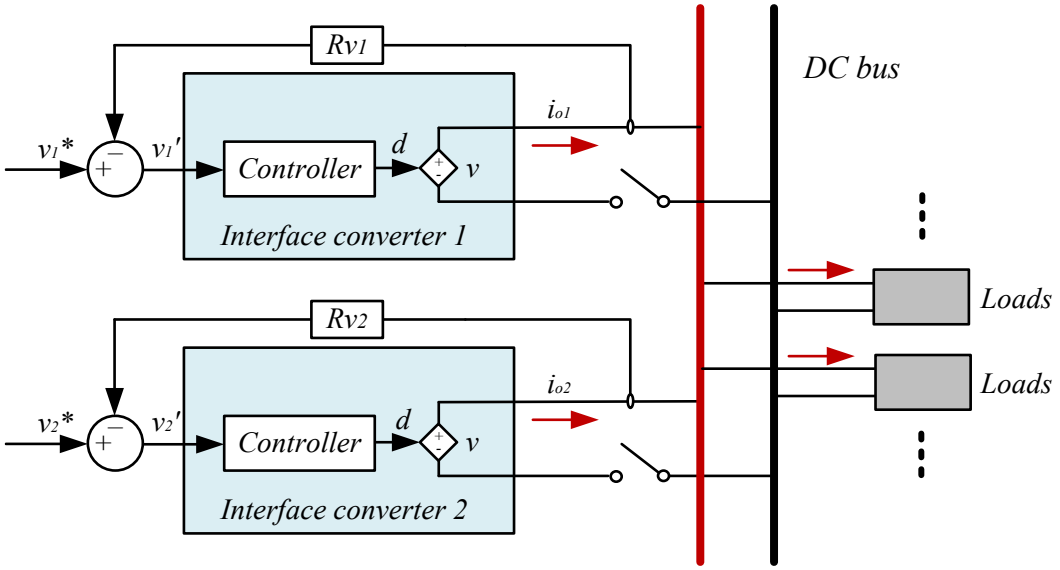


Figure 4.2 Two-node equivalent model of interface converters.

The two-node droop control equations can be attained in equation (4-1).

$$v_k' = v_k^* - i_{ok}R_{vk} \quad k \in \{1,2\} \tag{4-1}$$

where v_k' is the voltage reference for the control loop; v_k^* is the nominal voltage (or floating voltage); i_{ok} is the converter output current; R_{vk} is the virtual resistance (or droop coefficient); k is the k-th converter connected in the common DC bus.

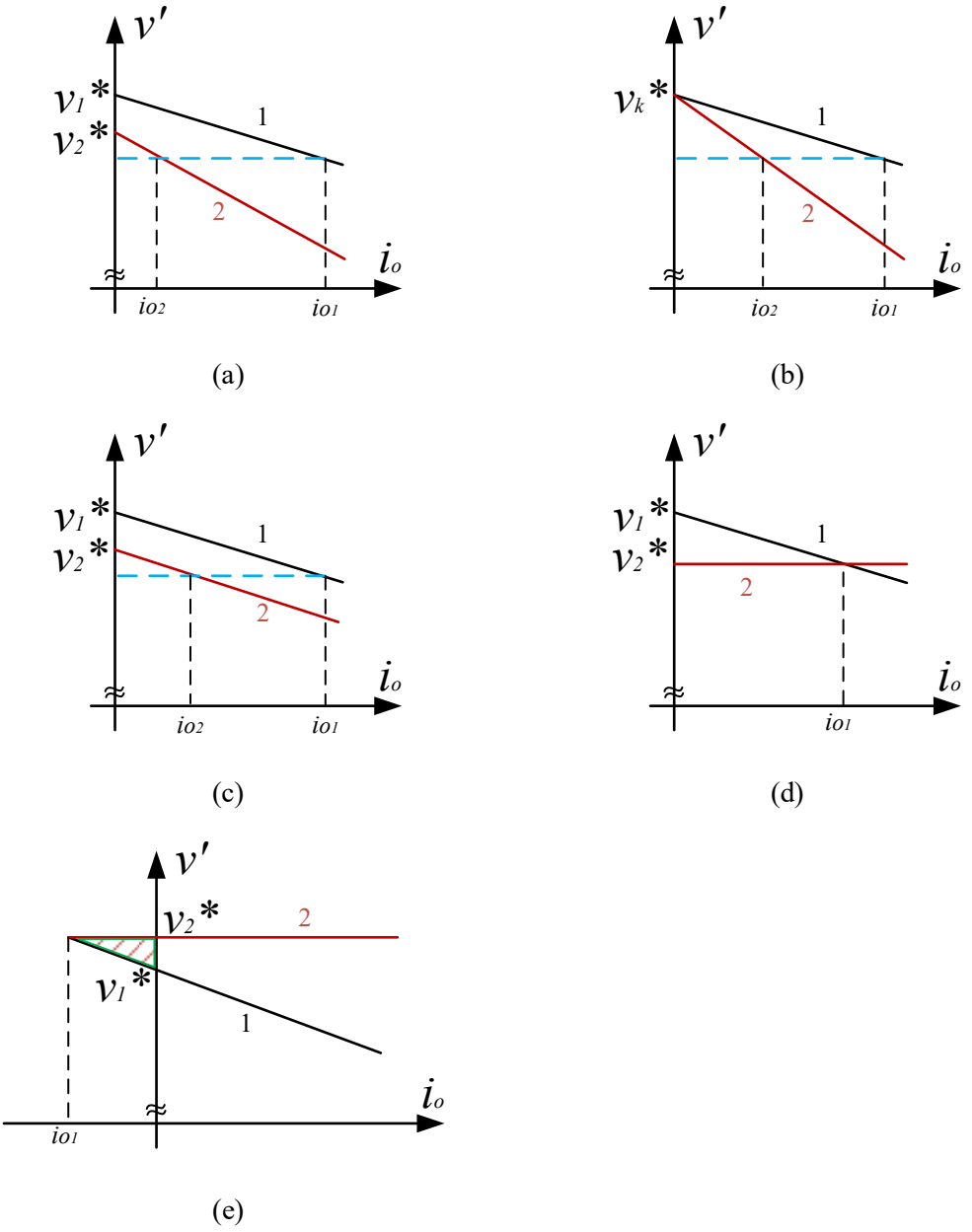


Figure 4.3 Various droop curve combinations. (a) droop curves with different floating voltages and droop coefficients; (b) droop curves with identical floating voltage but different droop coefficients; (c) droop curves with different floating voltages but identical droop coefficients; (d) droop curves with zero droop coefficient and point of intersection at right side; (e) droop curves with zero droop coefficient and point of intersection at left side.

By analysing all possible droop curves based on the above equations (4-1), the interactions of the two interface converters are shown in Figure 4.3.

Figure 4.3(a) shows droop curves having different floating voltages and droop coefficients. Their relationship can be shown in the following equation (4-2).

$$i_{o1} = \frac{v_1^* - v_2^*}{R_{v1}} + \frac{R_{v2}}{R_{v1}} \cdot i_{o2} \quad (R_{v1} \neq 0) \tag{4-2}$$

Once interface converter 2 is plugged in, the common DC bus voltage can be affected by both of these two parameters, and no effective and useful information can be used for bus signalling.

Figure 4.3(b) shows the general droop curves for paralleled interface converters [150] in a DC microgrid. Two curves share the same floating voltage, and current sharing can be attained through setting different droop coefficients, which is shown in the following equation (4-3),

$$i_{o1} = \frac{R_{v2}}{R_{v1}} \cdot i_{o2} \tag{4-3}$$

When interface converter 2 is plugged in, the DC bus voltage will rise due to the total output current being shared by interface converter 2. However, the bus voltage is locked under the floating voltage no matter how the load changes or the droop coefficient varies. Therefore, this group of droop curves is also not applicable for bus signalling.

The droop curves in Figure 4.3(c) have the same droop coefficient and different floating voltages. Their relationship is shown in equation (4-4),

$$i_{o1} = \frac{v_1^* - v_2^*}{R_{v1}} \cdot i_{o2} \tag{4-4}$$

Similarly, even though a constant current gap exists between the interface converters, it still has no effective parameters for bus signalling when interface converter 2 is plugged in.

Figure 4.3(d) shows one droop curve having zero droop coefficient. When interface converter 2 is plugged-in, the DC bus voltage can be reduced to v_2^*. The v_2^* is an effective value that can be used for bus signalling. Figure 4.3(e) shows a droop curve with zero droop coefficient, having a higher voltage than the floating voltage, and an intersection point on the negative part. In this case,

when interface converter 2 is plugged in, the DC bus voltage will be maintained at v_2^*, which is effective and can be used for bus signalling.

Compared with the two curves in Figure 4.3(d) and Figure 4.3(e), the lower voltage can also be easily reached if the load power is large enough in Figure 4.3(d). In practical implementation, it could lead to misinterpretation, and affect the effectiveness of bus signalling. Based on the above analysis, Figure 4.3(e) is selected for the bus signalling during the plug period.

4.3 Principle of the DC Bus Interacting Method

More details are added to the droop curves in Figure 4.3(e) and further shown in Figure 4.4. The bus voltage contains two voltage windows. The first one is a signalling voltage window, which only occurs over the signalling period. The other one is a working voltage window and has droop characteristics.

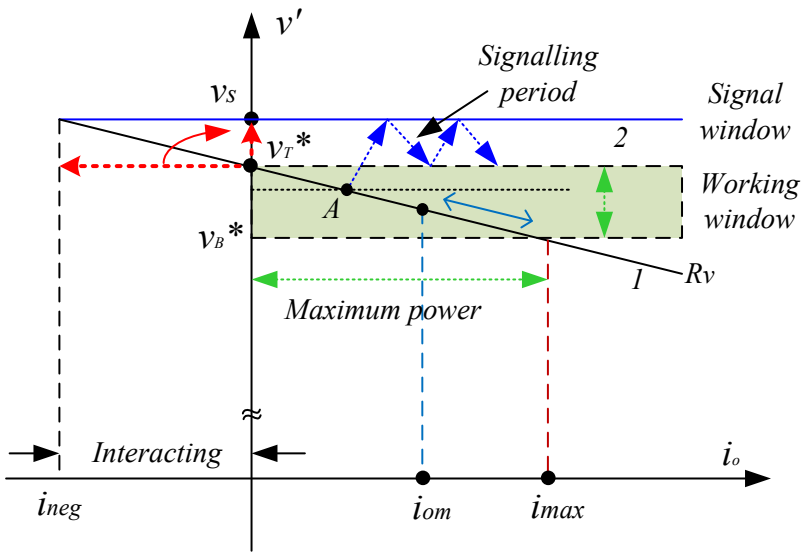


Figure 4.4 Dual window droop curves of interface converters.

Assuming an interface converter is working under droop curve 1, the v_T^* is top floating voltage for the control loop voltage reference, v_B^* is the bottom voltage where the maximum voltage deviation is allowed under the droop coefficient R_v, the maximum power difference allowed in this interface converter can be written in equation (4-5),

$$P_{max} = (v_T^* - v_B^*) \cdot i_{max} \tag{4-5}$$

where $v_B^* = (v_T^* - R_v i_{om})|_{i_{om}=i_{max}}$.

Theoretically, when interface converter 2 is plugged in and starts to conduct signalling, which means that the DC bus voltage will rise to the signal voltage v_S, it will generate a negative current i_{neg} due to the droop control in interface converter 1. The amplitude of i_{neg} can be expressed as equation (4-6).

$$i_{neg} = \frac{v_S - v_T^*}{R_v} \tag{4-6}$$

The negative current i_{neg} will cause an extra power burden for interface converter 2 because it not only needs to supply power to the load, but also must compensate for the interacting power introduced by the negative current. From the power balance consideration, interface converter 2 must satisfy the following equation (4-7),

$$P_2 \geq |v_S \cdot i_{neg}| + P_L \tag{4-7}$$

where the P_2 is power capability of interface converter 2; P_L is the load power.

In most practical applications, negative current is not desired because the power capacity of the converter to be connected to the DC bus is not guaranteed. For the Boost converter case, the excess power may cause instability in the system due to the non-minimum phase. Therefore, negative current compensation is required during this period. The compensation of the non-minimum phase will be further discussed and solved in Chapter 5.

The control block diagram of interface converter 2 is shown in Figure 4.5. The reason for interacting negative current is that the outer voltage loop is still active when the signalling interaction occurs. One solution is to isolate the outer voltage loop. Therefore, during the signalling period, the output current of the interface converter can still seamlessly operate with compensated positive current or zero current mode. The modified control block diagram is shown in Figure 4.6. In this case, the bus voltage is introduced to monitor the system state. Once the system is in signalling state, the outer voltage loop will be isolated. The current reference value

could be positive or zero to form positive current compensation or zero current compensation. Those compensations will be further discussed in the experimental section 4.5.1.

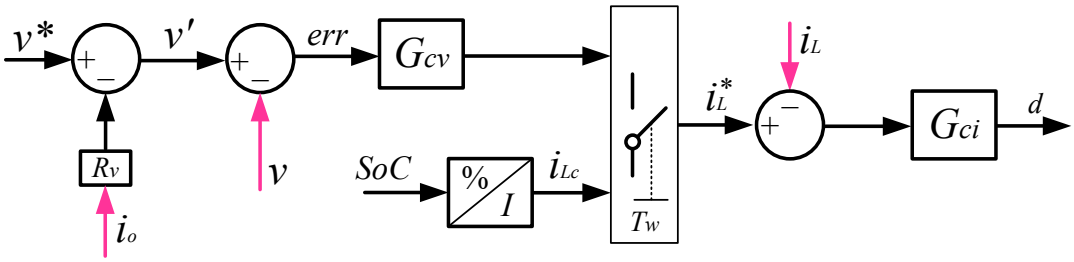


Figure 4.5 Control block of proposed DBI method.

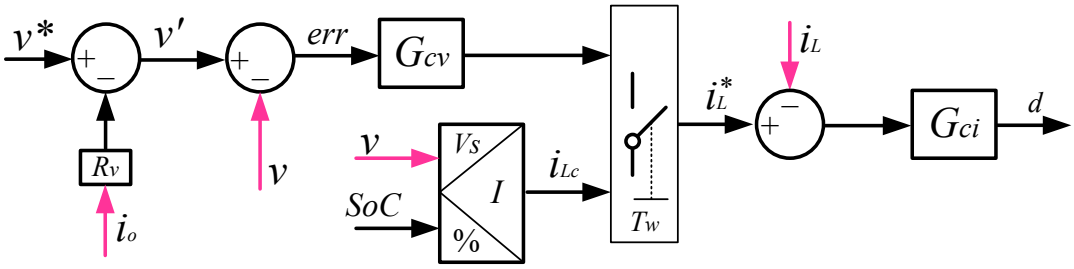


Figure 4.6 Control block of proposed DBI method with negative interacting current modification.

The common DC bus voltage participates in the inner current loop such that over the signalling period, the inner loop current reference i_{Lc} can be adjusted by the signal voltage v_S, which is shown as the red dashed arrow in Figure 4.4.

4.4 Signal Series Design

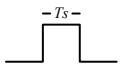
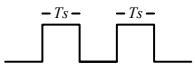
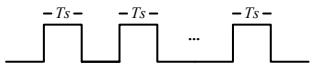
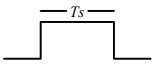
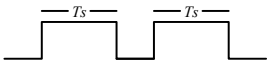
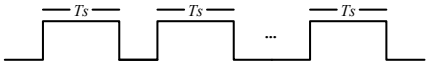
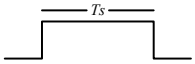
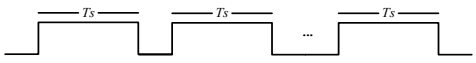
The above section discussed the working principle for achieving signalling. In this part, the signal series design will be introduced. As the blue dashed arrows show in Figure 4.4, the signal series can be designed with many options.

4.4.1 Signal Series and Extendibility

One of the easiest methods is to design different pulse widths to represent different distributed sources. A list of signal series design examples is shown in Table 4-1. Using different pulse

widths can be effective when the system does not contain a great number of distributed sources. However, the signalling period will last very long when the system has a large number of distributed sources. By noticing the signal series, the low part of the signal series is wasted, as the low voltage level is not used to define the signal series. Therefore, another way to make the signal series more effective is to use 1/0 to design the signal series.

Table 4-1 Signal series design with different pulse widths.

	Signal series with 1 bit	Signal series with 2 bits	⋯	Signal series with n bits
1			⋯	
2			⋯	
⋯	⋯	⋯	⋯	⋯
m			⋯	

Note: m is the number of distributed sources.

If assuming a fixed pulse width T_s and 5 bits for example, two signal series examples are shown in Figure 4.7. In this figure, the bit 1 represents the signal voltage v_S and bit 0 represents v_T^* or v, vice versa.

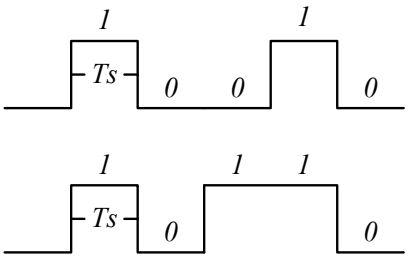


Figure 4.7 Signal series design with fixed pulse width and multiple bits.

Theoretically, for n bits signal series, there will be 2^n states, as equation (4-8) shows, for users to define.

$$\underbrace{C_2^1 C_2^1 C_2^1 \cdots C_2^1}_{n} = 2^n \ \ (n \geq 2) \tag{4-8}$$

Admittedly, the above two signal series design methods are not the only options. More protocol designs for different control functions and purposes are also feasible with the proposed dual-window DBS method. In this Chapter, a simple case study with a simple signal series is conducted in the experimental part (section 4.5.2) to validate the feasibility of the proposed method. A complex signal series with 6 bits will be used in Chapter 6 for the power sharing/management of DC microgrids.

4.4.2 Discussions of Signal Magnitude and Width

The key parameters of the proposed DC bus interacting method are the signal voltage v_S and the signal pulse width T_S. The signal pulse amplitude v_S can directly affect the DC bus voltage level. The requirement of choosing v_S is that it can be detected by the interface converters paralleled in the common DC bus. Assuming the system parameters are in Per Unit (PU), such as v_{bus}^{PU} for the common DC bus floating voltage in per unit, and v_s^{PU} for the signal voltage in per unit, then based on conventional DBS methods [66][74], let arbitrarily,

$$v_s^{PU} = 1.05 v_{bus}^{PU} \tag{4-9}$$

A signal pulse amplitude lower than this value is acceptable as long as the power noise from the DC bus voltage does not affect the signal and lead to misinterpretation. However, if the signal pulse amplitude is set to be too large, it significantly departs from the quiescent operating point. In this case, a redesign of compensators is required.

The selection of T_s depends on the control compensator and soft start time. The step response time of an interface converter normally ranges from micro-seconds to tens of micro-seconds. For Boost converters, the range of soft start time is dependent on their applications; it thus makes T_s range from tens of micro-seconds to hundreds of micro-seconds.

4.5 Experimental Validations

The experiment contains two parts. The first part shows the results of modification of negative interacting current; the second part shows a simple case study in which the proposed method can be used to actively control the other interface converter such that power sharing can be achieved. The experimental system configuration is shown in Figure 4.8.

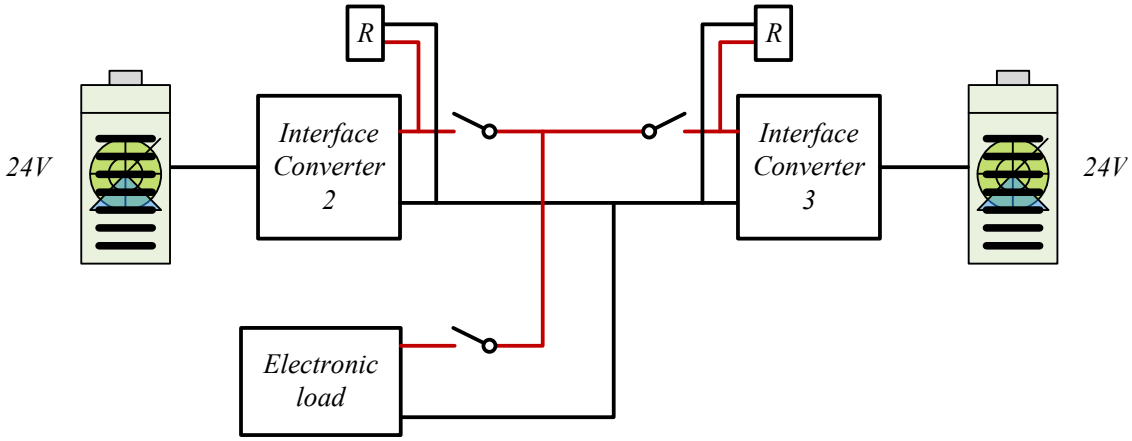


Figure 4.8 Experimental configuration for validating proposed DBI method.

The parameters used in this section are listed in Table 4-2.

Table 4-2 List of experimental parameters for dual-window DBI method.

Parameters	Values
v_S	52.5V
v_T^*	50V
v_B^*	45V
R_v	1Ω
R	220Ω·2
Electronic load	0-100W
Lead-acid battery banks	24V·2

4.5.1 Negative Interacting Current Modification

The experimental result of two interface converter interactions over the signalling period is shown in Figure 4.9. For illustration purposes, the signal pulse width is set as 2s, with 1 bit for observing the negative interacting current.

Interface converter 2 initially works under droop control, and interface converter 3 is plugged in at t_1. After a 3s delay (to conveniently show the results), interface converter 3 causes the DC bus to interact with interface converter 2, and the bus voltage is raised to 52.5V. During the signalling interaction period, the current in interface converter 2 is reduced to a negative value which is exactly as predicted. As the results, interface converter 3 injects a large current to supply both the load and the power caused by the negative current. It can be shown that plugged-in interface converter 3 has the power burden if there is no manipulation of the negative current. On the other hand, the interface converter to be plugged-in may not succeed in signal interaction if it has a low power capacity.

The results of compensating for the negative interacting current are shown in Figure 4.10 and Figure 4.11. The starting process is similar to that in Figure 4.9. The positive current compensation is shown in Figure 4.10. When interface converter 3 starts signalling, the bus voltage is regulated at the signal voltage, and due to the positive current compensation, the current in interface converter 3 is nearly zero in this case, which avoids the large current as shown in Figure 4.9. Therefore, the proposed current compensation method works very well. Similarly, zero current compensation is shown in Figure 4.11. In this case, the load power will be taken by interface converter 3 over the signalling period. The zero current compensation provides advantages for bidirectional power flow cases, such as battery banks.

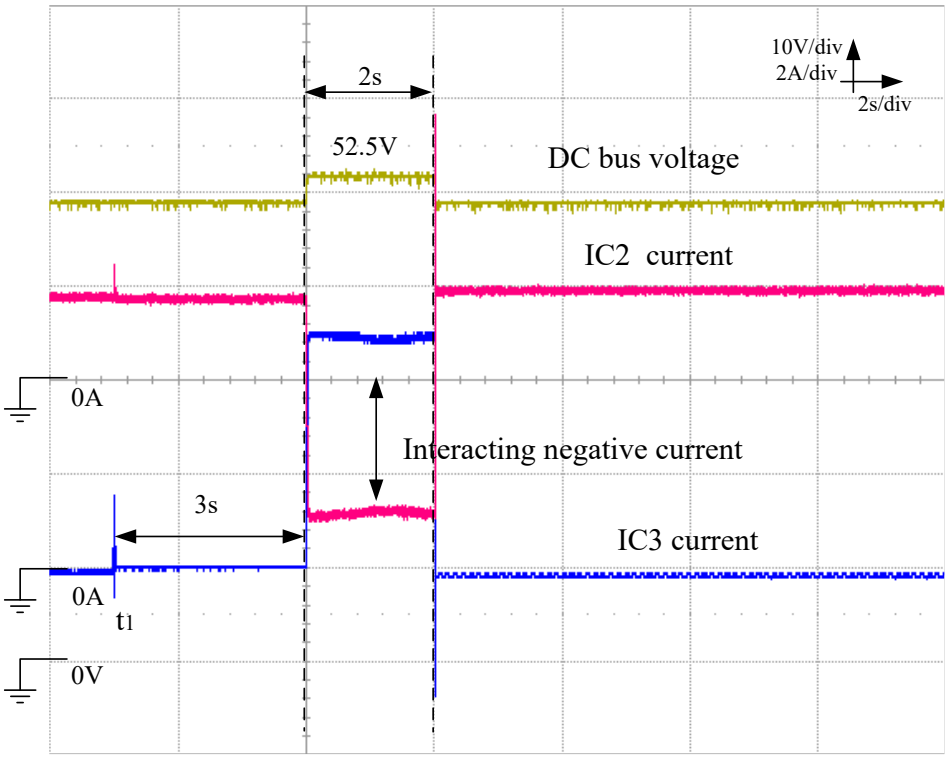


Figure 4.9 Experimental results of DBI method with negative interacting current.

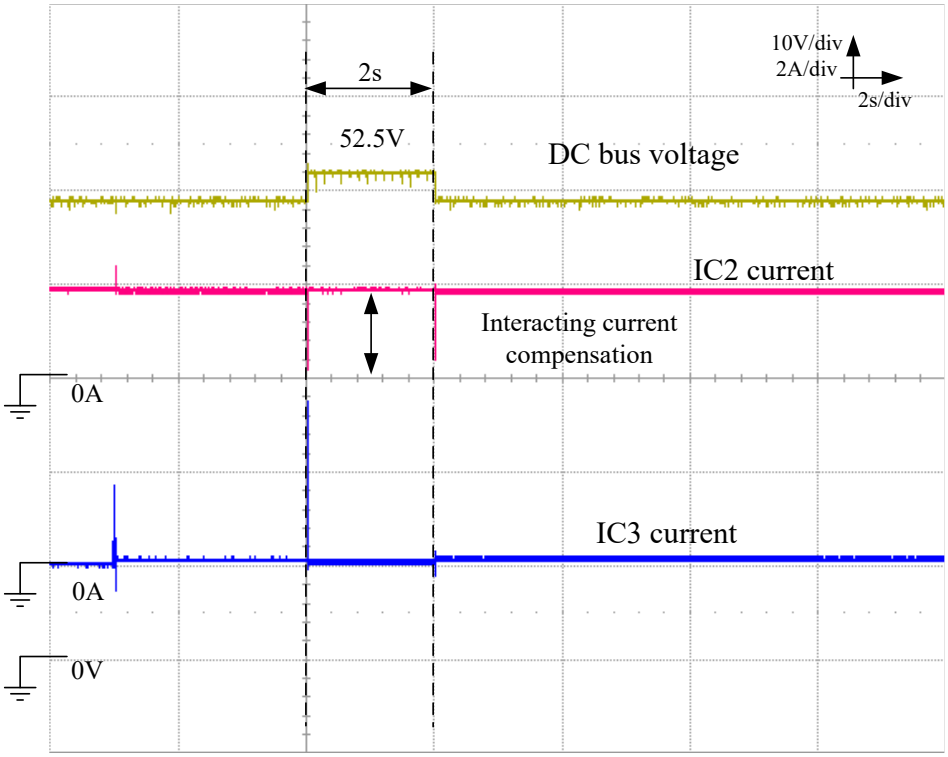


Figure 4.10 Experimental results of DBI method with positive interacting current compensation.

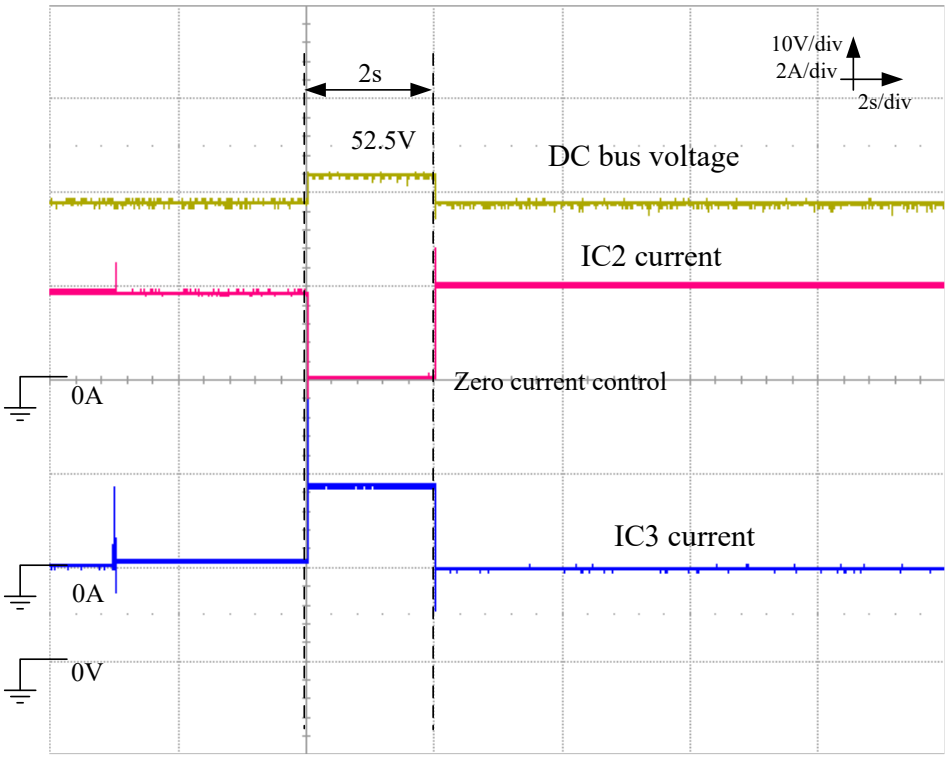


Figure 4.11 Experimental results of DBI method with zero interacting current compensation.

4.5.2 A Simple Case Study

A simple case study (has been published by the author as the reference [149]) is performed to validate the feasibility of the proposed method in power management. The signal series are chosen as two bits with pulse width 400*ms* as discussed in section 4.4. The experimental results are shown in Figure 4.12. The first signal series shown in this figure indicate that interface converter 3 is plugged in, which will be registered by interface converter 2. The second signal series shown in this figure is triggered by interface converter 2 to wake up interface converter 3 to participate in the power sharing with 1A. Similarly, when interface converter 3 is no longer able to supply the power due to the low SoC, it will send the signal series to interface converter 2 and then log off. Therefore, the two-way signalling is achieved by the proposed dual-window DBI control method. A complex signal series configuration to manage the power can be found in Chapter 6.

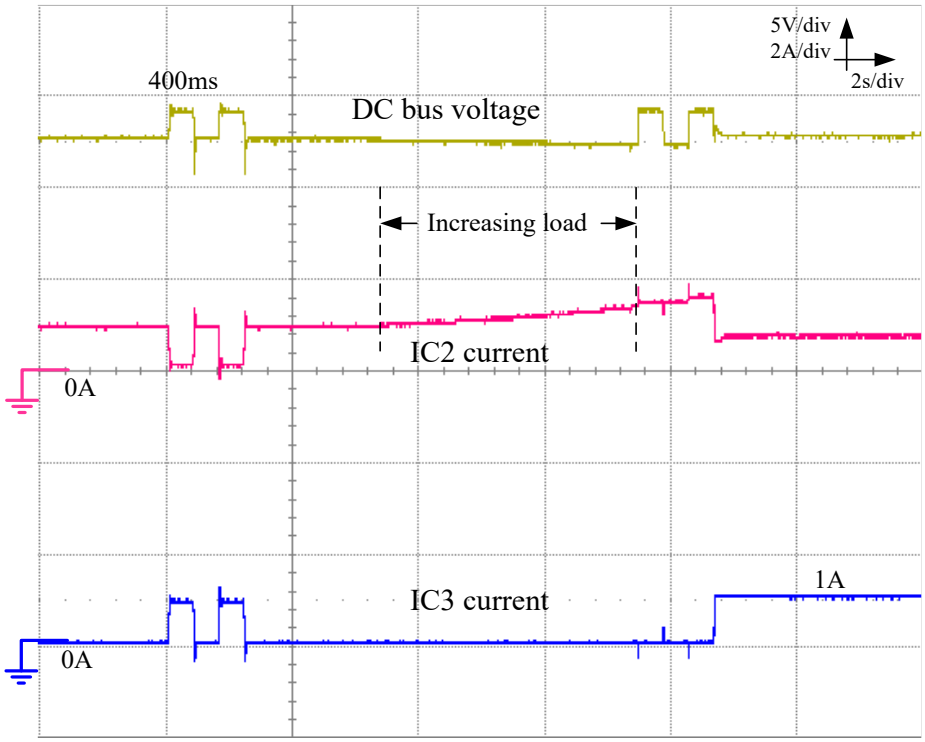


Figure 4.12 Experimental results of signalling with proposed DBI method, ON case.

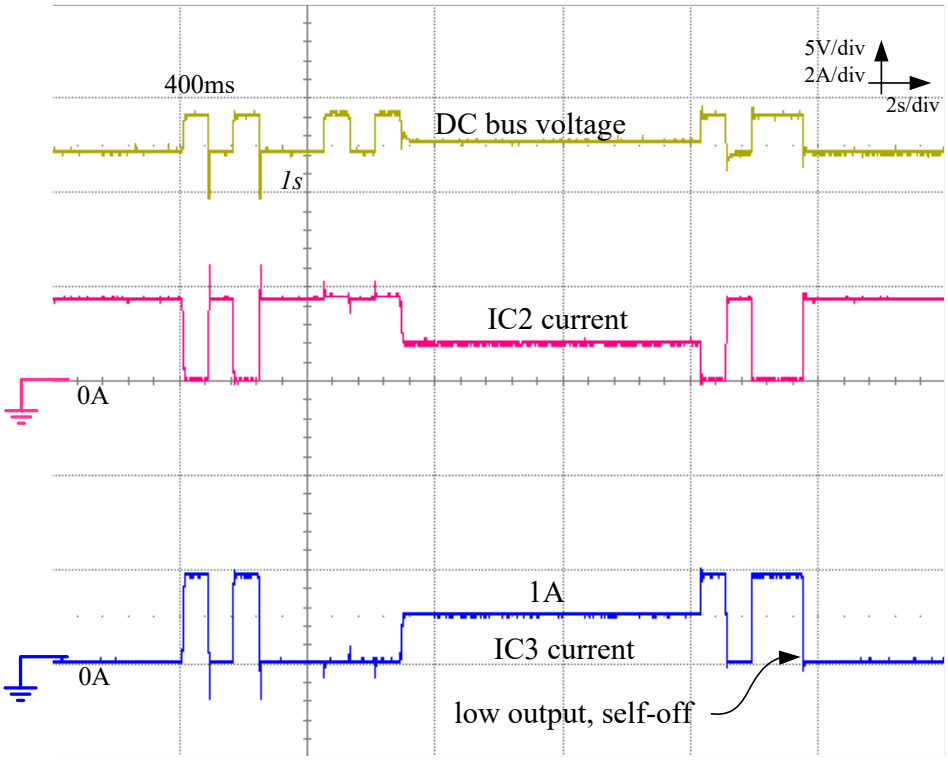


Figure 4.13 Experimental results of signalling with proposed DBI method, OFF case.

4.6 Conclusions

This chapter proposes a novel dual-window DBI control method for DC microgrids and discusses its mechanism and working principle. It can achieve plug and play performance as well as low speed signalling for power management for a DC microgrid. The idea behind the proposed DBI method originates from the various droop coefficient combinations. The theoretical existence of negative interacting current is addressed according to the practical application. The experimental results show the feasibility and effectiveness of the proposed DBI method.

The main contributions of this Chapter are the following:

A novel dual-window DC Bus interacting method is proposed for small scale DC microgrid control applications. With the DBI method, the interface converters within a DC microgrid system can exchange information without additional communication links and devices. This method does not change the previous controller parameters and is able to realise plug and play performance and low speed signalling. Compared with conventional DBS control, the proposed DBI method uses fewer voltage windows, has the potential to regulate more distributed sources, and is able to carry more information. Compared with PLC method, the proposed method does not need additional modulation and demodulation circuits and DFT programme. In addition, it is less impacted by line impedance than PLC.

The proposed DBI method has the following limitations:

This method relies on voltage sampling accuracy, which means that when the voltage transducer is broken or the voltage measurement is not accurate, this method will not work. Furthermore, this method will change the voltage level of the DC bus, which is not applicable to those applications with high requirements or sensitivity with regards to DC bus voltage. Finally, it has a limited information exchange rate compared with PLC but is sufficient for most DC microgrid control applications.

Chapter 5 Passive Stabilisers Design for Interface Converters

Boost converter is notorious for containing a non-minimum phase in transfer functions, which makes it more difficult to control compared with Buck converter. The non-minimum phase contained in the Boost converter transfer function makes it have the potential to threaten the system stability. The passive control theorem provides an idea for stable system analysis from the energy perspective. This theorem points out that a passive system is always stable. It provides the passive requirements for the transfer functions in linear time invariant (LTI) systems, which is called positive realness.

In this chapter, the passive theory is briefly introduced. The process to apply this theory to converter design and passivate the converter are explained. Besides, the parameters in the loop controllers based on the passive theory are illustrated. Finally, experimental results show the effectiveness of the proposed passive stabiliser.

5.1 Passive Theory—Brief Introduction

Passive theory is a systematic theorem to discuss the system stability (includes linear and nonlinear systems) and has many sub-theorems for different propositions and definitions. In this section, the author tries to abstract the theorems relevant to the design and requirement of interface converters. The full passivity theorem and related proofs in the following discussions can be found in the literature [151]. Passive theory discusses the stability from energy perspective. To put it

simply, if a system tends to consume the energy, then the system always tends to be stable. It can be illustrated as follows.

Consider a system with state variables $x \in R^n, u \in R^m$ and $y \in R^m$, if there exists a nonnegative function $H(x)$ and $\varepsilon(t)$ such that,

$$\int_0^t u^T(\tau)y(\tau)d\tau = H\big(x(t)\big) - H\big(x(0)\big) + \varepsilon(t) \tag{5-1}$$

Then the system is passive. Where $\int_0^t u^T(\tau)y(\tau)d\tau$ represents the energy supplied to the system, $H\big(x(t)\big) - H\big(x(0)\big)$ is the stored energy and $\varepsilon(t)$ represents the dissipated energy. This theory is widely applied in nonlinear systems. However, it is difficult to guide the linear controller analysis from design-oriented analysis (DOA). Fortunately, this theory also gives the passive requirement in the linear system.

Consider a stable LTI system as shown in equation (5-2).

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Eu \end{cases} \tag{5-2}$$

where $x \in R^n, u \in R^m$ and $y \in R^m$.

This system is said to be passive if and only if there exist matrices $P, L \in R^{m\times n}$ and $W \in R^{m\times n}$ with $P > 0, L > 0$ (positive definite) such that,

$$A^T P + PA = -Q^T Q - L \tag{5-3}$$

$$B^T P - C = W^T Q \tag{5-4}$$

$$W^T W = E + E^T Q \tag{5-5}$$

Lemma (Positive-real Lemma). A stable LTI system given in equation (5-2) with $E \neq 0$ is positive if and only if there exists a positive definite matrix P such that,

$$\begin{bmatrix} A^T P + PA & PB - C^T \\ B^T P - C & -E - E^T \end{bmatrix} < 0 \tag{5-6}$$

When $E = 0$, the above condition is reduced to,

$$A^T P + PA < 0 \tag{5-7}$$

$$B^T P = C \tag{5-8}$$

In most practical applications, it is not easy to the find the positive definite matrix P, and the above scheme is not applicable in real controller design. In DC/DC converter applications, the controller design is mainly based on the transfer functions. Therefore, the above input-output property can be defined on the transfer functions by introducing positive real transfer functions.

Definition A transfer function $G(s)$ is said to be positive real if

- $G(s)$ is analytic in $Re(s) > 0$;
- $G(j\omega) + G^*(j\omega) \geq 0$ for any frequency ω that $j\omega$ is not a pole of $G(s)$.

Here, $G^*(j\omega)$ is the complex conjugate transpose of $G(j\omega)$.

Theorem A linear system as given in equation (5-2) is said to be passive if and only if its transfer function $G(s) = C(sI - A)^{-1}B + E$ is positive real.

The above theorem forms an input-output version of the positive-real lemma in the frequency domain. For single input single output passive systems, the condition $G(j\omega) + G^*(j\omega) \geq 0$ reduces to $Re(G(j\omega)) \geq 0$, which means that the real part of their frequency response is always nonnegative. In other word, the phase shift is always within $[-90^o, 90^o]$, and for strictly passive system within $(-90^o, 90^o)$. In real scenario, the controller has limited bandwidth. Besides, sampling components, such as current and voltage transducers, have limited bandwidth. Therefore, the phase shift actually can be bounded within the switching frequency; then the above boundary can be written as equations (5-9).

$$Re(G(j\omega)) \geq 0, \omega \in (0, 2\pi f_s) \tag{5-9}$$

where f_s is the switching frequency of Boost converter.

A passive system is stable and easy to control. Therefore, the non-minimum phase contained in Boost converter then can be rendered with passivation. The passivation here refers to make the plant passive and (strictly) positive real.

5.2 Passivation for Interface Converters

The non-minimum phase contained in the Boost converter has the potential to threat the system stability. Commonly applied control methods for Boost converter are single loop voltage control and double loop voltage/current control. The non-minimum phase in voltage control plant transfer function contains second order terms, which makes the system difficult to control and the compensator structure complex. The double loop control eliminates the second order dominator and simplifies the outer loop control plant. This also simplifies the controller design. However, the non-minimum phase still exists, and could make the system unstable. From the transfer function analysis, the non-minimum phase makes the system have the negative part on Nyquist plot, and have the potential to encircle (-1, j0).

5.2.1 Modelling and Analysis of Interface Converters

The first step is to attain the converter transfer functions. Modelling of Boost converter with small signal analysis has been done in many literature [152][153]. For the analysis convenience and simplicity of models, the minor terms, such as inductor and capacitor equivalent parasitic resistance are ignored in this research. Accurate model and manipulations can be found in literature [153].

A typical interface converter connected to the DC bus is shown in Figure 5.1. By analysing the power switch ON and OFF state, average state equations are shown in equation (5-10) and equation (5-11).

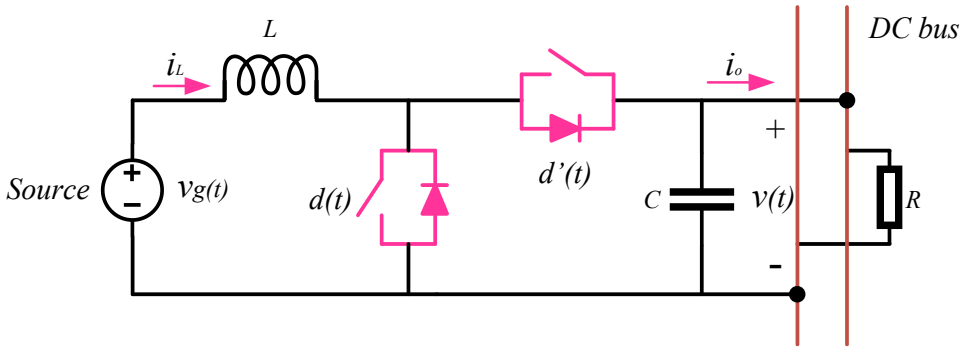


Figure 5.1 Interface converter in DC microgrids.

$$\begin{cases} L\dfrac{di_L(t)}{dt} = v_g(t) - d'(t)v(t) \\ C\dfrac{dv(t)}{dt} = d'(t)i_L(t) - i_o(t) \end{cases} \tag{5-10}$$

$$\frac{d}{dt}\begin{bmatrix} i_L(t) \\ v(t) \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{-d'(t)}{L} \\ \dfrac{d'(t)}{C} & 0 \end{bmatrix}\begin{bmatrix} i_L(t) \\ v(t) \end{bmatrix} + \begin{bmatrix} 0 & \dfrac{1}{L} \\ \dfrac{-1}{C} & 0 \end{bmatrix}\begin{bmatrix} i_o(t) \\ v_g(t) \end{bmatrix} \tag{5-11}$$

where $v_g(t)$ is the input voltage of distributed source, $i_L(t)$ is the inductor current, $v(t)$ is the terminal voltage, $i_o(t)$ is the output current, $d'(t)$ is equal to $1 - d(t)$ and $d(t)$ is the duty cycle of the PWM signal.

If denote $\mathrm{A} = \begin{bmatrix} 0 & \frac{-d'(t)}{L} \\ \frac{d'(t)}{C} & 0 \end{bmatrix}, B = \begin{bmatrix} 0 & \frac{1}{L} \\ \frac{-1}{C} & 0 \end{bmatrix}$, equation (5-11) can be written as equation (5-12).

$$\begin{bmatrix} \dot{i}_L(t) \\ \dot{v}(t) \end{bmatrix} = A\begin{bmatrix} i_L(t) \\ v(t) \end{bmatrix} + B\begin{bmatrix} i_o(t) \\ v_g(t) \end{bmatrix} \tag{5-12}$$

By applying small ac variations, calculations and manipulations, the equivalent ac small signal model of a Boost converter is shown in Figure 5.2.

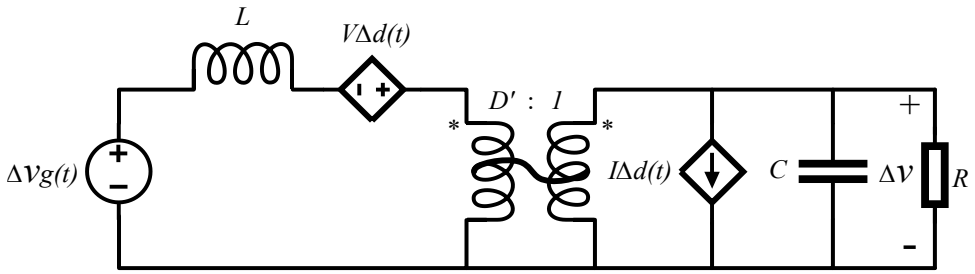


Figure 5.2 Equivalent model of Boost converter.

Transfer functions for the Boost converter are listed below from equation (5-13) to equation (5-16).

$$G_{vd}(s) = \frac{V}{D'} \cdot \frac{1 - s\dfrac{L}{D'^2R}}{den(s)} \tag{5-13}$$

$$G_{id}(s) = \frac{2V}{D'^2R} \cdot \frac{1 + s\frac{RC}{2}}{den(s)} \tag{5-14}$$

$$G_{vg}(s) = \frac{1}{D'} \cdot \frac{1}{den(s)} \tag{5-15}$$

$$G_{ig}(s) = \frac{1}{D'^2R} \cdot \frac{1 + sRC}{den(s)} \tag{5-16}$$

where $den(s) = 1 + s\frac{L}{D'^2R} + s^2\frac{LC}{D'^2}$.

The transfer functions can be displayed in Figure 5.3 for the convenience of controller design.

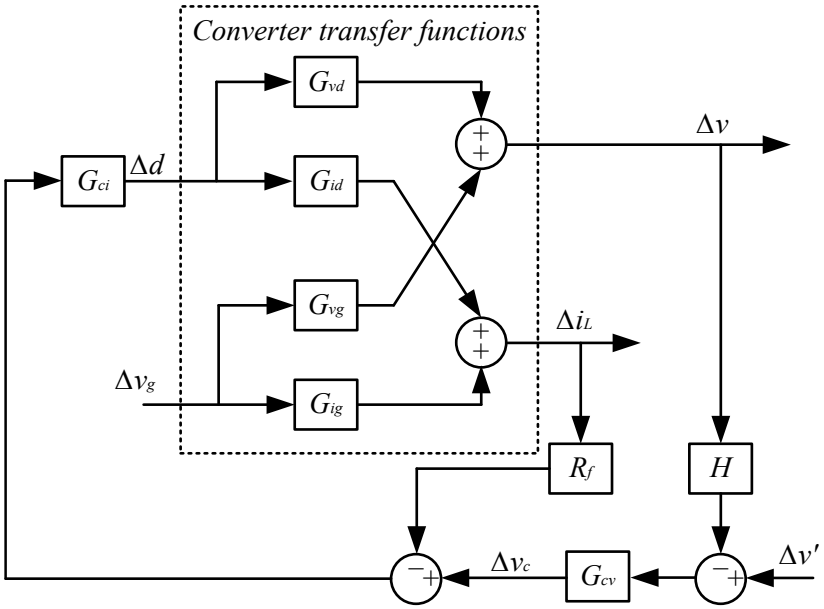


Figure 5.3 Converters transfer function map.

The inner loop transfer function G_{id} is shown in equation (5-14). The inner loop control plant has minimum phase numerator and second order dominator with infinite amplitude gain. All the passive components in the circuit are always larger than zero and the duty cycle D is always between (0,1), which mean that the inner loop G_{id} has no intersection with negative part of real axis on Nyquist plot. Thus, the inner loop is always stable.

The outer loop plant does not manifest from state equations, yet it can be attained from the transfer function map. With simple logic analysis from the transfer function map in Figure 5.3, the outer loop plant is the transfer function of inductor current reference to output voltage, as is shown in equation (5-17).

$$G_{vc} = \frac{\Delta v}{\Delta v_c} = \frac{\Delta v}{\Delta d}\frac{\Delta d}{\Delta v_c} \tag{5-17}$$

Δv_c is approximately equal to the inductor current multiplying the current sampling resistor R_f, which is because the purpose of the controller is trying to tune the value of inductor current to follow the value of Δv_c. Therefore,

$$\Delta v_c = \Delta i_L^* R_f \approx R_f \Delta i_L \tag{5-18}$$

By applying the equation (5-18) to equation (5-17), then the outer loop plant can be attained below,

$$G_{vc} = \frac{\Delta v}{\Delta v_c} \approx \frac{\Delta v}{\Delta d}\frac{\Delta d}{R_f \Delta i_L} = \frac{1}{R_f}\frac{G_{vd}}{G_{id}} \tag{5-19}$$

Applying the transfer functions G_{vd} and G_{id}, the outer loop control plant can be written as equation (5-20).

$$G_{vc} \approx \frac{1}{R_f}\frac{G_{vd}}{G_{id}} = \frac{D'R}{2R_f}\frac{1 - s\frac{L}{D'^2 R}}{1 + s\frac{RC}{2}} \tag{5-20}$$

Normally, the controller can be designed according to the control plant. However, by analysing this equation, the numerator contains the non-minimum phase, and it makes the outer plant have negative value over some frequency on Nyquist plot, which does not satisfy the positive real requirement. This may be the potential threat to the stability for the DC microgrid. The Nyquist plot of plant G_{vc} is drawn in Figure 5.4.

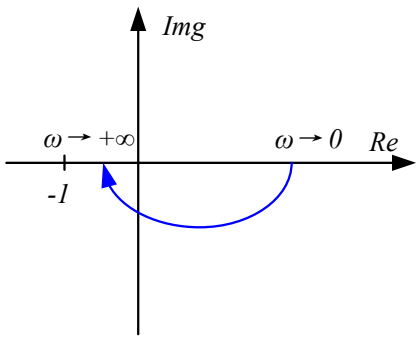


Figure 5.4 Nyquist plot of outer loop control plant.

In order to analyse how system components affect the system dynamics, for the calculation and reading convenience, let,

$$\alpha = \frac{D'R}{2R_f}, \beta = \frac{L}{D'^2R}, \gamma = \frac{RC}{2} \tag{5-21}$$

Then, the equation (5-20) becomes,

$$G_{vc} \approx \alpha \frac{1 - s\beta}{1 + s\gamma} \tag{5-22}$$

The dynamics over frequency domain can be analysed by substituting s with $j\omega$, one can get

$$\begin{aligned} G_{vc} \approx \alpha \frac{1 - s\beta}{1 + s\gamma} &= \alpha \frac{(1 - j\omega\beta)}{(1 + j\omega\gamma)} = \alpha \frac{(1 - j\omega\beta)(1 - j\omega\gamma)}{(1 + j\omega\gamma)(1 - j\omega\gamma)} \\ &= \alpha \frac{1 - j\omega\beta - j\omega\gamma + j^2\omega^2\beta\gamma}{1 - (j\omega\gamma)^2} \\ &= \alpha \frac{(1 - \omega^2\beta\gamma) - (\beta + \gamma)\omega j}{1 + \omega^2\gamma^2} \end{aligned} \tag{5-23}$$

The dominator is always positive. The real part $1 - \omega^2\beta\gamma$ has the potential to become negative when $\omega \to +\infty$. Therefore, at the low frequency and high frequency, the asymptotic value of G_{vc} is as shown below.

$$\omega \to 0, G_{vc} \to \alpha = \frac{D'R}{2R_f} \tag{5-24}$$

$$\omega \to +\infty, G_{vc} \to -\frac{\alpha\beta}{\gamma} = \frac{-L}{R_f D'RC} \tag{5-25}$$

By noticing this negative value, it can be found that increasing the value of capacitor and decreasing the load (equal to increasing the value of R) can make the total value move closer to the imaginary axis. So, one intuitive conclusion can be made is that increasing the capacitor or decreasing the load tend to make the system more stable in this case. This will be proved in experiment part. However, the inherent negative values cannot be overlooked.

5.2.2 Passivation with Feedforward Gain K

The physical mechanism of non-minimum phase is that it goes the opposite direction against the control signals. One of the efficient ways is to introduce the feedforward compensation to enhance the input dynamics over the output. Based on this analysis, the outer loop control block is then modified as Figure 5.5.

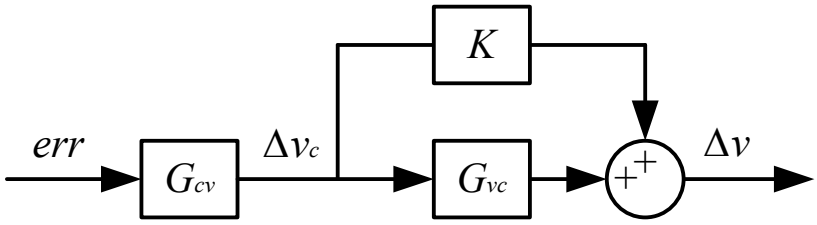


Figure 5.5 Control blocks of feedforward compensation for outer loop plant.

Similarly, by applying the feedforward compensation, the dynamic of outer loop plant is analysed as follows.

$$G'_{vc} = K + G_{vc} \approx K + \alpha\frac{1-s\beta}{1+s\gamma} = \frac{\alpha(1-s\beta)+K(1+s\gamma)}{1+s\gamma} = \frac{(\alpha+K)+s(K\gamma-\alpha\beta)}{1+s\gamma} \tag{5-26}$$

By replacing s with $j\omega$, the plant becomes

$$G'_{vc} \approx \left.\frac{(\alpha+K)+s(K\gamma-\alpha\beta)}{1+s\gamma}\right|_{s=j\omega} = \frac{\alpha+K+\omega^2\gamma(K\gamma-\alpha\beta)+j\omega[(K\gamma-\alpha\beta)-(\alpha+K)\gamma]}{1+\omega^2\gamma^2} \tag{5-27}$$

let $\omega \to 0$ and $\omega \to +\infty$, the value at low frequency and high frequency asymptotic can be written as follows,

$$\omega \to 0, G_{vc} \to \alpha + K = \frac{D'R}{2R_f} + K \tag{5-28}$$

$$\omega \to +\infty, G_{vc} \to K - \frac{\alpha\beta}{\gamma} = K - \frac{L}{R_f D'RC} \tag{5-29}$$

If the feedforward gain K equals to $\frac{\alpha\beta}{\gamma}$, the negative value can be compensated, thus outer plant is positive real according to passive theory and the passivation is completed.

However, the introduced feedforward gain K also alters the low frequency value, as shown in equation (5-28). This will lead to the natural voltage reference droop that will furtherly introduce voltage droop on quiescent operating point. The predicted Nyquist plot of compensated plant is shown in Figure 5.6.

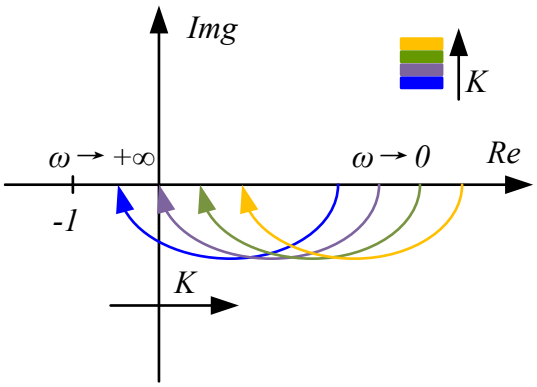


Figure 5.6 Nyquist plot analysis for passivation with K.

If keeping the quiescent operating point unchanged, then the quiescent operating point difference needs to be removed. Introducing the feedforward compensation alters the dynamics at both low and high frequency, while the low frequency alternation is not desired in most cases. Therefore, it should have a term to make the low frequency dynamic unchanged and compensate the high frequency negative value. Driven by this idea, high pass filter (HPF) has the feature to meet the above requirement.

5.2.3 Passivation with Feedforward HPF-K

Based on the requirements of suppressing the gain over low frequency to zero and keeping the high frequency part effective with gain K, the new feedforward compensator can be written as equation (5-30) shows.

$$G_p = K\frac{s}{s+\delta} \tag{5-30}$$

where δ is the corner frequency of passive controller.

Therefore, the new feedforward compensator control block is then shown in Figure 5.7.

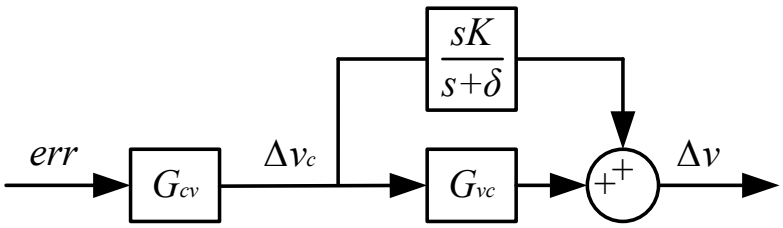


Figure 5.7 Control blocks feedforward compensation for outer loop plant with high pass filter.

Similarly, the asymptotic values over low frequency and high frequency can be examined as follows,

$$G'_{vc} = \frac{sK}{s+\delta} + G_{vc} \approx \frac{\alpha(1-s\beta)(s+\delta) + sK(1+s\gamma)}{(s+\delta)\cdot(1+s\gamma)} \tag{5-31}$$

By replacing s with $j\omega$, the plant becomes,

$$\begin{aligned} G'_{vc} &\approx \frac{(\alpha\delta + \omega^2\alpha\beta - \omega^2 K\gamma)(\delta - \omega^2\gamma) - j\omega(1+\gamma\delta)(\alpha\delta + \omega^2\alpha\beta - \omega^2 K\gamma)}{(\delta - \omega^2\gamma)^2 + \omega^2(1+\gamma\delta)^2} \\ &+ \frac{j\omega(\alpha - \alpha\beta\delta + K)(\delta - \omega^2\gamma) + \omega^2(\alpha - \alpha\beta\delta + K)(1+\gamma\delta)}{(\delta - \omega^2\gamma)^2 + \omega^2(1+\gamma\delta)^2} \end{aligned} \tag{5-32}$$

let $\omega \to 0$ and $\omega \to +\infty$, check the value at low frequency and high frequency approximation,

$$\omega \to 0, G'_{vc} \to \frac{\alpha\delta^2}{\delta^2} = \alpha = \frac{D'R}{2R_f} \tag{5-33}$$

$$\omega \to +\infty, G_{vc} \to \frac{-(\alpha\beta - K\gamma)\gamma\omega^4}{\gamma^2\omega^4} = K - \frac{\alpha\beta}{\gamma} = K - \frac{L}{R_f D'RC} \tag{5-34}$$

With noticing equation (5-33) and equation (5-34), the low frequency dynamic is not altered, and high frequency dynamic is then compensated by introduced gain K as expected. The predicted compensated Nyquist plot of plant is drawn in Figure 5.8. Therefore, the outer control loop is modified from the above passive compensation as required.

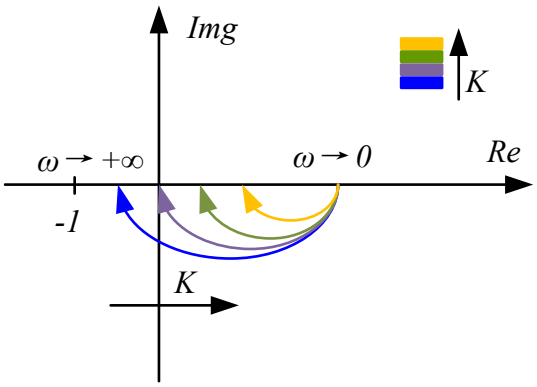


Figure 5.8 Nyquist plot analysis for passivation with HPF-K.

5.3 Discussion and Design

Based on the equation (5-34), one of the useful by-products from the proposed passivation is that the value of terminal capacitor can be reduced by increasing the passive controller gain K. Decreasing the value of terminal capacitor tends to move the negative intersection point far from the imaginary axis and make it encircle (-1, j0) on Nyquist plot. This reduces the margin and makes the system unstable. While the additional K can compensate the reduced margin and stabilise the system even when the terminal capacitor is reduced. In the case where terminal capacitor is unchanged, the passive controller can ensure the stable operation with large load variations.

5.3.1 Controllers Design

After the analysis of the passivation process described in section 5.2, the full control block diagram of interface converter can be attained by appropriate manipulations, which is shown in Figure 5.9.

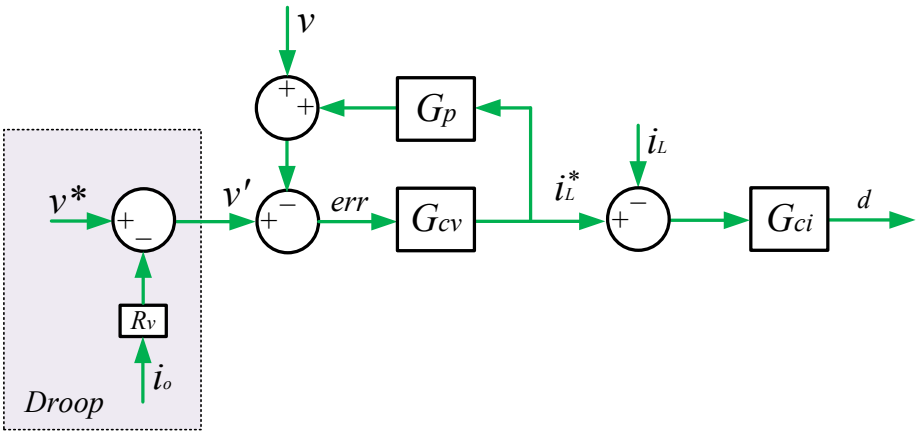


Figure 5.9 Full sketch of control block for interface converter.

The block contains the following controllers:

$$G_{ci} = G_{im} \cdot \frac{1 + \frac{\omega_{zi}}{s}}{1 + \frac{s}{\omega_{pi}}} \tag{5-35}$$

$$G_{cv} = G_{vm} \cdot (1 + \frac{\omega_{zv}}{s}) \tag{5-36}$$

$$G_p = \frac{sK}{s + \delta} \tag{5-37}$$

where G_{cv} is the outer loop controller, G_{ci} is the inner loop controller, and G_p is the passive controller.

The inner loop controller G_{ci} and outer loop controller G_{cv} can be designed from the conventional way with sufficient phase and magnitude margin. The proposed passivation is not to change the previous controllers and makes the whole system control complex. The only thing left is how to design the passive controller G_p.

The feedforward gain K is solved by above analysis, which is targeted at compensating the negative value; the corner frequency needs to be chosen from the frequency that outer loop plant enters the negative part in Nyquist plot, which means it requires that δ should satisfy the equation (5-38).

$$\delta = 2\pi f_p < \omega_N = 2\pi f_N \tag{5-38}$$

where ω_N/f_N is the frequency that outer loop plant enters the negative part; f_p is the corner frequency of passive controller.

By noticing the equation (5-23), the frequency that the plant steps into the negative area can be attained if let $1-\omega^2\beta\gamma=0$. The frequency is then shown in equation (5-39).

$$f_N=\frac{1}{2\pi}\sqrt{\frac{1}{\beta\gamma}} \tag{5-39}$$

By applying equation (5-21) to equation (5-39), the frequency that entering negative area is written as equation (5-40) (see Appendix A3.2 for detailed calculations).

$$f_N=\frac{1}{2\pi}\sqrt{\frac{2D'^2}{LC}} \tag{5-40}$$

Applying the parameters in Table 5-1, the Nyquist plots with passivation of K and HPF-K are shown in Figure 5.10 and Figure 5.11. The results are same as predicted in section 5.2.2 and section 5.2.3.

5.3.2 Discreteness of Controllers

The analysis is based on s domain. In a discrete digital system, the controllers need to be written in a discrete form and the process is also different from conventional PI controllers because of the introduced passivation loop.

The sampling time is required for the discrete forms of continuous transfer functions. The sampling time T_{sp} is set the same as switching frequency. Therefore, the discrete controllers (by bilinear approximation) applied in the DSP routine can be written as follows.

$$G_{ci\_d}=\frac{0.1493+0.03334z^{-1}-0.116z^{-2}}{1-1.12z^{-1}+0.1202z^{-2}} \tag{5-41}$$

$$G_{cv\_d}=\frac{49.73-48.7z^{-1}}{1-z^{-1}} \tag{5-42}$$

$$G_{p\_d}=\frac{0.406-0.406z^{-1}}{1-0.9875z^{-1}} \tag{5-43}$$

Applying the discrete controllers listed from equation (5-41) to equation (5-43) to Figure 5.9, the whole control process is then completed.

Table 5-1 Parameters used in both simulations and experiment.

Parameters	Values	Parameters	Values
Converter parameters			
L	$240\mu H$	V^*	50V
C	$470\mu F$	R	10Ω
f_s	25kHz	V_g	25V
Controller parameters			
R_v	0.5	ω_{zv}/f_{zv}	250Hz
G_{im}	0.3016	K	0~2.5
ω_z/f_z	1kHz	δ/f_{pa}	50Hz
ω_p/f_p	6.25kHz	T_{sp}	$40\mu s$
G_{vm}	49.2183		

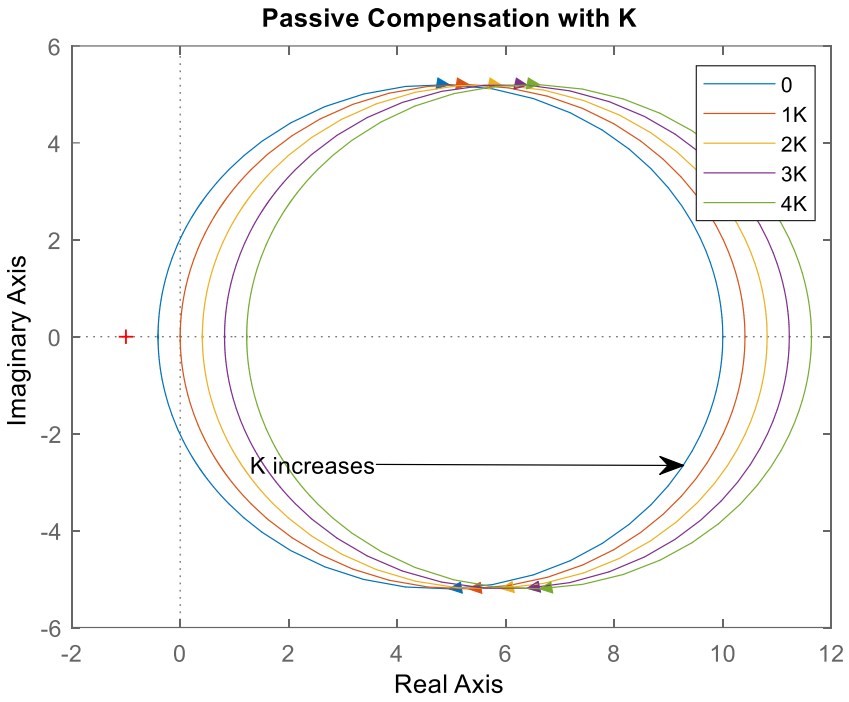


Figure 5.10 Nyquist plot passivation with K.

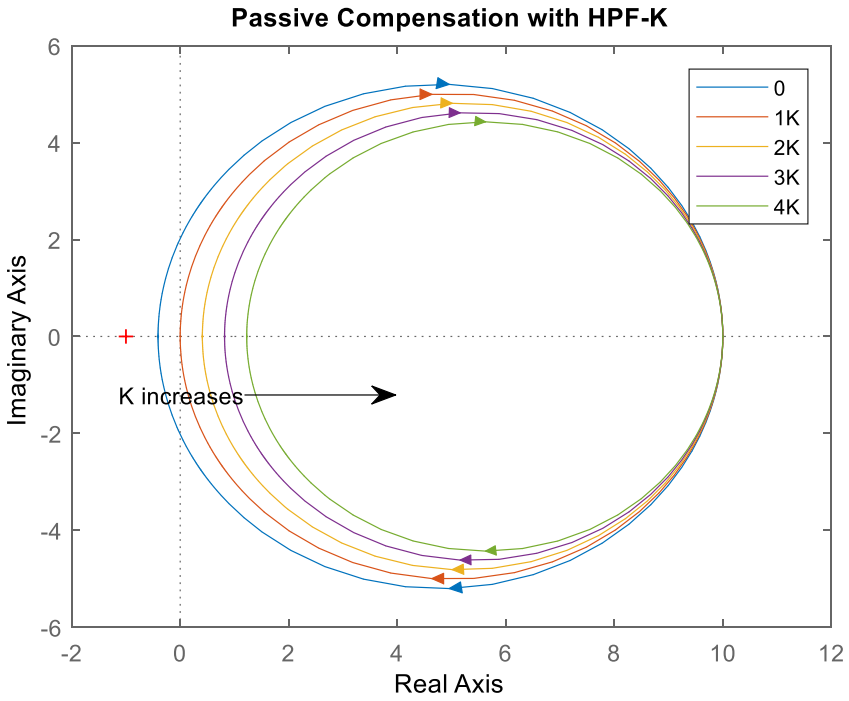


Figure 5.11 Nyquist plot passivation with HPF-K.

5.4 Experimental Validation

The experimental validation will be illustrated from two parts. The first part is to validate the effectiveness of the proposed passivation method for the interface converters. The second part is to validate that the modified feedforward compensator, which can stabilise the interface converter without changing of quiescent operating point.

5.4.1 Validation of Passive Stabilisers

The inner loop and outer loop controllers are not changed, and the controllers are designed from the values in Table 5-1. The converter will become unstable when the load reaches over 250W. When reducing the output capacitor, the instability can come earlier before the load reaches 250W based on above analysis. Therefore, in experiment, in order to show the effectiveness if proposed passivation methods, the capacitor is then reduced to 100uF and instability occurs as shown in Figure 5.12.

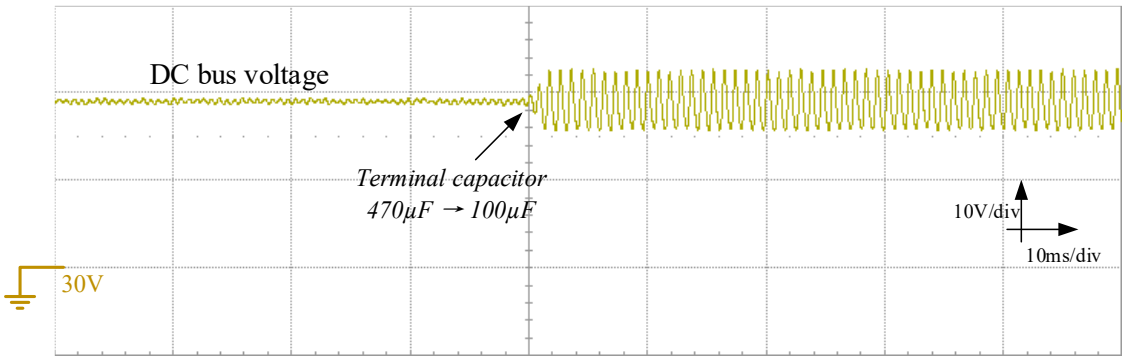


Figure 5.12 Reducing the terminal capacitor to make the system oscillate.

When applied the feedforward K compensator, the oscillation is then supressed as the result shown in Figure 5.13. An obvious voltage drop occurs because the introduced feedforward gain K impact the quiescent operating point as predicted.

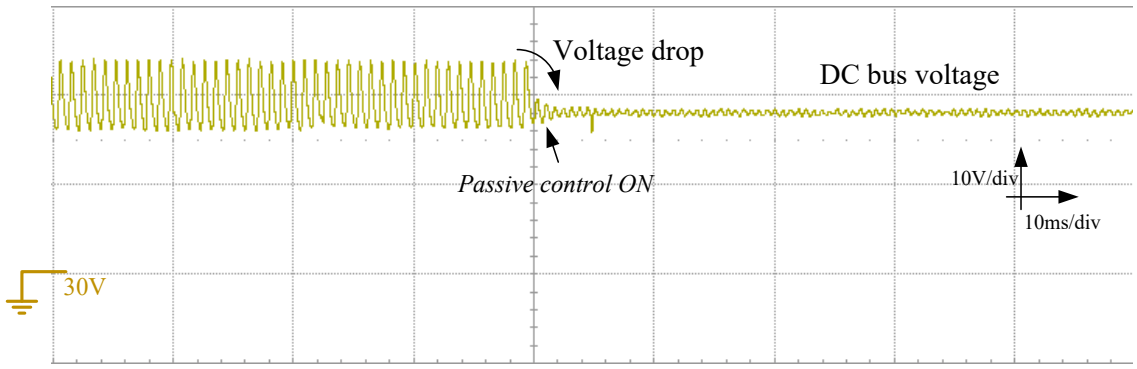


Figure 5.13 Unstable case becomes stable by applying passive control with expected voltage drop.

5.4.2 Modified Passive Stabilisers

The second part is to show the effectiveness of feedforward compensator with a high pass filter. In most cases, the natural voltage droop is not desired, and it is better to keep the previous features of interface converter. For example, introducing droop control discussed in Chapter 4 will further lower the bus voltage. Therefore, the high pass filter shows importance in this situation. The passivation results are shown in Figure 5.14 and Figure 5.15. It can be seen that large feedforward gain has better performance. Besides, introduced high pass filter will eliminate the impact on the alteration of quiescent operating point.

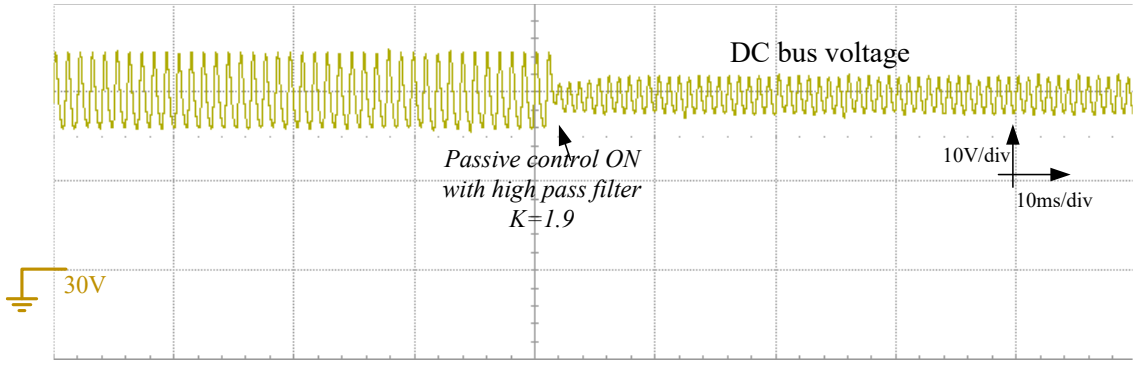


Figure 5.14 Unstable case becomes stable by applying passive control with HPF, K=1.9.

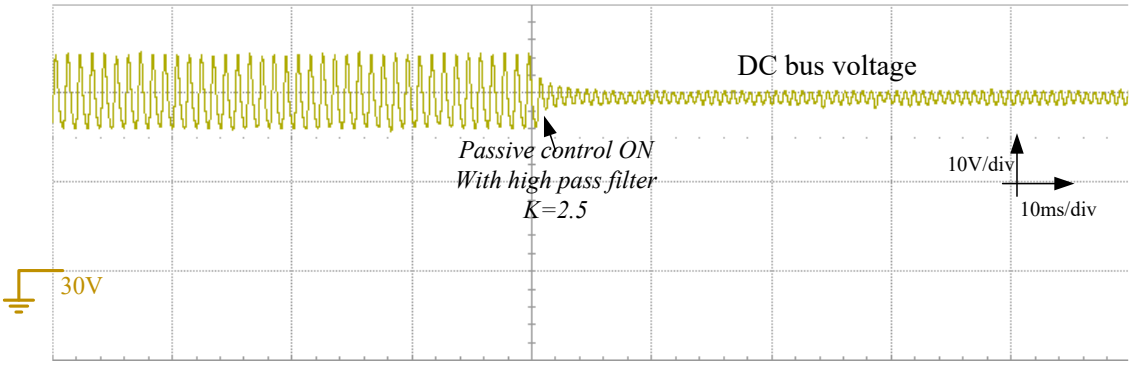


Figure 5.15 Unstable case becomes stable by applying passive control with HPF, K=2.5.

The instability can also occur in two paralleled interface converters. The two interface converters are both working at droop control with average current sharing. When switching off the passive stabilisers, the instability occurs immediately, which is shown in Figure 5.16.

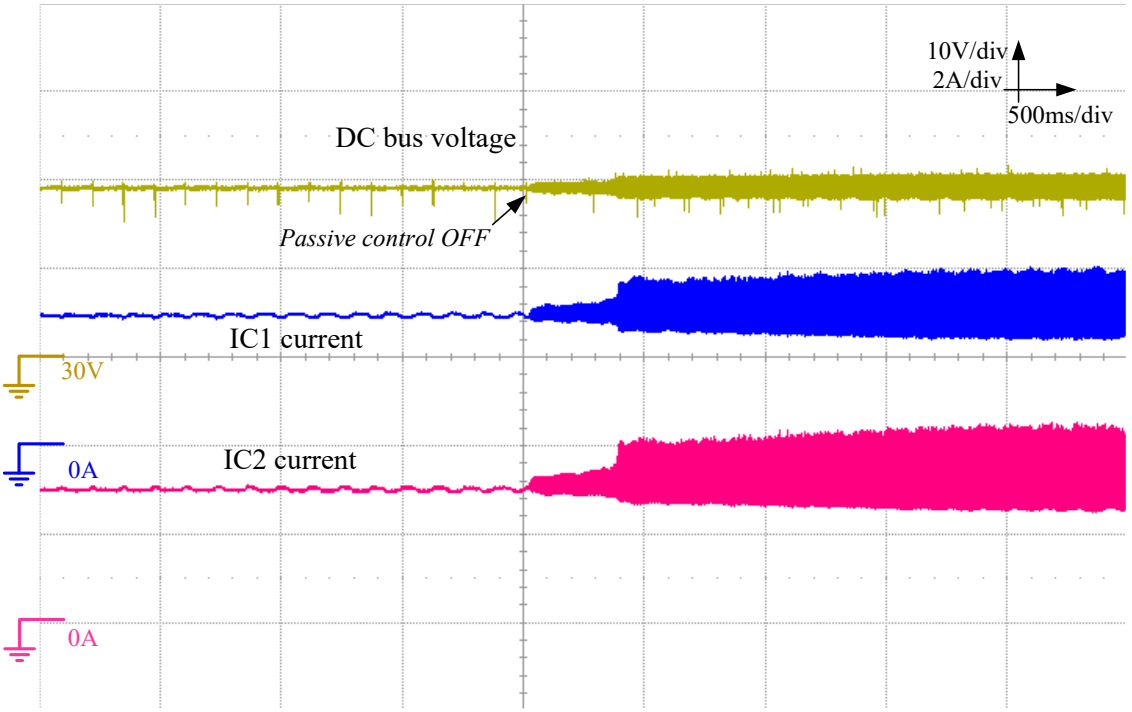


Figure 5.16 Instability occurs when the passivation controller is removed from two parallel interface converters with average current sharing droop control.

Therefore, the effectiveness of proposed passive stabiliser is experimentally validated. Adding the passivation loop can increase the stability of interface converters. It can help to enhance the stable performance in dealing with the fast and frequent load variations and load power sharing. As a by-product, introducing the passivation loop can also help reduce the size of the DC bus capacitor.

5.5 Conclusions

This Chapter presents the design of the passive controller for the primary control of interface converters. The passive controller is based on passive theorem to make the system transfer function react positive realness. Two types of controller are proposed and discussed, which is passivation K and passivation HPF-K respectively. Finally, the effectiveness of proposed passive stabiliser is experimentally validated.

The main contributions of this Chapter to the literature are the followings:

This chapter proposes a new passivation method for the Boost converters design to compensate the non-minimum phase. Compared with conventional methods, the proposed method does not need to modify the circuit topology to deal with non-minimum phase. It only modifies the structures of control blocks, which simplifies design process. Besides, it lines up with the double loop control design, which makes the proposed method compatible. In addition, this passive controller does not require the manipulation of the parasitic resistance on the output capacitor. Therefore, the output voltage ripple will not be impacted. Because of the flexible mechanism of proposed passive controller, the size of terminal capacitor can be reduced by increasing the feedforward gain, which makes the system less bulky than conventional control.

Chapter 6

Operation of DC Microgrids with Enhanced Stability in a Hierarchical Control Scheme

Chapter 4 proposes a dual-window DBI method for power management in DC microgrids. Chapter 5 proposes a passive stabiliser for enhancing the stability of an interface converter, so that the non-minimum phase contained in the interface converter is no longer a potential threat to the system stability.

In this Chapter, a DC microgrid system will be operated under a novel hierarchical control scheme, which includes the proposed dual-window DBI method and passive stabiliser. The DC microgrid consists of a grid-connected interface converter, two interface converters with battery storage, one interface converter with PV source, electronic and resistance loads. The terminal admittances of the interface converter under different working modes are modelled and discussed, which proves that the system is stable within the proposed control strategy. A six-bit signal series will be implemented for dual-window DBI signalling. The power regulation and management strategy used in this system is based on a typical home application. It has following features:

- Plug and play performance for distributed sources;
- Seamless on-grid and off-grid operation transfer;
- On grid and off grid power management without additional communications;

- PV power limitation for off-grid operation.

The reliability of the system under the proposed control scheme is also validated by the dynamic MPPT and load variations. Many operation situations are conducted in the experimental part.

6.1 System Control Configurations

6.1.1 Definitions of Each Control Layer

The DC microgrid in this Chapter works under a novel hierarchical control scheme. The primary controls and controller parameters are identical for all the interface converters and are passively stabilised according to the passive stabilization method presented in Chapter 5. Therefore, the stability over the whole operation process can be guaranteed. The secondary control is droop control, which is used for plug and play performance and signalling. In the tertiary control layer, the information attained from the signal series will determine the working state of interface converters, such as charging/discharging states, which is based on active signalling methods as discussed in Chapter 4. The hierarchical diagram is shown in Figure 6.1.

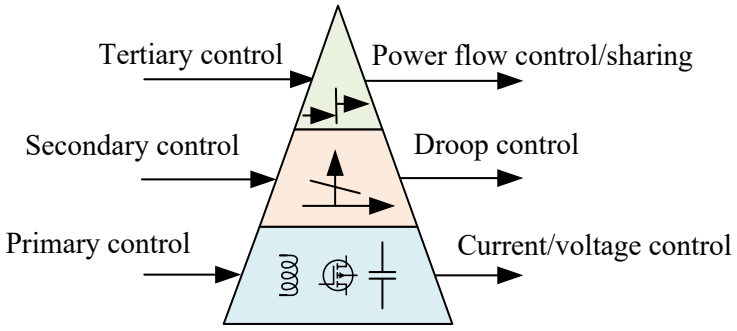


Figure 6.1 Functions of each control layer in hierarchical control scheme.

6.1.2 System Control Diagram

The system control diagram is shown in Figure 6.2, which contains a grid interface converter (IC1), two energy storage converters (IC2 and IC3), one PV interface converter (IC4), electronic

load and resistance loads. The grid converter is composed of a DC power source and a Boost converter. There are four identical bidirectional Boost converters in the system. In order to simulate the situation where the power from the microgrid feeds back to the utility grid, a resistance is used to soak up the surplus power from the DC microgrids, which can also be seen in Figure 3.9.

By examining the control blocks in Figure 6.2, the parameters, R_v and i_L^*, can be controlled/modified to manage the power balance. Regulating the droop coefficients to manage the power has been analysed and reviewed in Chapter 2. This method has some drawbacks, such as inaccurate power sharing and vulnerability from line impedance. Varying the i_L^* is an efficient power management method, or in other words, the interface converter works as a current source, which coincides with the analysis in Chapter 4. The working state of each interface converter can seamlessly transit between voltage mode and current mode over the signalling and normal working states. The mechanism of this control scheme is based on the MSC such that the power sharing accuracy can be guaranteed.

The PV generations can be regarded as constant current/power sources when they work under MPPT modes. The power flow of PV generation has only one direction, which means that they always inject power into the DC microgrids. If they are operated as voltage sources, the maximum power output will be sacrificed [73] as a trade-off. In this Chapter, the PV generation is operated at MPPT mode for maximum power output. The surplus power will be limited with a dedicated modified MPPT algorithm when the system works under off-grid mode.

Last but not least, adjustable electronic load can be operated as either constant power load or resistance load. The electronic load can be controlled from the computer interface. Therefore, the dynamic load variation can be achieved to validate the reliability of the proposed control scheme.

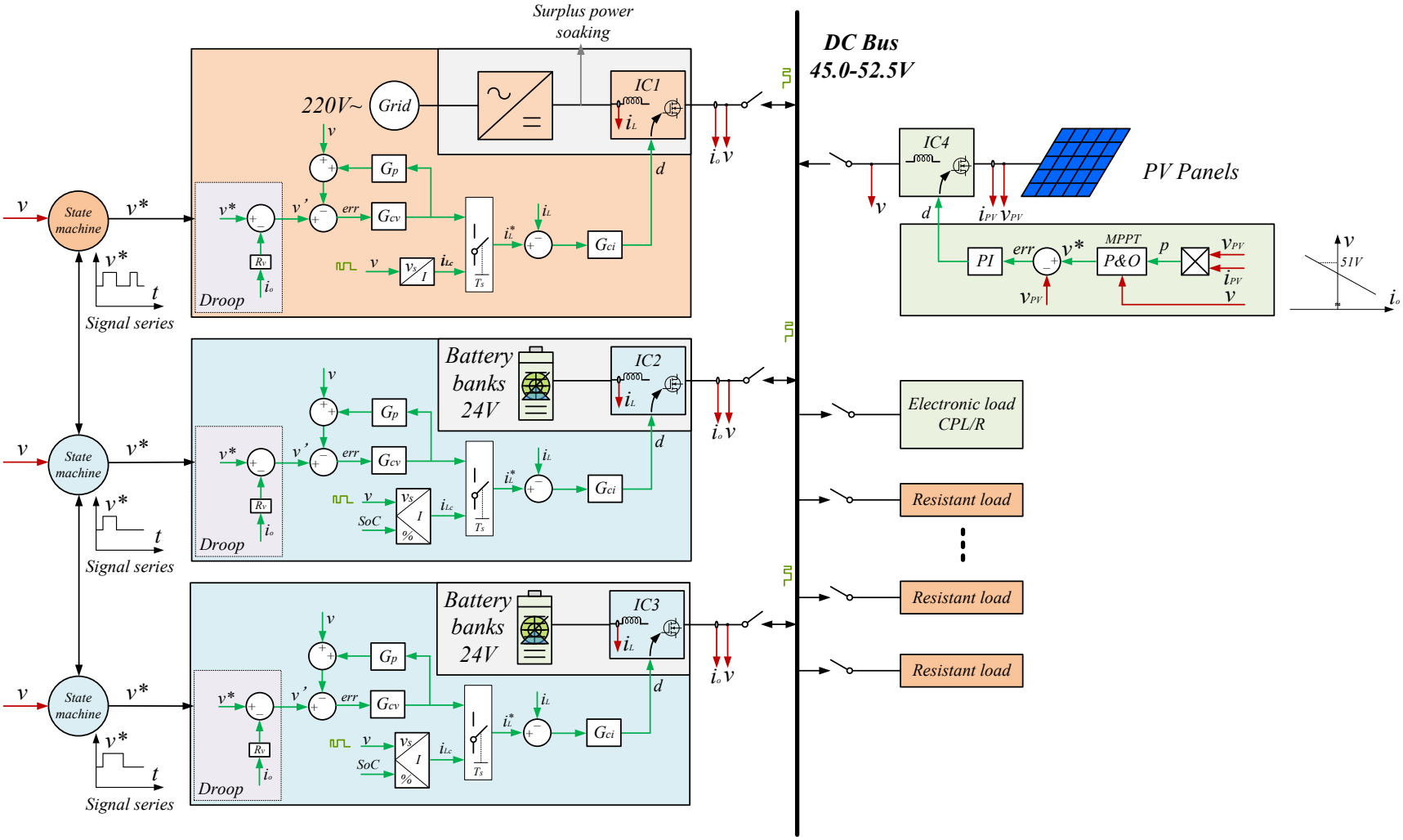


Figure 6.2 System control configuration diagram.

6.2 Terminal Admittance Modelling and Analysis

Based on the system control configuration diagram in Figure 6.2, the interface converters in the proposed DC microgrid system contain the following working modes: voltage mode, power injecting mode, and power absorbing mode. In addition, in voltage mode, the way in which the droop control and proposed passive stabiliser shape the terminal admittance will be shown step by step.

The system contains battery banks, and they have two working modes: charging and discharging mode. These two working states show different terminal impedance. Due to the fact that all the converters are connected in parallel, it is more convenient to analyse their admittances Y_T. As for the impedance, it can be easily attained by $Z_T = \frac{1}{Y_T}$.

6.2.1 Load Side Input Admittance

Unlike tightly regulated converters, battery energy storage has fixed terminal voltages. Therefore, power flow control is achieved through the inner current loop. Considering the battery works under the charging state, which is shown in Figure 6.3, the terminal input admittance can be attained as following discussion.

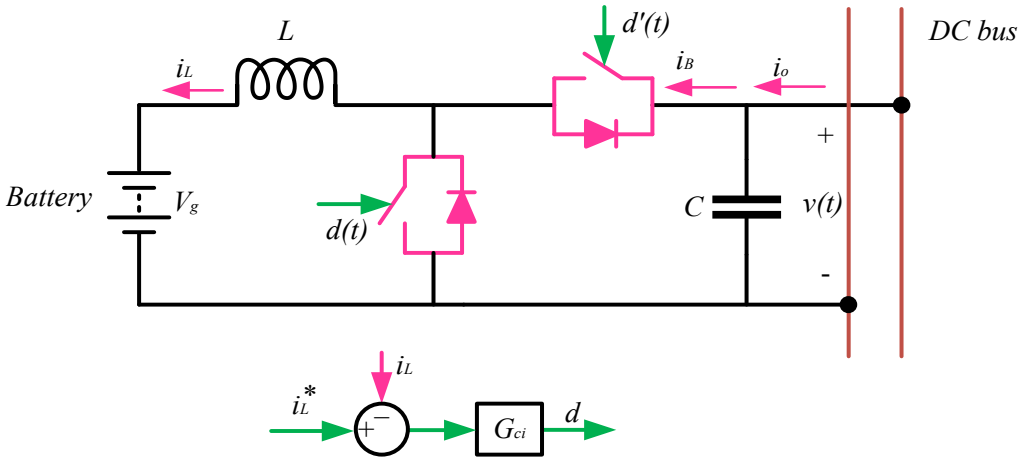


Figure 6.3 Terminal admittance modelling for battery charging mode.

By applying small signal analysis, and neglecting the decoupling capacitor on the battery side, the following equations can be attained based on the circuit diagram:

$$\Delta i_L(s) = \frac{(1-D)\cdot \Delta v(s)}{sL} - \frac{\bar{V}\cdot \Delta d(s)}{sL} \tag{6-1}$$

$$\Delta i_B = \Delta i_L \cdot (1-D) - \Delta d(s)\cdot \bar{I_L} \tag{6-2}$$

$$\Delta i_o(s) = \Delta i_B + sC\cdot \Delta v(s) \tag{6-3}$$

Then, based on the control block, the duty cycle variation can be attained.

$$\Delta d(s) = -\Delta i_L \cdot G_{ci} \tag{6-4}$$

The above equations are sorted and assigned to signal flow charts, as shown in Figure 6.4.

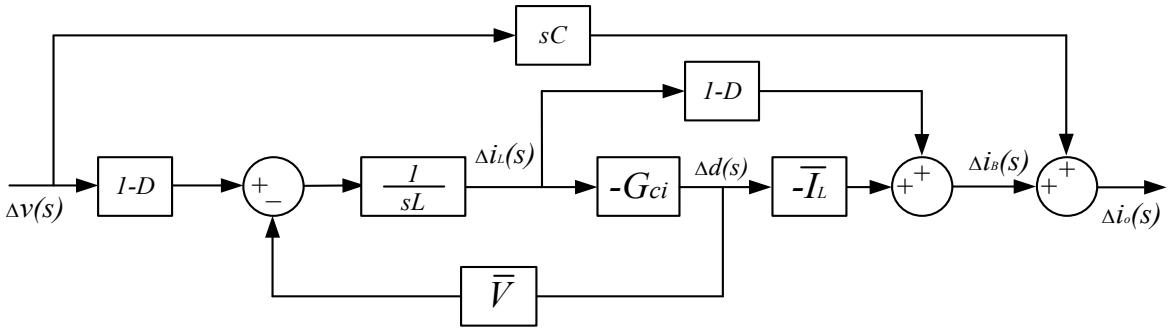


Figure 6.4 Signal flow chart of terminal admittance for battery charging mode.

By applying Mason's gain formula (MGF) and calculations, the terminal admittance can be attained in equation (6-5).

$$Y_T^{Bat\_CPL} = \frac{\Delta i_o(s)}{\Delta v(s)} = \frac{(1-D)G_{ci}\bar{I_L} + (1-D)^2 + sC(sL - G_{ci}\bar{V})}{sL - G_{ci}\bar{V}} \tag{6-5}$$

Similarly, when the battery banks work in discharging mode, the current direction will be reversed. The terminal admittance of current injecting source is written in equation (6-6).

$$Y_T^{Bat\_CPS} = -\frac{\Delta i_o(s)}{\Delta v(s)} = \frac{(1-D)G_{ci}\bar{I_L} + (1-D)^2 + sC(sL + G_{ci}\bar{V})}{sL + G_{ci}\bar{V}} \tag{6-6}$$

Replacing G_{ci} from the equation (5-35), and let $s \to 0$, the terminal admittance approximation at low frequency can be attained in equation (6-7).

$$Y_T^{Bat\_CPL} \to \frac{(1-D)G_{im}(\omega_z)\overline{I_L}}{-G_{im}(\omega_z)\overline{V}} = \frac{(1-D)\overline{I_L}}{-\overline{V}} = -\frac{\overline{I_o}}{\overline{V}} = -\frac{1}{R} \tag{6-7}$$

It can be seen that the terminal admittance in low frequency approximation is negative, which acts like a constant power load. The result coincides with the analysis in Chapter 2, section 2.2. The high frequency approximation is dominated by the capacitor, which also can be seen in equation (6-5). The capacitor always contains one order higher than the other terms. Therefore, the terminal admittance always tends towards infinite. The detailed derivations and calculations of terminal input admittance are shown in Appendix A4.

Similarly, when the battery works in discharging mode, performing as a constant power source, the terminal admittance over low frequency approximation can be attained based on equation (6-6), the results is $\frac{1}{R}$, which is shown in equation (6-8).

$$Y_T^{Bat\_CPS} \to \frac{(1-D)G_{im}(\omega_z)\overline{I_L}}{G_{im}(\omega_z)\overline{V}} = \frac{(1-D)\overline{I_L}}{\overline{V}} = \frac{\overline{I_o}}{\overline{V}} = \frac{1}{R} \tag{6-8}$$

Therefore, it can be concluded that when the battery works as a constant power source it will not impact the system stability. This result also agrees with the previous studies in chapter 2, section 2.2.3. The terminal admittance over the whole frequency range is shown in Figure 6.5.

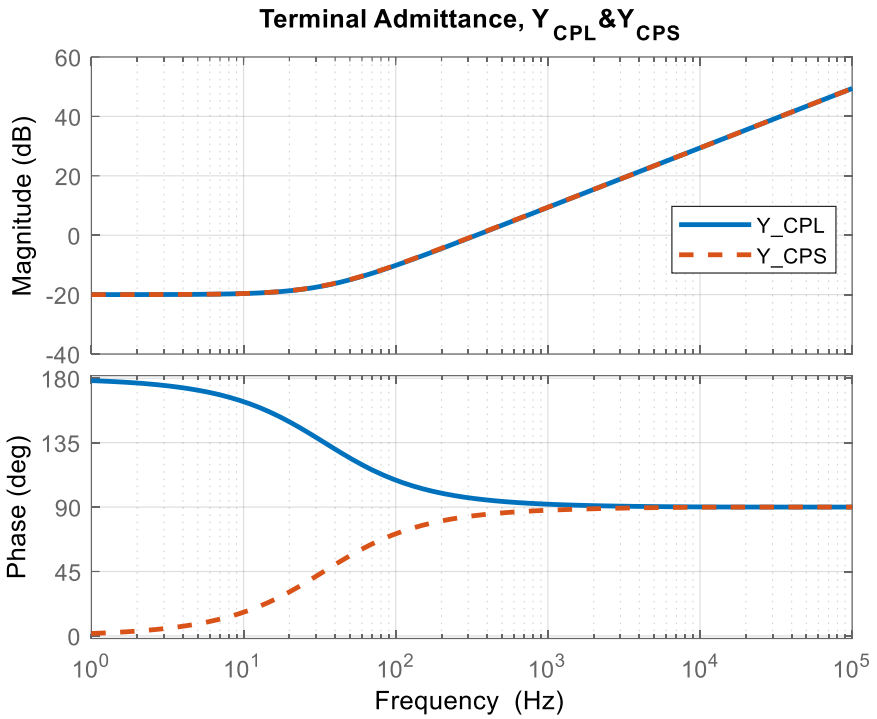


Figure 6.5 Terminal admittance of CPL and CPS.

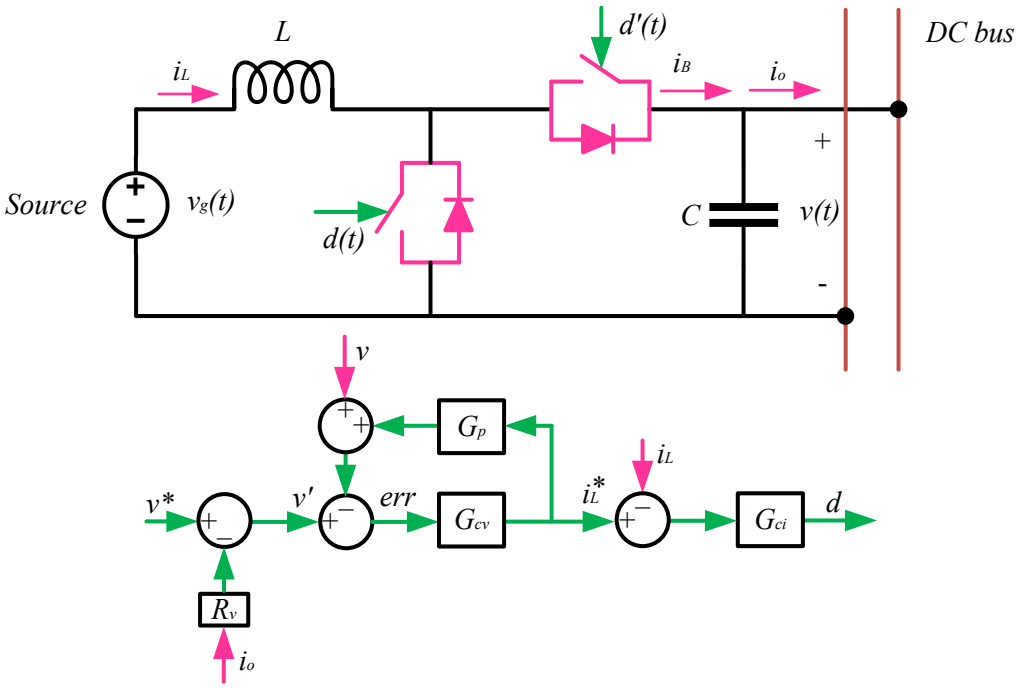


Figure 6.6 Circuit diagram and control blocks for terminal admittance evaluations.

6.2.2 Source Side Output Admittance

The source side interface converter works as a voltage source. It is also worthwhile to investigate the terminal output admittance shaped by the proposed passive controller. The circuit diagram and control blocks of the interface converter are shown in Figure 6.6.

Similarly, applying small signal analysis, the following equations can be attained based on the circuit diagram.

$$\Delta i_L(s) = \frac{\bar{V} \cdot \Delta d(s)}{sL} - \frac{(1-D) \cdot \Delta v(s)}{sL} \tag{6-9}$$

$$\Delta i_B = \Delta i_L \cdot (1-D) - \Delta d(s) \cdot \bar{I_L} \tag{6-10}$$

$$\Delta i_o(s) = \Delta i_B - sC \cdot \Delta v(s) \tag{6-11}$$

If voltage reference v^* is assumed to be constant, based on the above control blocks in Figure 6.6, the following equations can be attained.

$$\Delta i_L^* = (-\Delta i_B R_v - \Delta v - G_p \cdot \Delta i_L^*) \cdot G_{cv} \tag{6-12}$$

$$\Delta d(s) = (\Delta i_L^* - \Delta i_L) \cdot G_{ci} \tag{6-13}$$

The above equations are sorted and assigned to the signal flow chart in Figure 6.7.

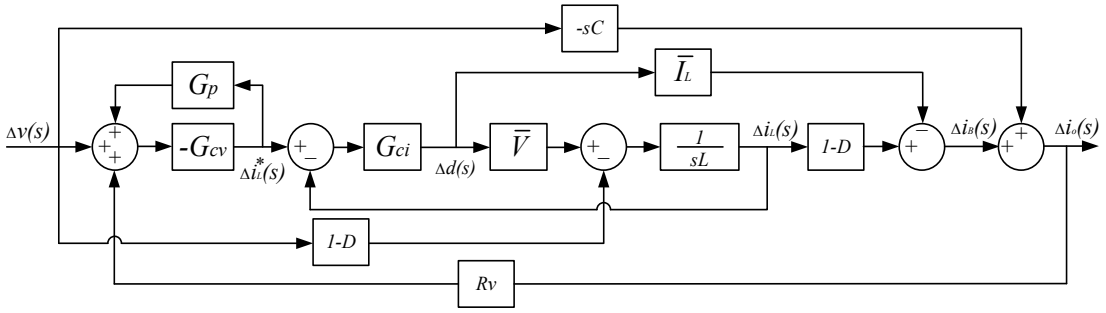


Figure 6.7 Signal flow chart of terminal admittance.

Again, by applying MGF and calculations (detailed calculations can be found in Appendix A5), the terminal admittance can be attained in equation (6-14),

$$Y_T^{P\&D} = -\frac{\Delta i_o(s)}{\Delta v(s)}$$
$$= \frac{G_{cv}G_{ci}\bar{V}(1-D) + (1-D)^2\left(1+G_pG_{cv}\right) - (sL)G_{cv}G_{ci}\bar{I_L} + (1-D)G_{ci}\bar{I_L}\left(1+G_pG_{cv}\right)}{(sL) + G_{ci}\bar{V} + G_{cv}G_{ci}\bar{V}(1-D)R_v - (sL)G_{cv}G_{ci}\bar{I_L}R_v + G_pG_{cv}(sL) + G_{ci}\bar{V}G_pG_{cv}}$$
$$+ \frac{sC\left((sL) + G_{ci}\bar{V} + (sL)G_pG_{cv} + G_pG_{cv}G_{ci}\bar{V}\right)}{(sL) + G_{ci}\bar{V} + G_{cv}G_{ci}\bar{V}(1-D)R_v - (sL)G_{cv}G_{ci}\bar{I_L}R_v + G_pG_{cv}(sL) + G_{ci}\bar{V}G_pG_{cv}}$$

(6-14)

If let $R_v = 0$, the terminal admittance without droop control can be written in equation (6-15),

$$Y_T^{P} = -\frac{\Delta i_o(s)}{\Delta v(s)}$$
$$= \frac{G_{cv}G_{ci}\bar{V}(1-D) + (1-D)^2\left(1+G_pG_{cv}\right) - (sL)G_{cv}G_{ci}\bar{I_L} + (1-D)G_{ci}\bar{I_L}\left(1+G_pG_{cv}\right)}{(sL) + G_{ci}\bar{V} + G_pG_{cv}(sL) + G_{ci}\bar{V}G_pG_{cv}}$$
$$+ \frac{sC\left((sL) + G_{ci}\bar{V} + (sL)G_pG_{cv} + G_pG_{cv}G_{ci}\bar{V}\right)}{(sL) + G_{ci}\bar{V} + G_pG_{cv}(sL) + G_{ci}\bar{V}G_pG_{cv}}$$

(6-15)

If let $K = 0$, the terminal admittance without a passive stabiliser can be written in equation (6-16).

$$Y_T^{D} = -\frac{\Delta i_o(s)}{\Delta v(s)} = \frac{G_{cv}G_{ci}\bar{V}(1-D) + (1-D)^2 - (sL)G_{cv}G_{ci}\bar{I_L} + (1-D)G_{ci}\bar{I_L}}{(sL) + G_{ci}\bar{V} + G_{cv}G_{ci}\bar{V}(1-D)R_v - (sL)G_{cv}G_{ci}\bar{I_L}R_v}$$
$$+ \frac{sC\left((sL) + G_{ci}\bar{V}\right)}{(sL) + G_{ci}\bar{V} + G_{cv}G_{ci}\bar{V}(1-D)R_v - (sL)G_{cv}G_{ci}\bar{I_L}R_v}$$

(6-16)

If let $R_v = 0$ and $K = 0$, the terminal admittance of initial double loop control can be written in equation (6-17).

$$Y_T^{dbl} = -\frac{\Delta i_o(s)}{\Delta v(s)}$$
$$= \frac{G_{cv}G_{ci}\bar{V}(1-D) + (1-D)^2 - (sL)G_{cv}G_{ci}\bar{I_L} + (1-D)G_{ci}\bar{I_L} + sC\left((sL) + G_{ci}\bar{V}\right)}{(sL) + G_{ci}\bar{V}}$$

(6-17)

First of all, by replacing G_{cv}, G_{ci} and G_p with the equations (5-35), (5-36) and (5-37), neglecting the high frequency pole contained in G_{ci} for calculation convenience, and let $s \to 0$, the terminal admittance can thus be attained,

$$Y_T^{dbl} \to \frac{G_{vm}(\omega_{zv})G_{im}(\omega_z)\bar{V}(1-D)}{0} \to +\infty \tag{6-18}$$

This result explains the terminal impedance characteristic (where $Z_T^{dbl} \to 0$) of tightly regulated converters discussed in Chapter 2, section 2.1.3. Therefore, droop control is required if two converters are connected in parallel.

Secondly, when applying the proposed passive stabilisers, the low frequency admittance approximation is shown as follows,

$$s \to 0, Y_T^{HPF-K} \to \frac{G_{vm}(\omega_{zv})G_{im}(\omega_z)\bar{V}(1-D)}{0} \to +\infty \tag{6-19}$$

The result shows that the HPF-K passive stabiliser does not change the low frequency terminal admittance, which is as predicted.

Thirdly, when the droop control is introduced in the outer controllers, the terminal admittance is shaped by the virtual resistance, as shown in equation (6-20).

$$s \to 0, Y_T^{D} \to \frac{G_{vm}(\omega_{zv})G_{im}(\omega_z)\bar{V}(1-D)}{G_{vm}(\omega_{zv})G_{im}(\omega_z)\bar{V}(1-D)R_v} = \frac{1}{R_v} \tag{6-20}$$

This result coincides with the previous analysis of the equivalent circuit model of droop control in Chapter 2. Similarly, the terminal admittance approximation of the intact controller is shown in equation (6-21),

$$s \to 0, Y_T^{P\&D} \to \frac{G_{vm}(\omega_{zv})G_{im}(\omega_z)\bar{V}(1-D)}{G_{vm}(\omega_{zv})G_{im}(\omega_z)\bar{V}(1-D)R_v} = \frac{1}{R_v} \tag{6-21}$$

The proposed passive controller does not change the previous low frequency approximation. Drawing the above terminal admittance, the results are shown in Figure 6.8. One interesting thing is that the proposed passive controller decreases the terminal admittance. Based on impedance

inequality analysis, increased terminal impedance is undesirable for cascaded converters (or constant power load). There is also a possible trade-off between compensating the non-minimum phase and regulating constant power load. However, with droop control, this will not be an issue because the virtual resistance will dominate the low frequency impedance.

The minor loop gain of these two interface converter interactions is drawn in Figure 6.9. Based on the theorem discussed in Chapter 2, the system is stable. Therefore, the solutions for stabilising DC microgrids in this case can be concluded as follows:

- The total source power in the system is designed to be larger than the load power;
- When the above condition is not satisfied, load shedding or decreasing the total load power is necessary;
- Within the power capacity, adding the passive resistor can help stabilise the system;
- Adding the terminal capacitor or increasing the passive gain can help stabilise the system.

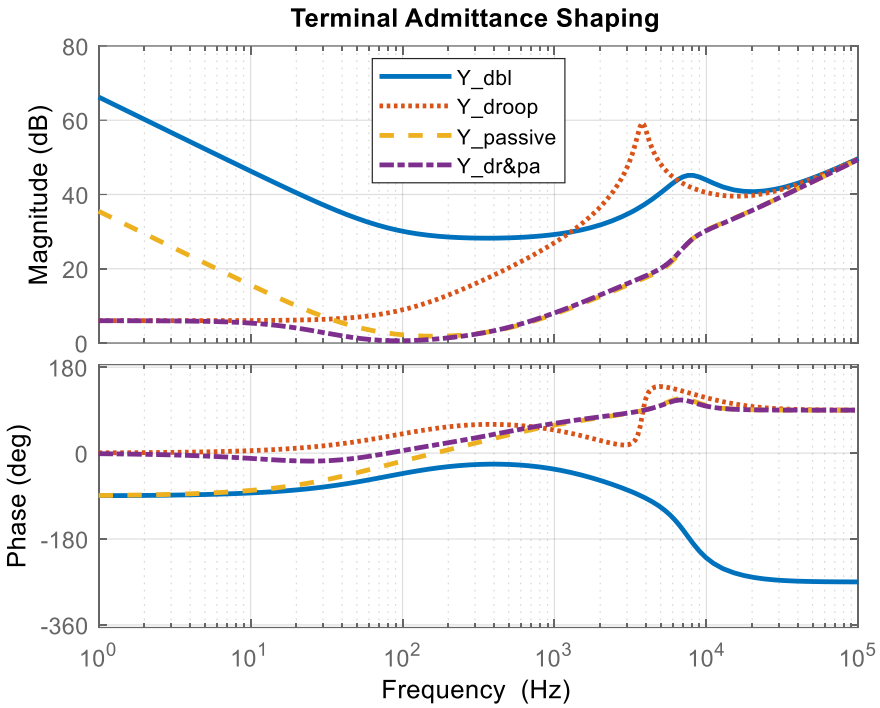


Figure 6.8 Terminal admittance shaping of interface converter by passive stabilisers.

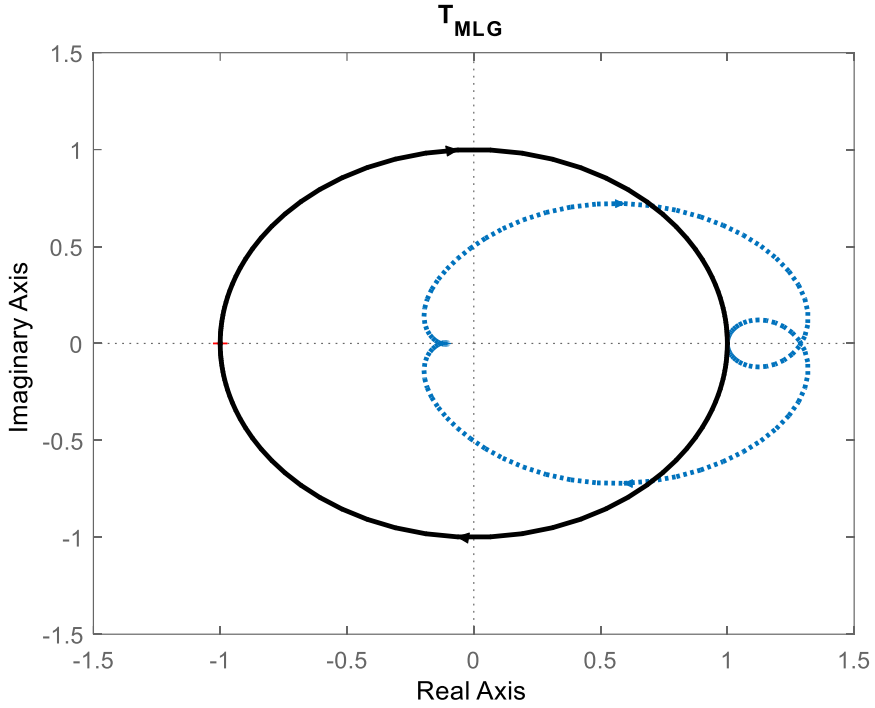


Figure 6.9 Minor loop gain of passive controller with CPL.

6.3 Signal Series Interpretations

The signal series can be designed according to the user's requirements. In this Chapter, a DC microgrid house application is used as an example to show the effectiveness of a hierarchical control scheme with the proposed DBI method. The DC microgrid house involves two operation modes: on-grid mode and island (off-grid) mode. When the system is grid-connected, it is desired that the energy storage devices are charged in the off-grid situation. When the system is operated in island mode, the power balance needs to be well considered. Based on the requirements, rules on this application are made here. One important point is that the following rule-based method is based on the author's best knowledge and experience but may not optimal. This is not the only way to regulate the DC microgrids. Optimisation of system operation is beyond the scope of this thesis.

The first part is for on-grid operation; the operation rules are listed below.

- The energy storage devices connected with the DC microgrid only absorb power from the grid;
- If multiple energy storage devices are involved, the system will supply power to the first connected module; and a dedicated delay is needed to avoid the mutual disturbance between each module;
- If the PV generation power has surplus power, it will be supplied to the grid.

The second part is for off-grid operation. A seamless switch between on-grid and off-grid operation is required. In off-grid operation, the operation rules are listed below.

- The assigned Interface Converter (IC) that maintains the DC bus voltage has the right to switch ON other sources connected in the DC microgrid to supply the load with a higher priority;
- The assigned IC that maintains the bus voltage has a higher priority to absorb power from the DC microgrid if the PV has additional power;

- If all the energy storage devices are fully charged, PV will work in the power limitation mode to maintain the system power balance;

Based on the above operation rules, the signal series is designed with six bits. The specific functions of each bit are listed and explained in Table 6-1.

Table 6-1 Signal series design with six bits.

Bits	Example	Full meanings
1	1	Start signal, indicates the signalling start.
2	1	1: ON, 0: OFF, indicates the IC state.
3	0	0: IC2, 1: IC3, indicates the number of IC.
4	1	1: droop mode, 0: power mode, indicates the IC's working mode.
5	0	1: discharge, 0: charge, indicates the IC's working state.
6	0	0: 1A, 1: 2A, indicates the IC's current amplitudes for charging or discharging.

Signal series have different meanings if they are sent by different ICs. The explanations of all possible signal combinations are given in Appendix A6.

The above designed signal series can be applied to regulate the DC bus voltage for signalling. The floating voltage v_T^* in this section is chosen as 50V, and the signalling voltage v_S is chosen as 52.5V, which is 1.05PU as discussed in Chapter 4. The pulse width T_s is chosen as 100ms. Therefore, an intact signal example can be shown in Figure 6.10. In this example, the signal series is 110100, which means that IC2 is on and operates in droop mode.

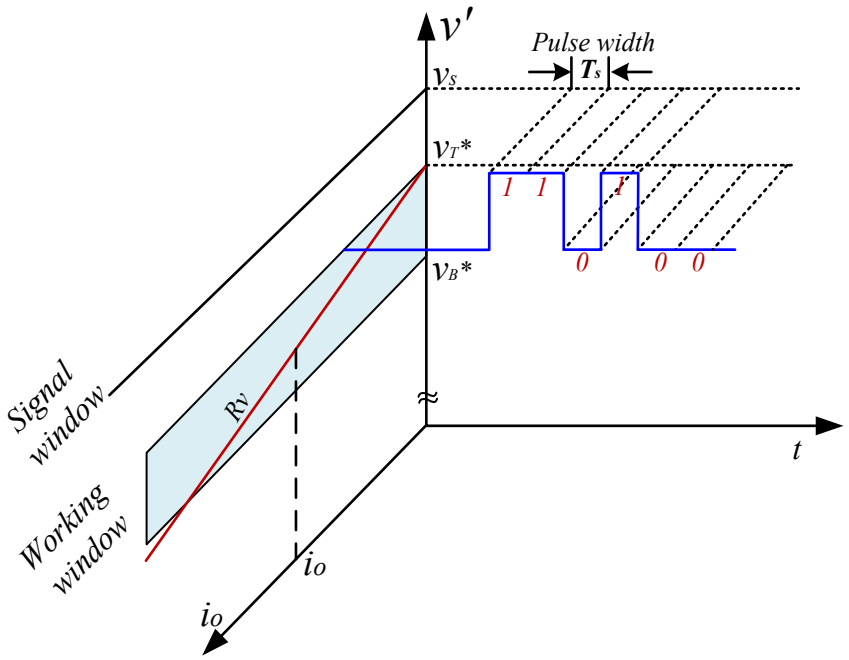


Figure 6.10 Signal series sample in 3-D plot.

During the signalling period, the DC bus voltage will be regulated as the designed signal series shown in Figure 6.10 to achieve signalling. It must be mentioned that a longer signal series can have more information available, yet the interaction period will take more time as a trade-off.

6.4 Algorithms and State Machine

The system operation algorithm is implemented in a digital signal processor (DSP). The controller design has been discussed in Chapter 4 and Chapter 5. As for the PV generations, the power limitation in the off-grid mode needs to be applied. The switch between system operation modes is realised by a designed state machine.

6.4.1 PV Power Limitation Algorithm

When the system works under off-grid mode, the surplus power in PV generations may cause a power imbalance in the system. Therefore, the surplus power needs to be limited when the energy storage is fully charged. Based on the power-voltage (P-V) curves shown in Figure 6.11,

there are two possible operating points lower than the maximum power point. The discussion of the pros and cons of the two operating points is provided in reference [154]. Therefore, the predicted PV tracking curve is the blue solid line as shown in Figure 6.11.

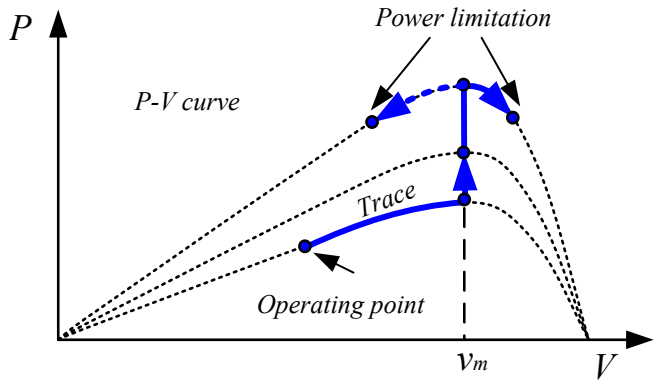


Figure 6.11 PV predicted tracking curve of power limitation.

The MPPT algorithm used here is a standard perturbation and observation (P&O) method. The MPPT algorithm is not the main focus of this thesis. There are many other MPPT algorithms that can be found in the literature, such as reference [155]. The droop control in a DC microgrid makes the system exhibit a similar behaviour to that of batteries, which means that when the system is load-dominant, the DC bus voltage will drop down. In contrast, when the system is source-dominant, the DC bus voltage will increase. This is shown in Figure 6.12.

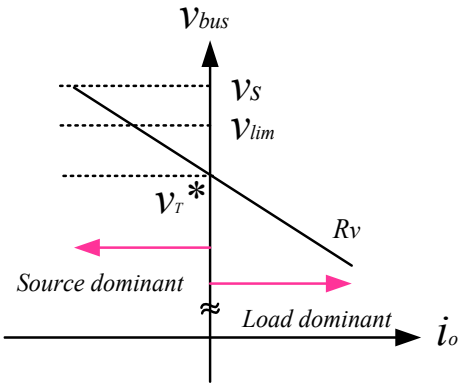


Figure 6.12 Battery characteristics of DC microgrids with droop control.

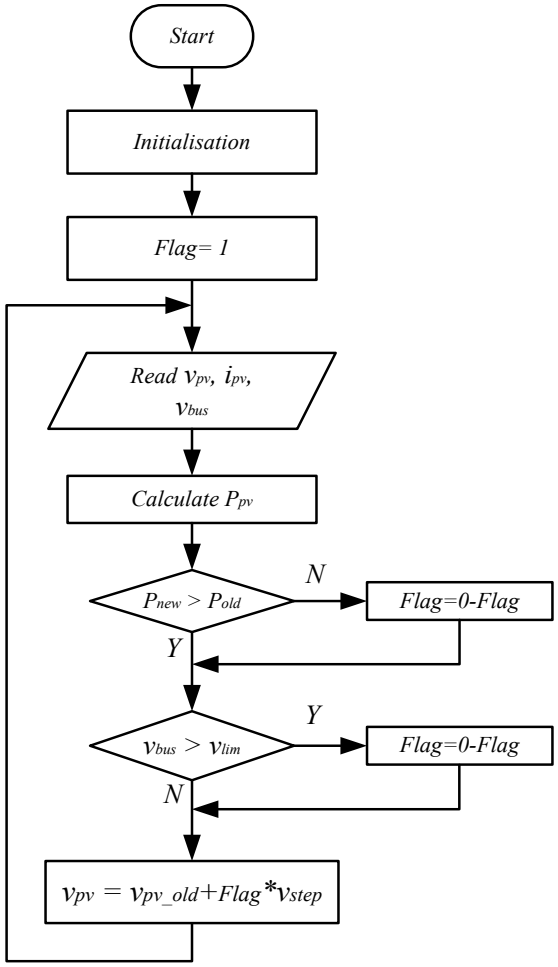


Figure 6.13 Flow chart of algorithm for PV surplus power limitation.

When the PV generation is higher than the load consumption, it will start to inject power into the battery banks. The bus voltage thus will be raised. In the general case, if other energy storage devices can absorb the surplus power, they will be switched on for charging. When all energy storage devices in the system are fully charged, the surplus power will continue to raise the DC bus voltage until it reaches the voltage limit v_{lim} as is shown in Figure 6.12. Then, the operating point from the PV curves will move away from the maximum power point, and the PV generation is limited. The flow chart of PV power limitation algorithm is shown in Figure 6.13.

6.4.2 System State Machine

The system state machine contains two levels. The first level is for signal series sending and receiving, which is shown in Figure 6.14.

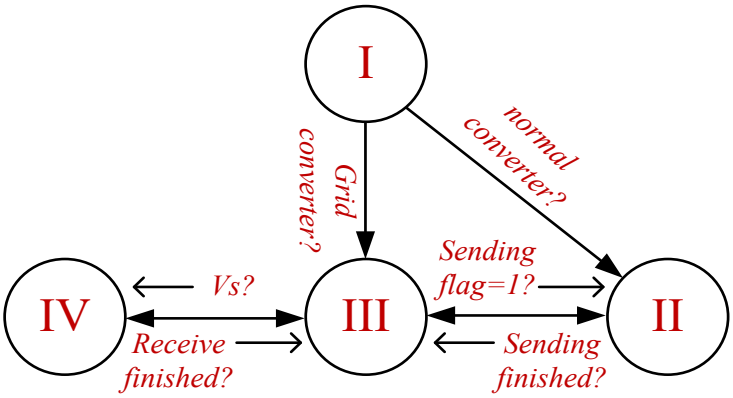


Figure 6.14 State machine of signal series sending and receiving.

- State I: this state mainly includes the initializations. The functions of the converter need to be determined by the users. If this converter is operated as a grid-connected converter, then it will not need to send signals and will directly step into state III. If the converter is operated as a normal converter, it will step into state II for signal series sending.
- State II: this state is responsible for the signal sending. After finishing sending the signal series, it will step into state III. The signal series may come from state III or state I.
- State III: this state is the centre of the state machine. In this state, the controller always monitors the common DC bus voltage, and determines if any signal voltage comes through. This state also contains the second level state machines for the transfer between sleep mode, droop mode and power mode. When the signal voltage arrives, it will trigger the receiving algorithm in state IV. In addition, it will react to the load situations and automatically or manually trigger the sending algorithm in state II to switch on other sources in DC microgrids for charging/discharging operations.
- State IV: this state is responsible for signal receiving. After the signal series is received, it will step into state III. Meanwhile, when the interface converter steps into this state, it will work with current compensation as discussed in Chapter 4 because the bus voltage will be regulated by other interface converters connected in the DC microgrid.

The second level state machine is included in state III in the first level. At this level, it mainly deals with the mode switch between sleep mode, droop mode and power mode according to the signal series attained at the first level. The state machine is shown in Figure 6.15.

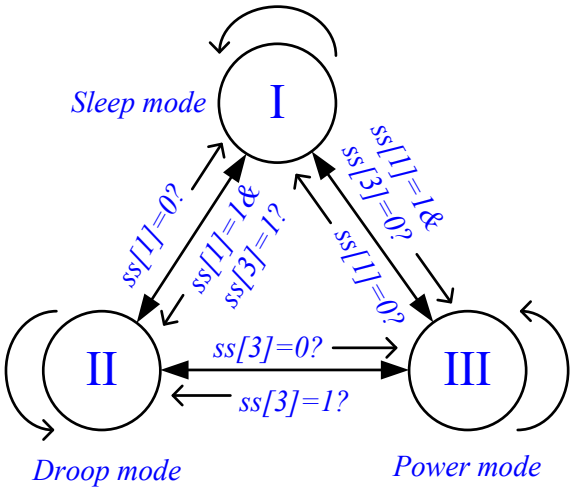


Figure 6.15 State machine switches of different working modes.

- State I: in this state, the interface converter works under sleep mode, monitoring the DC bus voltage and waiting for the potential signal series from other interface converters. All of the converters except the grid converter will firstly step into this mode. Once the received signal with the indication that they need to work in droop mode or power mode, they will enter the respective working mode.
- State II: in this state, the interface converter works under droop control mode. The grid converter will firstly step into this mode. As for other converters working under this mode, they will have their own regulatory functions such as surplus power limitations from PV generations.
- State III: in this state, the interface converter will work under power control mode. The reference current in the control loop is determined by the signal series and it interacts with battery's SoC. When the battery is fully charged, it will go to sleep in state I.

The system operates under the above proposed hierarchical control scheme with designed algorithms and state machine. Plug and play performance of DC microgrids can be achieved within this control scheme.

6.5 Experimental Validations

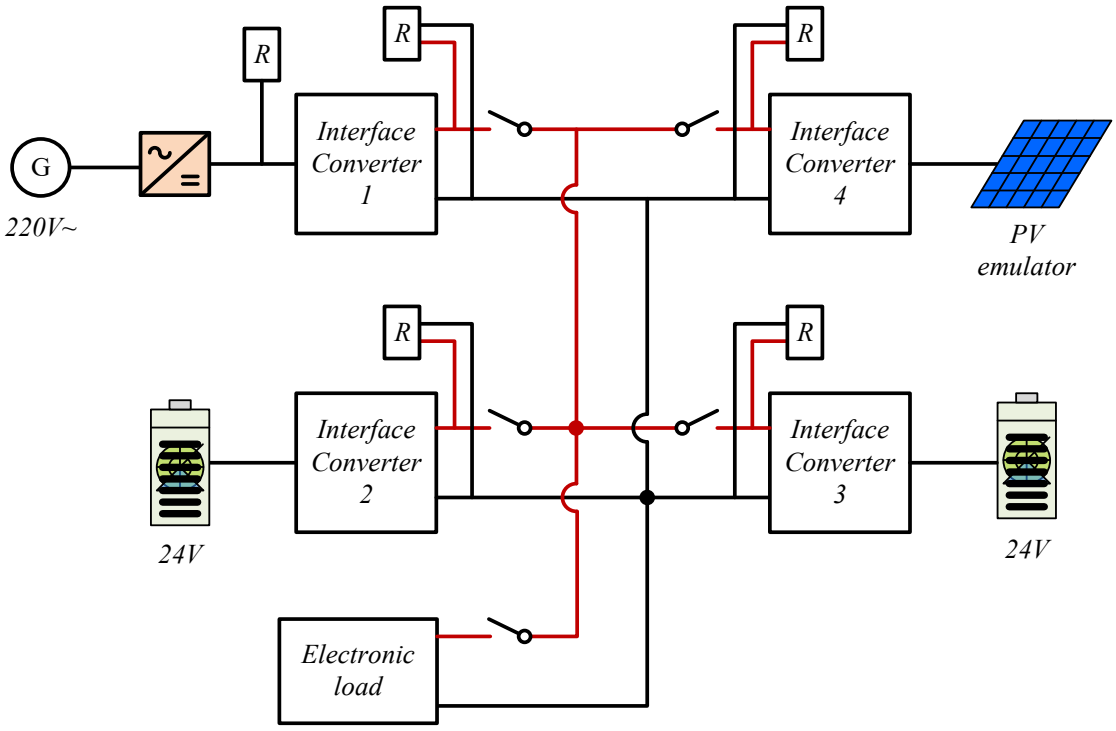


Figure 6.16 Configuration of experimental setup .

The parameters and their values used in the experiment are listed in Table 6-2.

Table 6-2 Data of experimental setup for plug and play operation.

Parameters/equipment	Values/types
Equipment	
PV emulators	62050H-660S
Battery banks	Valve regulated lead acid type rechargeable battery, 12V 24/33Ah.
DC electronic load	EA-EL 2400-25, 400W
Resistance load (R)	10Ω/220Ω/100Ω, etc.
Signal series and control	
v_S	52.5V
v_T^*	50V
v_{lim}	51V
T_s	100ms

The experiment contains two parts: on-grid operation and off-grid operation. In on-grid mode, the DC bus voltage is maintained by the grid-connected interface converter. In off-grid mode, the DC bus voltage is maintained by the assigned interface converter with battery banks, which is interface converter 2 in this case. The configuration of experimental setup is shown in Figure 6.16.

6.5.1 On-grid operations

For on-grid operation, the grid interface converter will maintain the DC bus voltage using droop control. Figure 6.17 shows the experimental results of on-grid operations. Firstly, the DC bus voltage is regulated by IC1, then IC2 is plugged in. IC2 starts to interact with IC1 and regulates the bus voltage with signal series 110000, which indicates that IC2 is on and needs to absorb the power from the DC microgrid with a charging current of 1A. After a 2 second information process, IC1, which dominates the bus voltage, will send the signal back to switch on IC2 with a charging current of 1A. While the charging process is long in real applications, in this study, the charging process is shortened to 10 seconds via an internal time counter. When IC2 is fully charged, it will send the signal to IC1, and then it will go into sleep mode and be ready for the discharging process.

When the energy storage devices in the system are fully charged, the PV generations have additional power from supplying the load, and the additional power is then sent back to the grid. The experimental result is shown in Figure 6.18. The dynamic MPPT test is also applied in this figure. The PV generation steps up firstly and then step down. The DBI signalling can still be achieved during the step-down period, which also shows the effectiveness of the proposed control strategies.

If there are multiple energy storage devices connected in the DC microgrid, which is shown in Figure 6.19, a period of delay is required before the next IC is plugged in to give enough time for IC1 to process the information. If the IC to be plugged in is in a fully charged state, it will remain in sleep mode. In this figure, IC3 interacts with IC1 and regulates the bus voltage with

signal series 111010, which means that IC3 is ready for discharge and there is no need to absorb power from the DC microgrid.

If both energy storage devices are at low SoC and need to absorb power from the grid, then IC1 will switch on IC2 first because it was plugged into the DC microgrid earlier than IC3. When IC3 is plugged in, it will be switched on as well to absorb power from the microgrid. The experimental results for this case is shown in Figure 6.20.

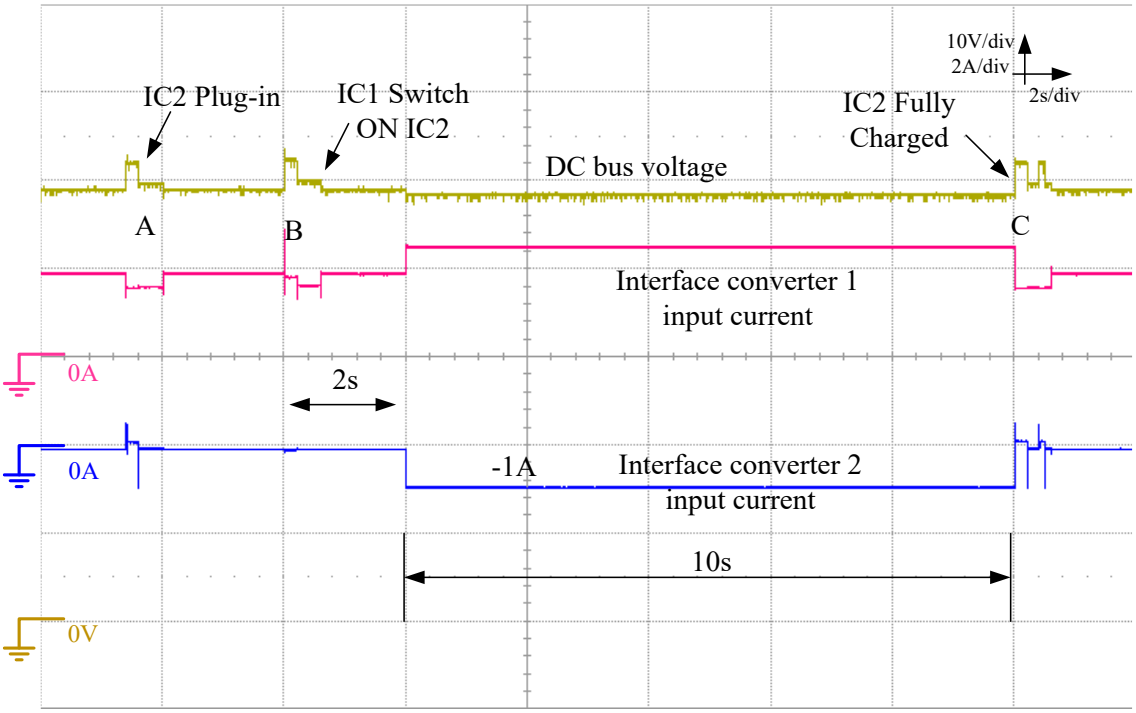


Figure 6.17 System operation under on-grid mode; IC2 is plugged in at low power capacity and then IC1 switches on IC2 to absorb power from the DC microgrid with a charging current of 1A.

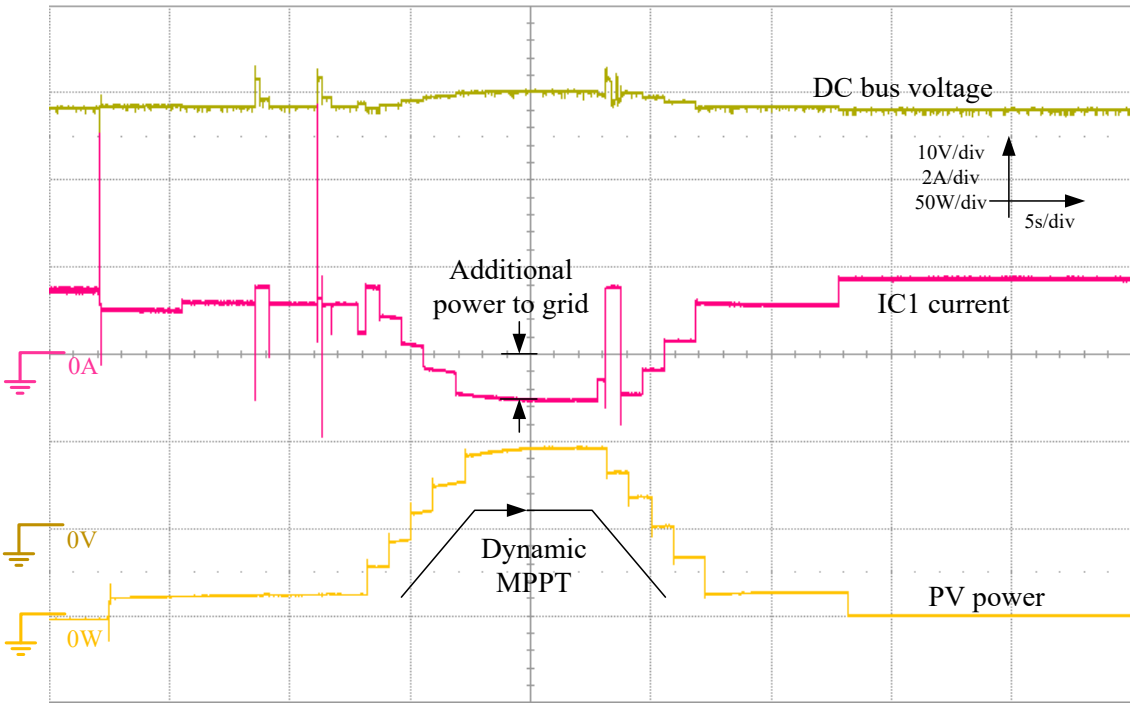


Figure 6.18 System operation under on-grid mode; IC2 is plugged in at full power capacity and the additional power from the PV generations will be supplied to the grid.

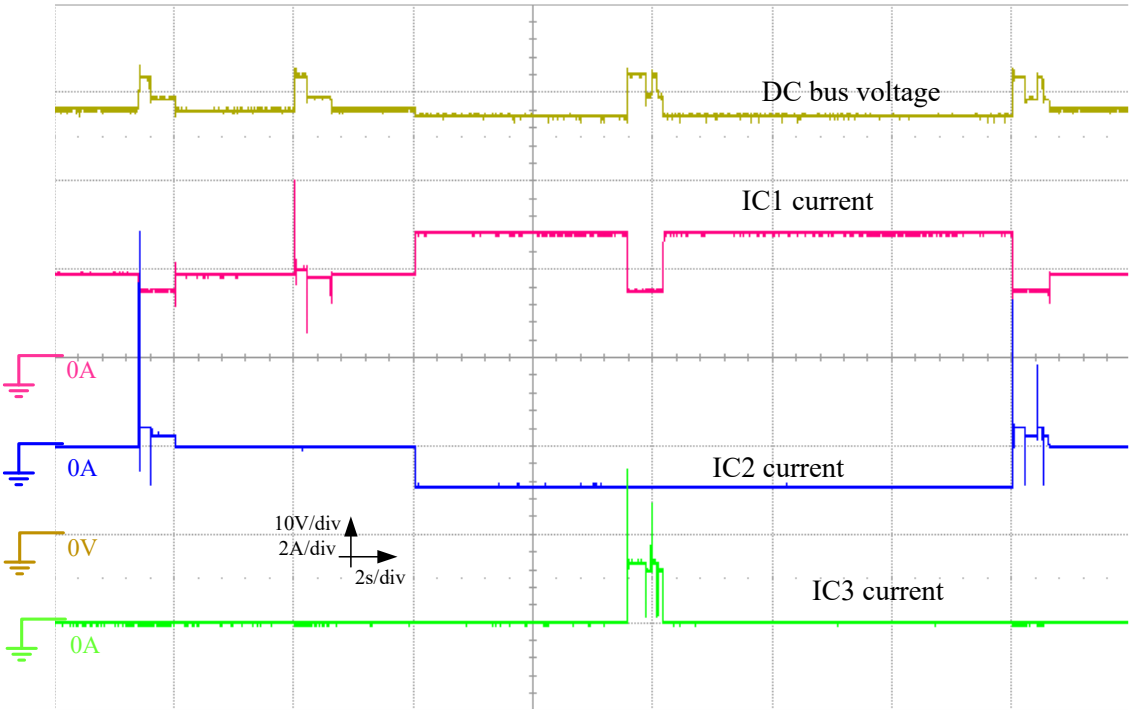


Figure 6.19 System operation under on-grid mode; IC2 is plugged in at low power capacity and then IC1 switches on IC2 to absorb power from the DC microgrid with a charging current of 1A; IC3 is plugged in at full power capacity and is ready for discharging.

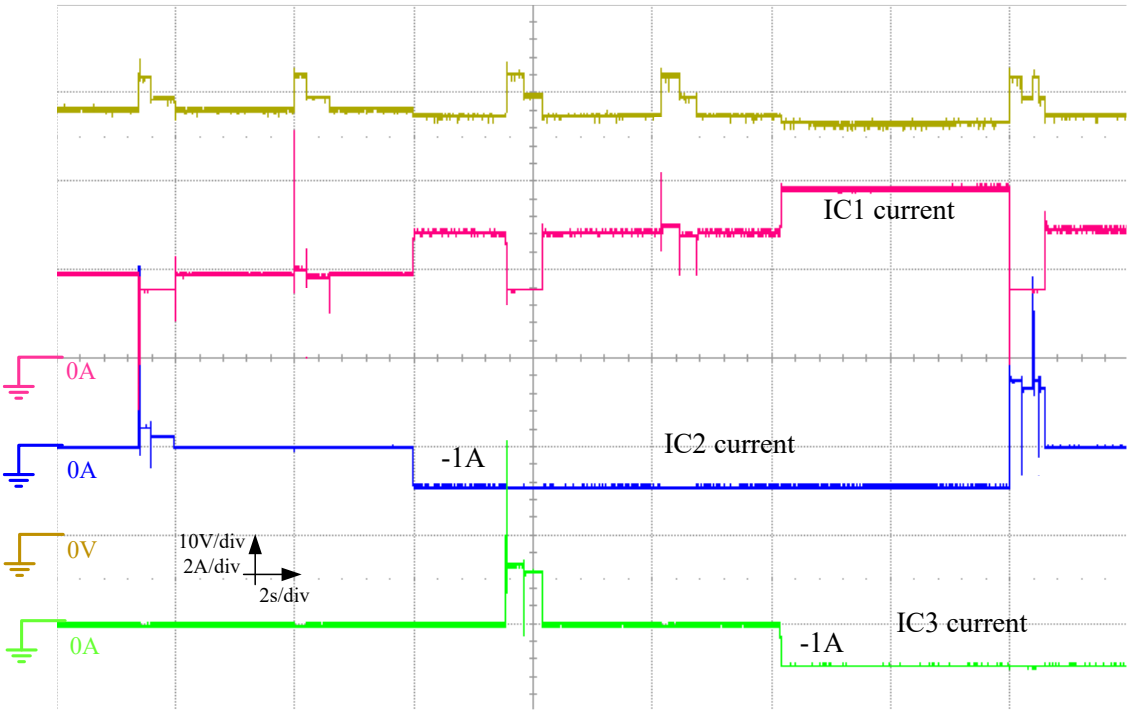


Figure 6.20 System operation under on-grid mode; IC2 is plugged in at low power capacity and then IC1 switches on IC2 to absorb power from the DC microgrid with a charging current of 1A; IC3 is plugged in at low power capacity and then IC1 switches on IC3 to absorb power from the DC microgrid with a charging current of 1A.

The DC bus voltage is maintained by the grid interface converter when the system is operated in on-grid mode. When the system works under off-grid mode, at least one converter in the DC microgrid will be used to maintain the DC bus voltage. PV generation needs to work in MPPT mode to maximize power output, and it is not the best option to regulate the DC bus due to the fast-changing external environment, such as temperature and irradiance. Therefore, in this experiment, one battery bank is chosen to maintain the DC bus voltage when the grid interface converter is switched off.

When the grid interface converter is going to be switched off, one off-signal is required to inform the other converters in the system to maintain the bus voltage. This means that the system cannot regulate the power actively when the grid interface converter is broken or plugged out abruptly, which is one of limitations of the proposed method. Without active signalling, the rest of the interface converters are either all off and the system is restarted, or all will work under droop control and share power equally.

The seamless transfer from on-grid mode to off-grid mode is shown in Figure 6.21. IC2 (with battery source) is connected in the DC microgrid. The signal series is 110010, which indicates it is fully charged and ready for discharging or maintaining the DC bus voltage. Before the grid interface converter is plugged out, it sends signal series 110110 to assign the IC2 as the dominant converter to maintain the DC bus voltage. Once receiving this signal, IC2 starts to regulate the DC bus voltage under droop control, which is exactly the same as the grid interface converter. Therefore, the average current sharing is shown in this figure. During this period, the grid interface converter can be mechanically plugged out at any time.

Another similar issue which is worth discussing is that when the grid interface converter is connected again, it will send the signal to IC2 to work in power mode and regain control over the DC bus voltage. The seamless transfer is achieved through droop control, which is shown in Figure 6.22. IC2 will step into charging mode according to its SoC to compensate for the power loss in the off-grid mode. When it is fully charged, it will do the same thing, as shown in Figure 6.17.

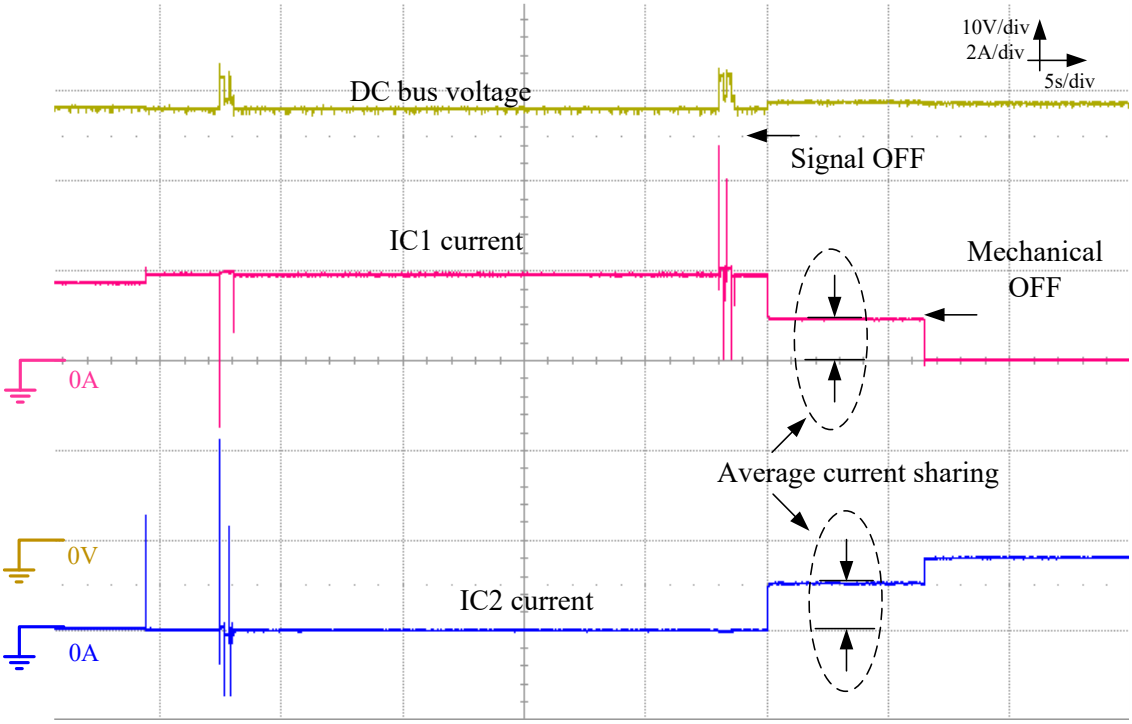


Figure 6.21 Seamless alternation from on-grid mode to off-grid mode.

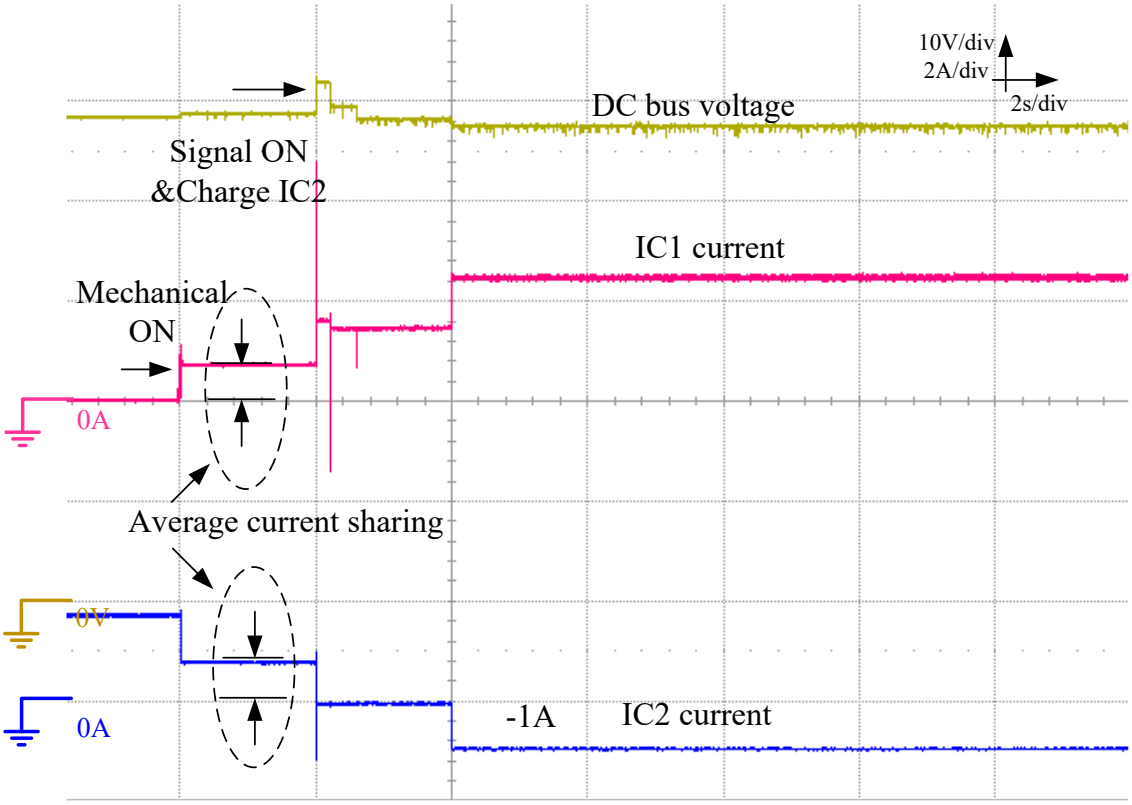


Figure 6.22 Seamless alternation from off-grid mode to on-grid mode.

6.5.2 Off-grid operations

When the system works under off-grid mode, the situation will be different. The surplus PV power needs to be considered in this case. In this section, the surplus power from PV generations will be limited through the proposed modified MPPT algorithm.

Figure 6.23 shows IC3 plugged in, with the power to supply the load, and then IC2 switches on IC3 and makes IC3 supply the load first. In some cases, if the load is heavy, IC2 could also switch on IC3 with a discharging current of 2A to supply the load, which is shown in Figure 6.24. Meanwhile a dynamic load test is also shown in Figure 6.24. The operation of dynamic load can be viewed from IC2's current. Compared with Figure 6.23, the load power in Figure 6.24 is larger than that in Figure 6.23. Therefore, 2A discharging current is applied in this case. Similarly, a dynamic load test further shows the effectiveness of proposed control strategies.

If the system has additional PV power, the additional power will be supplied to batteries via IC2 first according to the operation rules. When it is at full SoC state, it will switch on IC3 to absorb power from the DC microgrid. The experimental result is shown in Figure 6.25.

The final case is when all the energy storage devices are at full SoC state, and PV generation is still higher than the total load consumption. Based on the operation rules, the surplus PV power will be limited as shown in Figure 6.26. In this case, the PV generations will no longer work in maximum power point tracking mode, and the operating point will move to either the left side or the right side arbitrarily to reduce the PV generation. In this case, it moves to the right-side operating point.

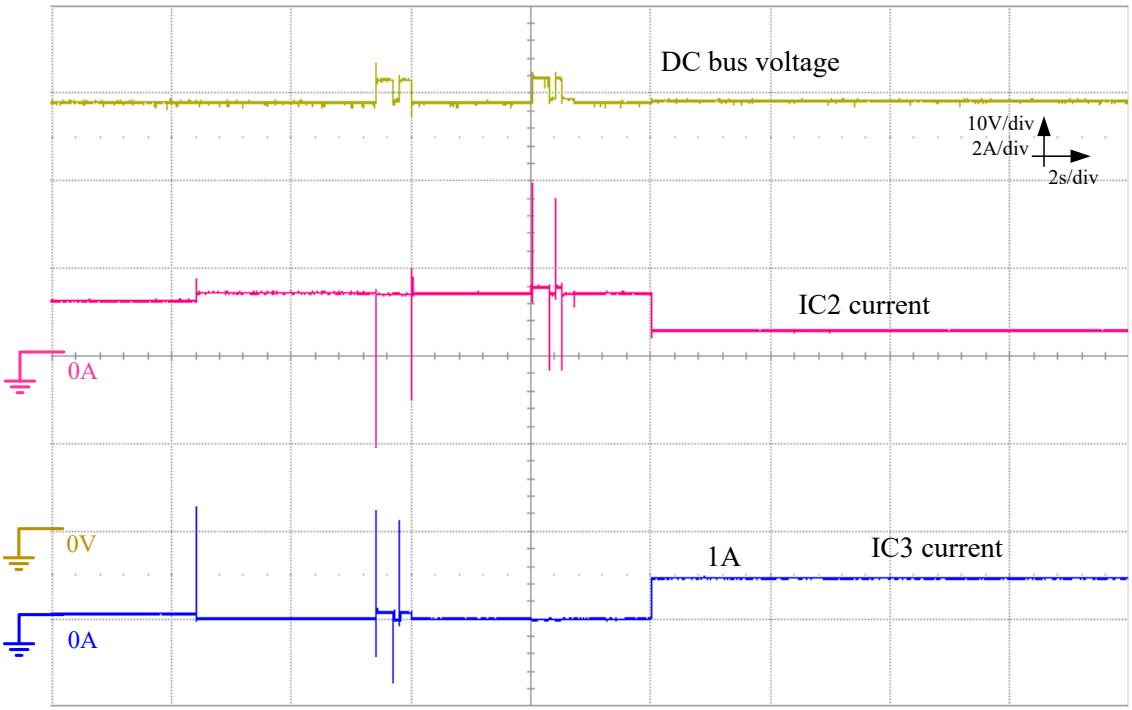


Figure 6.23 System operation under off-grid mode; IC3 is plugged in and is able to supply the power to the DC microgrid, then IC2 switches on IC3 and supplies the load with 1A due to the light load.

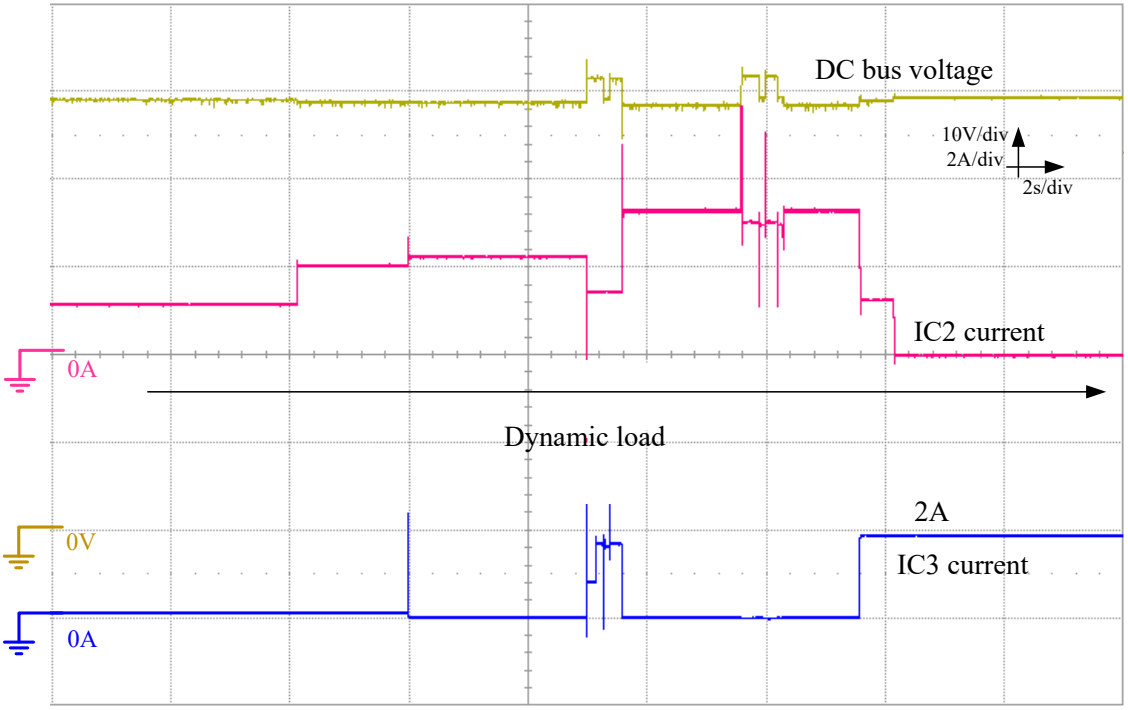


Figure 6.24 System operation under off-grid mode; IC3 is plugged in and is able to supply the power to the DC microgrid, then IC2 switches on IC3 with 2A due to the dynamically instant heavy load.

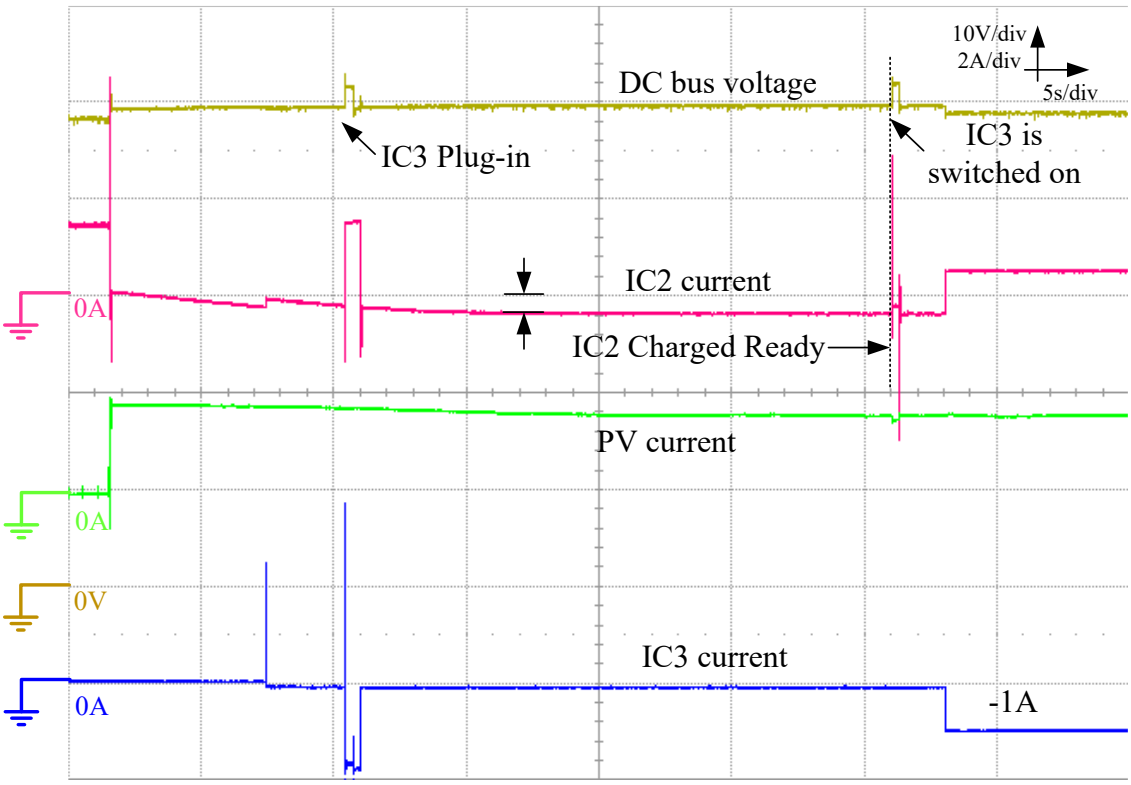


Figure 6.25 System operation under off-grid mode; IC3 is plugged in and needs power from the DC microgrid, IC2 needs power as well; IC2 absorbs power first; when it is full, then IC2 switches on IC3 and absorbes power at 1A.

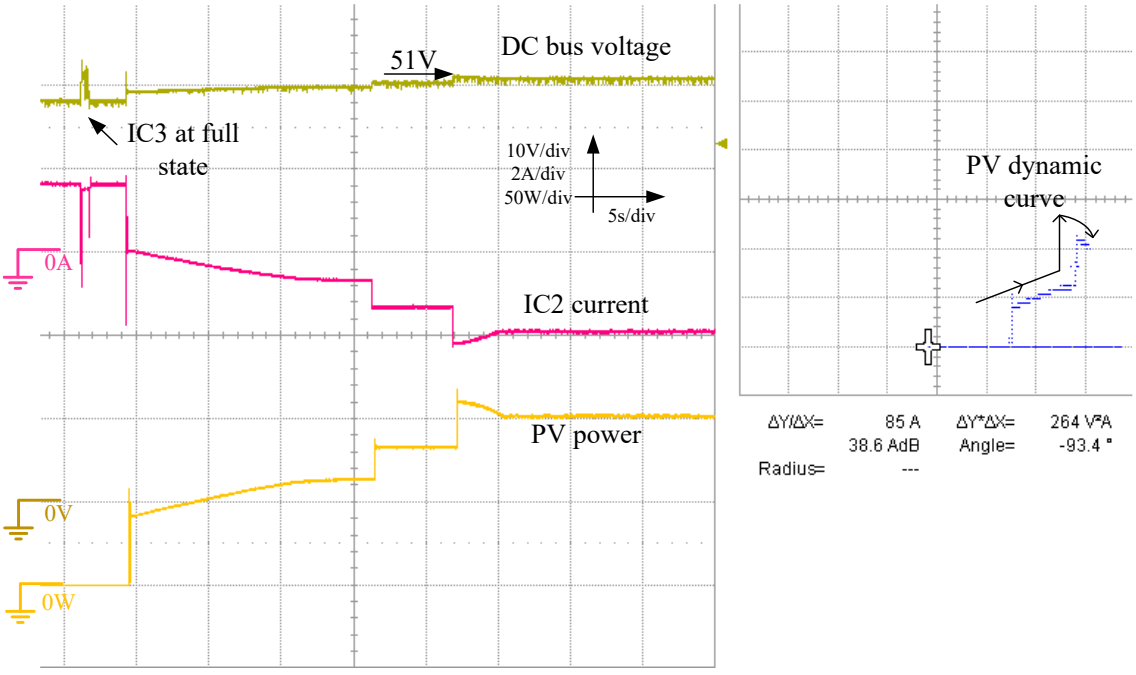


Figure 6.26 System operation under off-grid mode; IC3 is plugged in and at full SoC state, and IC2 is also nearly at full SoC, then the PV output power is limited and operating point moves to the right side.

6.6 Conclusions

This Chapter presents the design of a novel hierarchical control scheme for a DC microgrid in home applications. The control methods proposed in chapter 4 and chapter 5 are applied in this hierarchical control scheme. Based on the system control configurations, terminal admittance models of all possible working modes are built. In addition, the system stability is evaluated by admittance-based minor loop gain analysis, which shows that the system is stable within all possible working modes. The DC microgrid system is operated with a finite state machine and plug and play performance is realised. The grid-connected mode and off-grid mode are experimentally operated. The seamless switch between on-grid and off-grid operation is also implemented. A modified MPPT algorithm is proposed for the power balance consideration when the system is operated in off-grid mode.

The main contributions of this Chapter are the following:

This chapter presents a novel hierarchical control scheme for a DC microgrid without communication infrastructure, while simple power management between the distributed sources can be realised. In addition, it provides terminal admittance models for battery charging/discharging modes and a voltage source with a proposed primary controller. It shows how the additional controllers shape the terminal admittance on the conventional double loop control step by step. It can be found that the proposed passive controller increases the output impedance (or decreases the output admittance), which is not beneficial for the cascaded converters. There is a trade-off between the regulating constant power load and compensating non-minimum phase. However, in real applications, this amount of impedance increase is totally acceptable. As for the power balance consideration, a modified MPPT algorithm is proposed to limit the surplus power for islanded DC microgrids. The power limitation algorithm is embedded within the MPPT algorithm, which simplifies the control design.

Chapter 7 Conclusions and Future Work

This Chapter concludes the work in this thesis. The connections of each Chapter are presented. The future work is prospected. Finally, the author's publications during the Ph.D. study are listed.

7.1 Conclusions

This thesis proposed a set of new control methods on a hierarchical control scheme for a low voltage DC microgrid. A simple power management without communication infrastructure is realised within this hierarchical control. To put it specifically,

1. It proposes a novel dual-window DC bus interacting method for the power distribution managements on distributed sources. With the proposed DBI methods, the DC microgrid system is able to achieve power coordination, no longer relying on the communication infrastructure. The proposed method also does not alter the structure of interface converter, and does not need additional circuits for signalling interpretations, so that the additional cost of communication infrastructure is saved.
2. It proposes a new passive stabiliser for the interface converters that contain non-minimum phase. The proposed passive controller compensates the negative part caused by the non-minimum phase, such that non-minimum phase will no longer impact the system stability. Therefore, the interface converter can be more stable under complex operation conditions in DC microgrids.

3. A novel hierarchical control scheme with the proposed DBI method is implemented and assessed for a typical household DC microgrid application. The terminal of admittance of each working mode in the system are modelled and evaluated, especially for the bidirectional power flow controls, such as battery banks. The seamless transfer between on-grid mode and off-grid mode may be achieved. The power balance management, especially at the off-grid mode, is solved by the proposed modified MPPT algorithms for PV generations.

All experimental validations are conducted by the designed low voltage DC microgrid experimental system. The contributions of each control methods are illustrated on the conclusion section of corresponding chapter.

Apart from that, the chapter of literature review also provides fruitful information on control strategies and stability studies in DC microgrids. Many concepts in DC microgrids are clearly stated, such as centralised and decentralised control. Different control methods are compared and categorised. Especially, the working principles of lower layer control are specifically illustrated. The instability factors in the DC microgrids are classified for a single DC bus microgrid. The stability criteria and stabilisation methods are reviewed and compared from this classification.

7.2 Future Work

The DC microgrid is a prosperous and developing research topic. There are still many interesting topics to be addressed in the future work.

Firstly, from the stability perspective, the DC microgrid system global model for stability is still very difficult to obtain. It needs to find new convincing way to evaluate the system stability, especially for a system with multiple DC microgrids or DC microgrid clusters. Current research on system stability analysis is based on impedance inequality. When facing the unknown and variant DC microgrid system, it makes this inequality less useful. Total system impedance evaluation is a conservative method even though the impedance graph can be attained by single

terminal small signal injection. The results attained by this evaluation is a sufficient condition for system stable operation. However, unnecessary passive element will be required to satisfy this condition. This no doubt adds to the running cost of and makes the system bulky. Therefore, an effective criterion to guide the DC system stability design and planning is necessary.

Secondly, from control perspective, this topic has many interesting researches on present literature, especially for the droop control. The future trend on this topic is foreseen to go on with droop control. Droop control is an easy method and can be manipulated or compatible to many other control methods. It is still the first option on the secondary control. Even though the current communications technology is very mature, the research on the non-communication-based control methods is still necessary. These methods can be very useful in case of the communications failure or cyber-attack. The non-communications layer will be in charge of the power regulation in case of losing the communication infrastructure, which adds immunity and reliability of DC microgrids. On the other hand, to line up with future smart grid, communication infrastructure is required. A paradigm and standard for the communication means and protocol are urgent to be set.

Thirdly, in the further smart grid configuration, DC microgrid will be one of the important power distribution structure. The optimal power dispatch will be a hot research. Compared with conventional utility dispatch, DC microgrids show their flexibility on this due to power electronics devices. Some of concepts are starting emerging, such as energy router. The optimisation in DC microgrids can mimic conventional AC system. The advantage on DC microgrid system is that it does not have reactive power, which make the system optimisation easier. The renewable energy models, such as PV, wind turbine, battery energy, etc., is required to be adjusted to DC microgrids optimisation. The objective functions can be minimising running cost, carbon emission, etc.

Based on the above analysis and the developed DC microgrid experimental bench, the future work can be investigated are as follows,

- Upgrading the energy storage system. Using mixed the battery and supercapacitors energy storage to respond different requirements of loads based on droop control;
- Adding the communication infrastructure to line up with smart grid.
- Modelling the renewable sources in DC microgrids dispatch, providing optimisation scheme based on the minimum running cost, and carbon emission;
- Investigating the optimisation on multiple DC microgrids, maximising the owner's profit.

7.3 Author's Publications

The author's publications related to this thesis are listed below.

IEEE Transactions:

[1]. F. Li, Z. Lin, Z. Qian and J. Wu, "A Dual-Window DC Bus Interacting Method for DC Microgrids Hierarchical Control Scheme," *IEEE Transactions on Sustainable Energy, early access*.

Conferences:

[2]. F. Li, Z. Lin, Z. Qian and J. Wu, "Active DC bus signaling control method for coordinating multiple energy storage devices in DC microgrid," 2017 IEEE Second International Conference on DC Microgrids (ICDCM), Nuremburg, 2017, pp. 221-226.

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[5]. F. Li, Z. Lin, J. Wu and A. Chen, " Terminal Capacitor Compensation Based Stability Design for DC Microgrids," 2019 IEEE Third International Conference on DC Microgrids (ICDCM), Matsue, 2019.

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Appendix

This appendix is the supplement of previous Chapters, it mainly incudes the system prototype and setup, equation manipulations and calculations.

A1. Design of Interface Converters

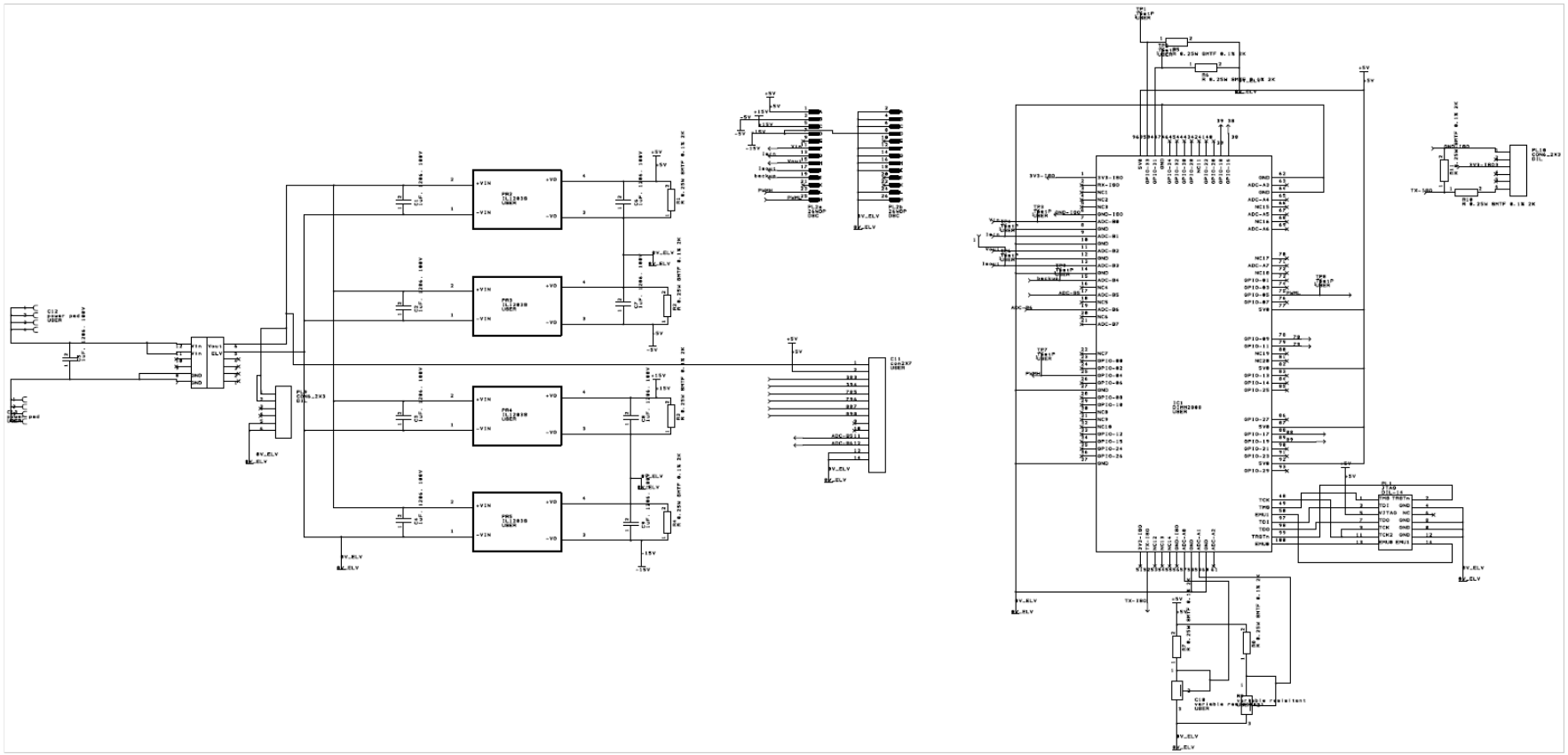

Figure A. 1 Schematic of control board.

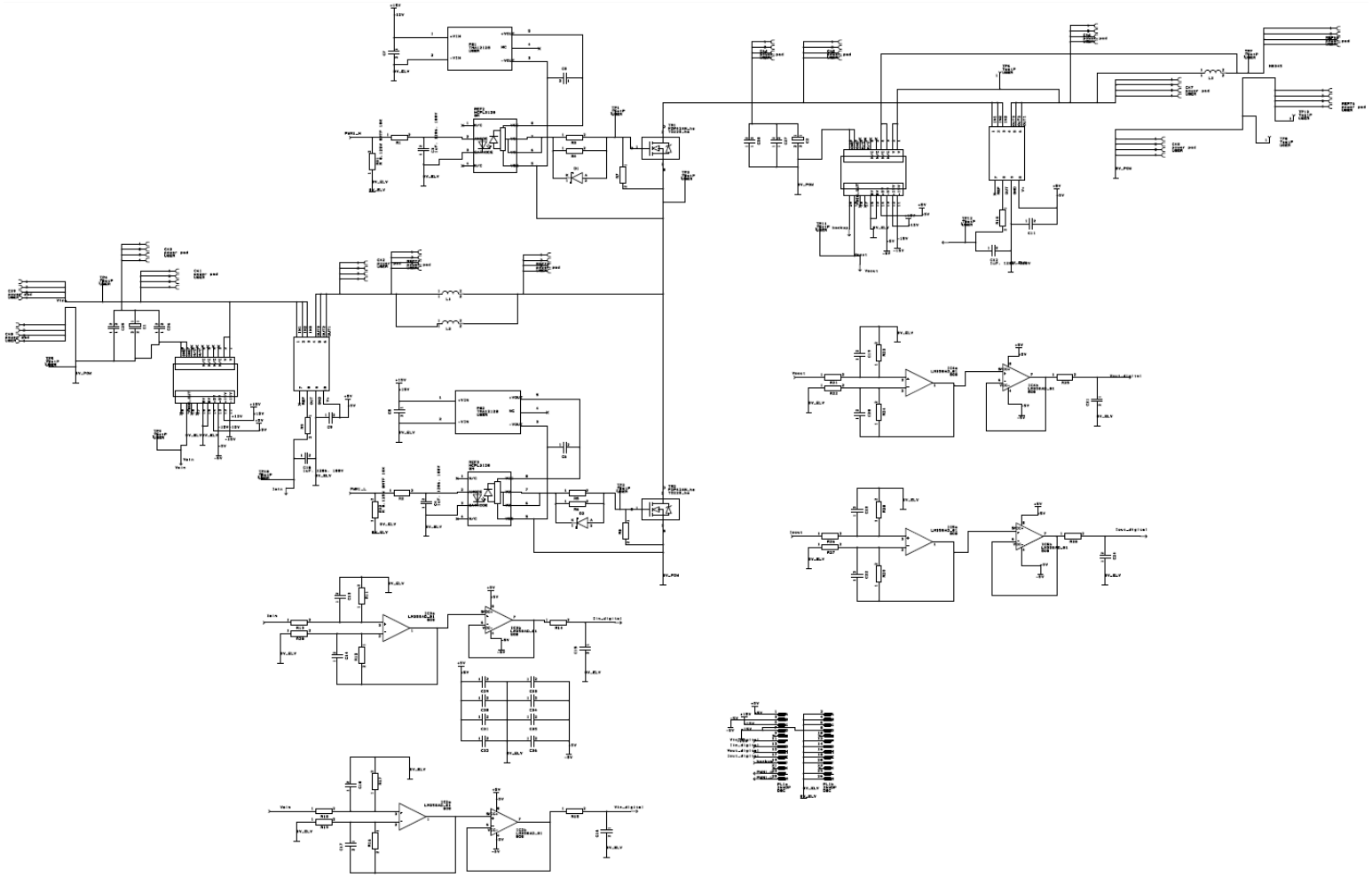

Figure A. 2 Schematic of power board.

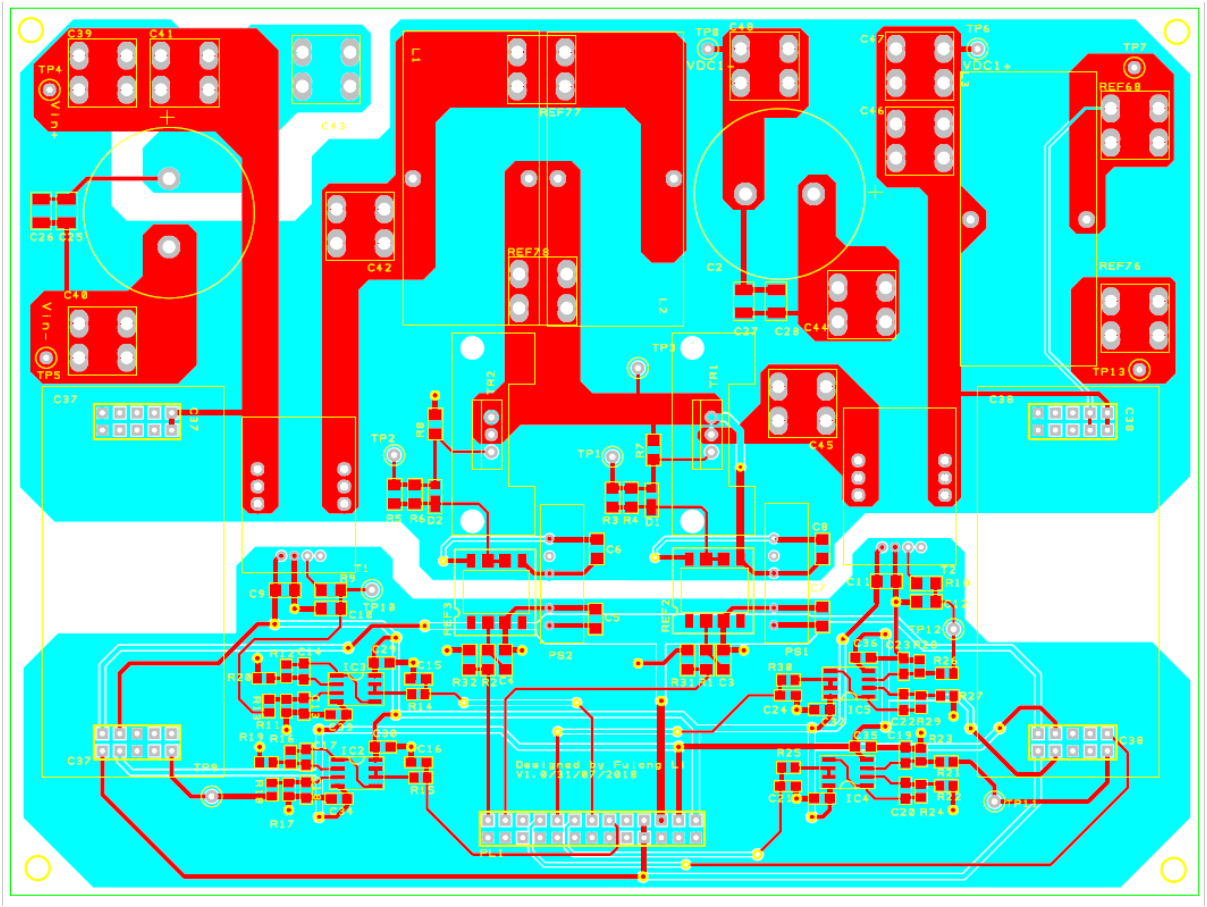

Figure A. 3 PCB layout of power board.

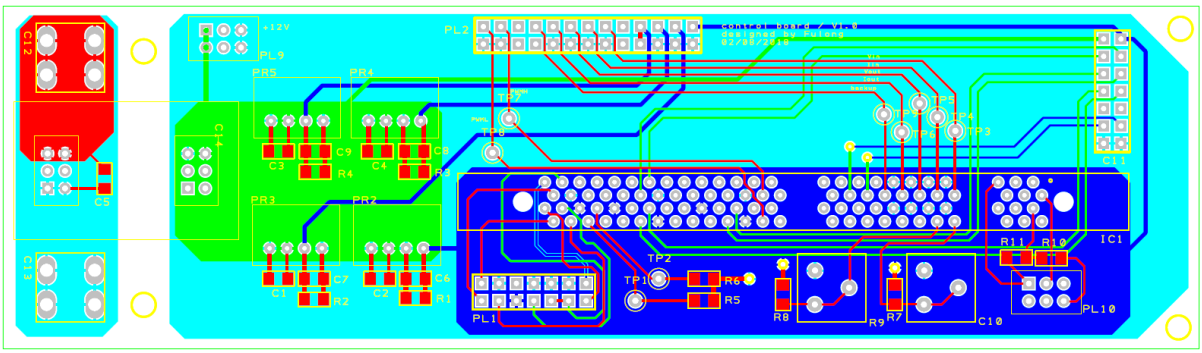

Figure A. 4 PCB layout of control board.

A2. Values of Passive Components

Table A- 1 Voltage sample circuit.

Types	Values	Types	Values
R_1	2kΩ*4	C_1	$1\mu F$
R_2	120Ω	C_2	$1\mu F$
R_3	10kΩ	C_3	$0.01\mu F$
R_4	10kΩ	C_4	$0.01\mu F$
R_5	10kΩ	C_5	$0.1\mu F$
R_6	10kΩ		
R_7	220Ω		

Table A- 2 Current sample circuit.

Types	Values	Types	Values
R_1	10Ω	C_1	$1\mu F$
R_2	10kΩ	C_2	$0.01\mu F$
R_3	10kΩ	C_3	$0.01\mu F$
R_4	5.6kΩ	C_4	$0.01\mu F$
R_5	5.6kΩ	C_5	$0.1\mu F$
R_6	220Ω		

Table A- 3 MOSFET drive circuit.

Types	Values	Types	Values
R_1	120Ω	C_1	$1\mu F$
R_2	20Ω	C_2	$100pF$
R_3	20Ω	C_3	$1\mu F$
R_4	10kΩ		

A3. Passive Stabiliser Design

A3.1 Calculations for Passive Controller

Passive with feedforward gain K,

$$G'_{vc} = K + G_{vc} \approx \frac{(\alpha + K) + s(K\gamma - \alpha\beta)}{1 + s\gamma} = \frac{(\alpha + K) + j\omega(K\gamma - \alpha\beta)}{1 + j\omega\gamma}$$

$$= \frac{[(\alpha + K) + j\omega(K\gamma - \alpha\beta)] \cdot (1 - j\omega\gamma)}{(1 + j\omega\gamma)(1 - j\omega\gamma)}$$

$$= \frac{\alpha + K - (\alpha + K)j\omega\gamma + j\omega(K\gamma - \alpha\beta) - j^2\omega^2\gamma(K\gamma - \alpha\beta)}{1 - (j\omega\gamma)^2}$$

$$= \frac{\alpha + K + \omega^2\gamma(K\gamma - \alpha\beta) + j\omega[(K\gamma - \alpha\beta) - (\alpha + K)\gamma]}{1 + \omega^2\gamma^2}$$

Passive with HPF-K,

$$G'_{vc} = G_p + G_{vc} \approx \frac{\alpha(1 - s\beta)(s + \delta) + sK(1 + s\gamma)}{(s + \delta) \cdot (1 + s\gamma)} = \frac{\alpha(1 - j\omega\beta)(j\omega + \delta) + j\omega K(1 + j\omega\gamma)}{(j\omega + \delta) \cdot (1 + j\omega\gamma)}$$

$$= \frac{\alpha(j\omega + \delta - j^2\omega^2\beta - j\omega\beta\delta) + j\omega K + j^2\omega^2 K\gamma}{j\omega + j^2\omega^2\gamma + \delta + j\omega\gamma\delta}$$

$$= \frac{j\omega\alpha + \alpha\delta - j^2\omega^2\alpha\beta - j\omega\alpha\beta\delta + j\omega K + j^2\omega^2 K\gamma}{\delta - \omega^2\gamma + j\omega(1 + \gamma\delta)}$$

$$= \frac{(\alpha\delta + \omega^2\alpha\beta - \omega^2 K\gamma) + j\omega(\alpha - \alpha\beta\delta + K)}{(\delta - \omega^2\gamma) + j\omega(1 + \gamma\delta)}$$

$$= \frac{[(\alpha\delta + \omega^2\alpha\beta - \omega^2 K\gamma) + j\omega(\alpha - \alpha\beta\delta + K)] \cdot [(\delta - \omega^2\gamma) - j\omega(1 + \gamma\delta)]}{[(\delta - \omega^2\gamma) + j\omega(1 + \gamma\delta)] \cdot [(\delta - \omega^2\gamma) - j\omega(1 + \gamma\delta)]}$$

$$= \frac{(\alpha\delta + \omega^2\alpha\beta - \omega^2 K\gamma)(\delta - \omega^2\gamma) - j\omega(1 + \gamma\delta)(\alpha\delta + \omega^2\alpha\beta - \omega^2 K\gamma)}{(\delta - \omega^2\gamma)^2 - j^2\omega^2(1 + \gamma\delta)^2}$$

$$+ \frac{j\omega(\alpha - \alpha\beta\delta + K)(\delta - \omega^2\gamma) - j^2\omega^2(\alpha - \alpha\beta\delta + K)(1 + \gamma\delta)}{(\delta - \omega^2\gamma)^2 - j^2\omega^2(1 + \gamma\delta)^2}$$

$$= \frac{(\alpha\delta + \omega^2\alpha\beta - \omega^2 K\gamma)(\delta - \omega^2\gamma) - j\omega(1 + \gamma\delta)(\alpha\delta + \omega^2\alpha\beta - \omega^2 K\gamma)}{(\delta - \omega^2\gamma)^2 + \omega^2(1 + \gamma\delta)^2}$$

$$+ \frac{j\omega(\alpha - \alpha\beta\delta + K)(\delta - \omega^2\gamma) + \omega^2(\alpha - \alpha\beta\delta + K)(1 + \gamma\delta)}{(\delta - \omega^2\gamma)^2 + \omega^2(1 + \gamma\delta)^2}$$

A3.2 Negative Frequency Calculations

$$1 - \omega^2 \beta\gamma = 0$$

$$1 = \omega^2 \beta\gamma$$

$$\omega = \sqrt{\frac{1}{\beta\gamma}} = \omega_N$$

$$f_N = \frac{1}{2\pi}\sqrt{\frac{1}{\beta\gamma}}$$

$$f_N = \frac{1}{2\pi}\sqrt{\frac{1}{\frac{L}{D'^2 R}\frac{RC}{2}}} = \frac{1}{2\pi}\sqrt{\frac{2D'^2}{LC}}$$

A4. Terminal Input Admittance Calculations

A4.1 Constant Power Load

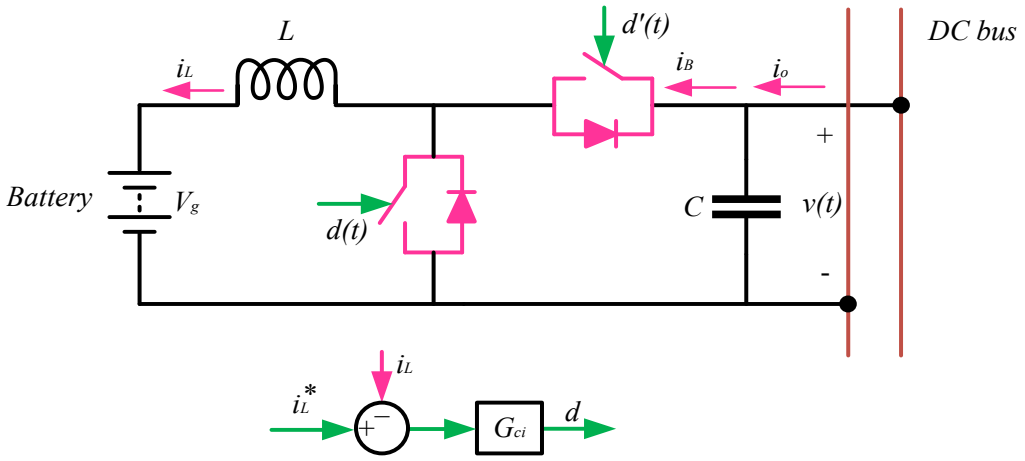

Figure A. 5 Circuit and control block diagram of constant power load.

$$\Delta i_L(s) = \frac{(1-D)\cdot\Delta v(s)}{sL} - \frac{\bar{V}\cdot\Delta d(s)}{sL}$$

$$\Delta i_B = \Delta i_L \cdot (1-D) - \Delta d(s)\cdot I_L$$

$$\Delta i_o(s) = \Delta i_B + sC\cdot\Delta v(s)$$

$$\Delta d(s) = -\Delta i_L \cdot G_{ci}$$

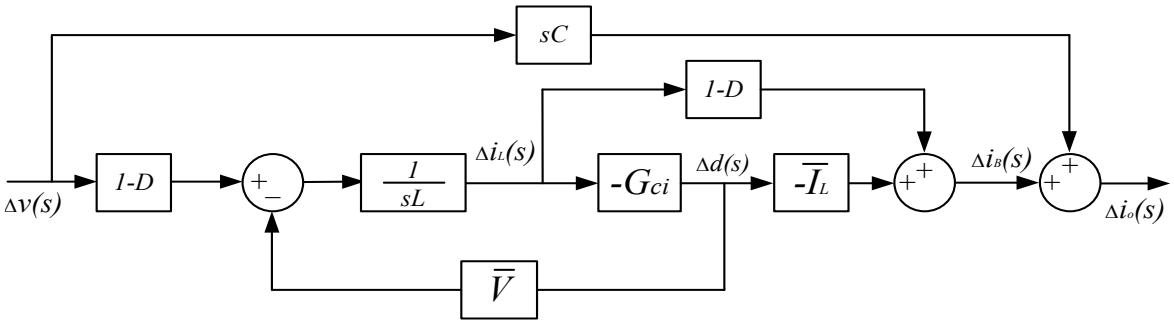

Figure A. 6 Signal flow chart of constant power load.

$$Lp_1 = \frac{-G_{ci}}{sL}\cdot\bar{V}\cdot(-1)$$

$$P_1 = (1-D)\frac{-G_{ci}}{sL}\cdot(-\bar{I}_L), \Delta_1 = 1$$

$$P_2 = (1-D)\frac{1}{sL}\cdot(1-D), \Delta_2 = 1$$

$$P_3 = sC, \Delta_3 = 1 - Lp_1$$

$$Y_T^{Bat\_CPL} = \frac{\Delta i_o(s)}{\Delta v(s)} = \frac{P_1\Delta_1 + P_2\Delta_2 + P_3\Delta_3}{1 - Lp_1} = \frac{\frac{(1-D)G_{ci}\bar{I}_L + (1-D)^2}{sL} + sC\left(1 - \frac{G_{ci}\bar{V}}{sL}\right)}{1 - \frac{G_{ci}\bar{V}}{sL}}$$

$$= \frac{(1-D)G_{ci}\bar{I}_L + (1-D)^2 + sC(sL - G_{ci}\bar{V})}{sL - G_{ci}\bar{V}}$$

$$Y_T^{Bat\_CPL} = \frac{\Delta i_o(s)}{\Delta v(s)} = \frac{P_1\Delta_1 + P_2\Delta_2 + P_3\Delta_3}{1 - Lp_1}$$

$$= \frac{(1-D)G_{im}\cdot\left(1 + \frac{\omega_z}{s}\right)\bar{I}_L + (1-D)^2 + sC(sL - G_{im}\cdot(1 + \frac{\omega_z}{s})\bar{V})}{sL - G_{im}\cdot(1 + \frac{\omega_z}{s})\bar{V}}$$

$$= \frac{(1-D)G_{im}\cdot(s+\omega_z)\bar{I}_L + s(1-D)^2 + sC(s^2L - G_{im}\cdot(s+\omega_z)\bar{V})}{s^2L - G_{im}\cdot(s+\omega_z)\bar{V}}$$

$$s \to 0, Y_T^{Bat\_CPL} \to \frac{(1-D)G_{im}(\omega_z)\bar{I}_L}{-G_{im}(\omega_z)\bar{V}} = \frac{(1-D)\bar{I}_L}{-\bar{V}} = -\frac{\bar{I}_o}{\bar{V}} = -\frac{1}{R}$$

A4.2 Constant Power Source

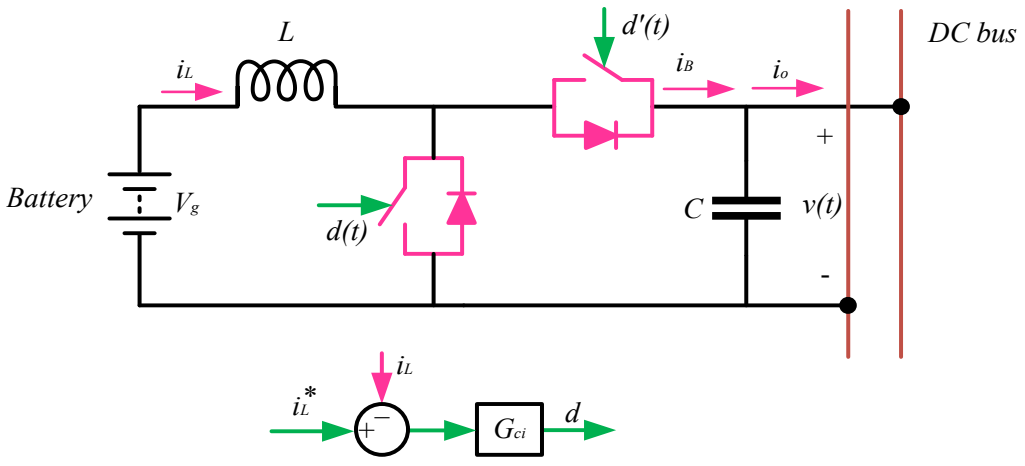

Figure A. 7 Circuit and control diagram of constant power source.

$$\Delta i_L(s) = \frac{\bar{V}\cdot\Delta d(s)}{sL} - \frac{(1-D)\cdot\Delta v(s)}{sL}$$

$$\Delta i_B = \Delta i_L \cdot (1-D) - \Delta d(s) \cdot I_L$$

$$\Delta i_o(s) = \Delta i_B - sC \cdot \Delta v(s)$$

$$\Delta d(s) = -\Delta i_L \cdot G_{ci}$$

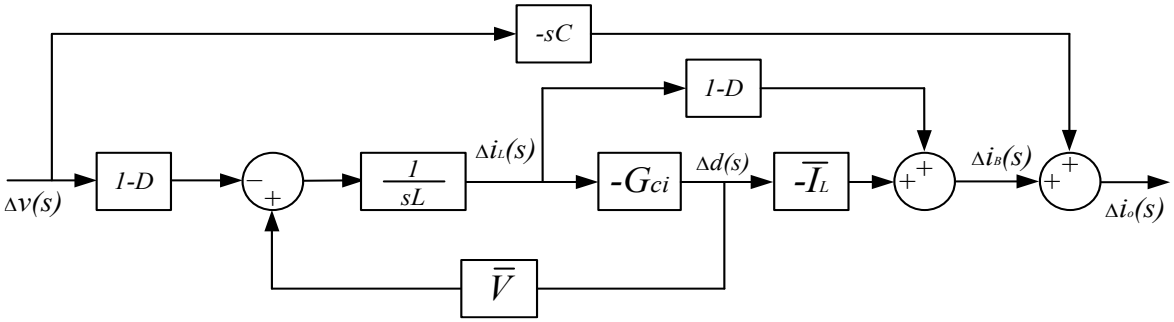

Figure A. 8 Signal flow chart of constant power source.

$$Lp_1 = \frac{-G_{ci}}{sL+r} \cdot \bar{V}$$

$$P_1 = -(1-D)\frac{-G_{ci}}{sL} \cdot (-\bar{I_L}), \Delta_1 = 1$$

$$P_2 = -(1-D)\frac{1}{sL} \cdot (1-D), \Delta_2 = 1$$

$$P_3 = -sC, \Delta_3 = 1 - Lp_1$$

$$Y_T^{Bat\_CPS} = -\frac{\Delta i_o(s)}{\Delta v(s)} = -\frac{P_1\Delta_1 + P_2\Delta_2 + P_3\Delta_3}{1-Lp_1} = \frac{\frac{(1-D)G_{ci}\bar{I_L} + (1-D)^2}{sL} + sC(1+\frac{G_{ci}\bar{V}}{sL})}{1+\frac{G_{ci}\bar{V}}{sL}}$$

$$= \frac{(1-D)G_{ci}\bar{I_L} + (1-D)^2 + sC(sL + G_{ci}\bar{V})}{sL + G_{ci}\bar{V}}$$

$$Y_T^{Bat\_CPS} = \frac{\Delta i_o(s)}{\Delta v(s)} = \frac{P_1\Delta_1 + P_2\Delta_2 + P_3\Delta_3}{1-Lp_1}$$

$$= \frac{(1-D)G_{im} \cdot \left(1+\frac{\omega_z}{s}\right)\bar{I_L} + (1-D)^2 + sC(sL + G_{im} \cdot (1+\frac{\omega_z}{s})\bar{V})}{sL + G_{im} \cdot (1+\frac{\omega_z}{s})\bar{V}}$$

$$= \frac{(1-D)G_{im} \cdot (s+\omega_z)\bar{I_L} + s(1-D)^2 + sC(s^2L + G_{im} \cdot (s+\omega_z)\bar{V})}{s^2L + G_{im} \cdot (s+\omega_z)\bar{V}}$$

$$s \to 0, Y_T^{Bat\_CPS} \to \frac{(1-D)G_{im}(\omega_z)\bar{I_L}}{G_{im}(\omega_z)\bar{V}} = \frac{(1-D)\bar{I_L}}{\bar{V}} = \frac{\bar{I_o}}{\bar{V}} = \frac{1}{R}$$

A5. Terminal Output Admittance Calculations

A5.1 Passive Stabilisers with Droop Control

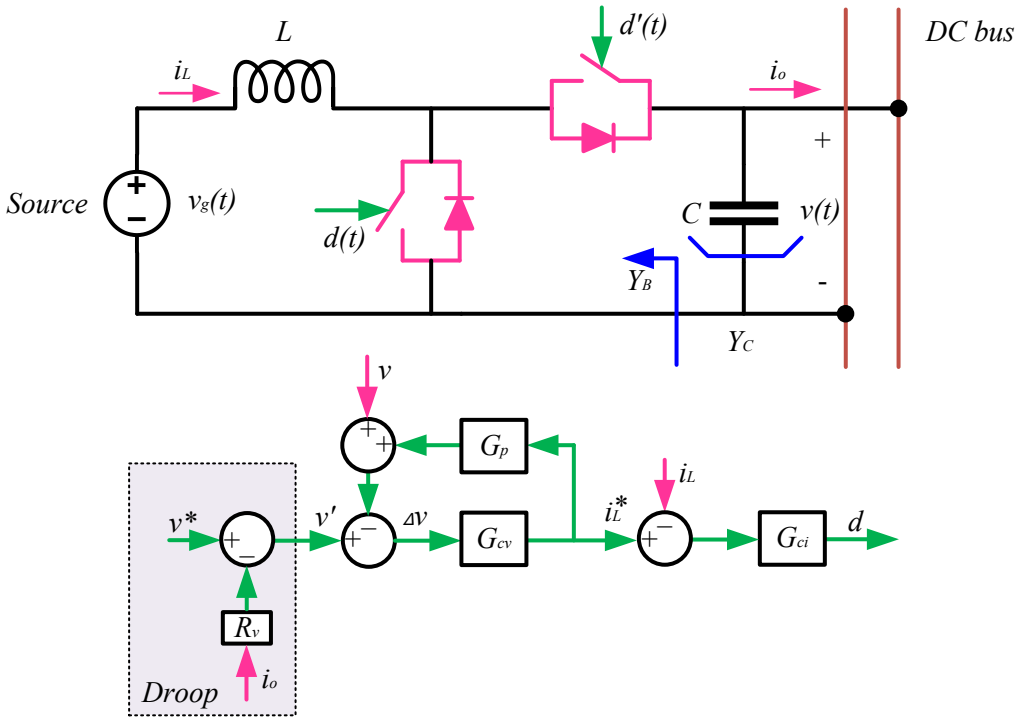

Figure A. 9 Circuit and control blcok diagram of source side converter.

Based on the circuit, we can attain,

$$\Delta i_L(s) = \frac{\bar{V} \cdot \Delta d(s)}{sL} - \frac{(1-D) \cdot \Delta v(s)}{sL}$$

$$\Delta i_B = \Delta i_L \cdot (1-D) - \Delta d(s) \cdot I_L$$

$$\Delta i_o(s) = \Delta i_B - sC \cdot \Delta v(s)$$

If assuming voltage reference v^* constant, and based on the control blocks shown above, then we can get,

$$i_L^* = \left(v' - \left(v + G_p \cdot i_L^*\right)\right) \cdot G_{cv} = \left(v^* - i_B \cdot R_v - \left(v + G_p \cdot i_L^*\right)\right) \cdot G_{cv}$$

$$\rightarrow \quad \Delta i_L^* = (-\Delta i_B R_v - \Delta v - G_p \cdot \Delta i_L^*) \cdot G_{cv}$$

$$\Delta d(s) = (\Delta i_L^* - \Delta i_L) \cdot G_{ci}$$

Applying above state equations on the control blocks, we can get

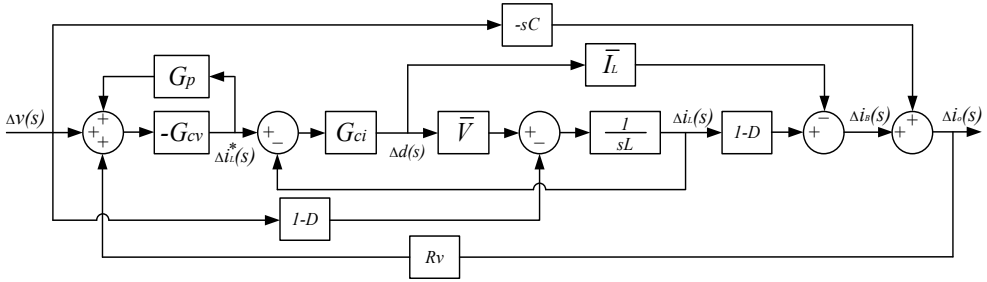

Figure A. 10 Signal flow chart of source side converter - whole controller.

If we apply Mason's gain formula, then we can get

$$Lp_1 = G_{ci}\bar{V}\frac{1}{sL}\cdot(-1)^1$$

$$Lp_2 = -G_{cv}G_{ci}\bar{V}\frac{1}{sL}(1-D)R_v\cdot(1)^1$$

$$Lp_3 = -G_{cv}G_{ci}\bar{I_L}R_v\cdot(-1)^1$$

$$Lp_4 = -G_pG_{cv}$$

$$LL_{p1} = Lp_1Lp_4$$

$$P_1 = -G_{cv}G_{ci}\bar{V}\frac{1}{sL}(1-D)\cdot(1)^1, \Delta_1 = 1$$

$$P_2 = (1-D)\frac{1}{sL}(1-D)\cdot(-1)^1, \Delta_2 = 1 - Lp_4$$

$$P_3 = -G_{cv}G_{ci}\bar{I_L}\cdot(-1)^1, \Delta_3 = 1$$

$$P_4 = (1-D)\frac{1}{sL}G_{ci}\bar{I_L}\cdot(-1)^3, \Delta_4 = 1 - Lp_4$$

$$P_5 = -sC, \Delta_5 = 1 - Lp_1 - Lp_4 + Lp_1Lp_4$$

So the final output admittance can be attained by following equation,

$$Y_o^{P\&D} = -\frac{\Delta i_o(s)}{\Delta v(s)} = -\frac{P_1\Delta_1 + P_2\Delta_2 + P_3\Delta_3 + P_4\Delta_4 + P_5\Delta_5}{1 - Lp_1 - Lp_2 - Lp_3 - Lp_4 + LL_{p1}}$$

$$= \frac{G_{cv}G_{ci}\bar{V}\frac{1}{sL}(1-D) + (1-D)^2\frac{1}{sL}\left(1+G_pG_{cv}\right) - G_{cv}G_{ci}\bar{I_L} + (1-D)\frac{1}{sL}G_{ci}\bar{I_L}\left(1+G_pG_{cv}\right)}{1 + G_{ci}\bar{V}\frac{1}{sL} + G_{cv}G_{ci}\bar{V}\frac{1}{sL}(1-D)R_v - G_{cv}G_{ci}\bar{I_L}R_v + G_pG_{cv} + G_{ci}\bar{V}\frac{1}{sL}G_pG_{cv}}$$

$$+ \frac{sC(1 + G_{ci}\bar{V}\frac{1}{sL} + G_pG_{cv} + G_pG_{cv}G_{ci}\bar{V}\frac{1}{sL})}{1 + G_{ci}\bar{V}\frac{1}{sL} + G_{cv}G_{ci}\bar{V}\frac{1}{sL}(1-D)R_v - G_{cv}G_{ci}\bar{I_L}R_v + G_pG_{cv} + G_{ci}\bar{V}\frac{1}{sL}G_pG_{cv}}$$

$$= \frac{G_{cv}G_{ci}\bar{V}(1-D) + (1-D)^2\left(1+G_pG_{cv}\right) - (sL)G_{cv}G_{ci}\bar{I_L} + (1-D)G_{ci}\bar{I_L}\left(1+G_pG_{cv}\right)}{(sL) + G_{ci}\bar{V} + G_{cv}G_{ci}\bar{V}(1-D)R_v - (sL)G_{cv}G_{ci}\bar{I_L}R_v + G_pG_{cv}(sL) + G_{ci}\bar{V}G_pG_{cv}}$$

$$+ \frac{sC((sL) + G_{ci}\bar{V} + (sL)G_pG_{cv} + G_pG_{cv}G_{ci}\bar{V})}{(sL) + G_{ci}\bar{V} + G_{cv}G_{ci}\bar{V}(1-D)R_v - (sL)G_{cv}G_{ci}\bar{I_L}R_v + G_pG_{cv}(sL) + G_{ci}\bar{V}G_pG_{cv}}$$

Where $G_{ci} = G_{im}\cdot\frac{1+\frac{\omega_z}{s}}{1+\frac{s}{\omega_p}}$, $G_{cv} = G_{vm}\cdot(1+\frac{\omega_{zv}}{s})$ and $G_p = K\frac{s}{s+\delta}$.

$$Y_o^{P\&D}$$

$$= \frac{G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{V}(1-D)+(1-D)^2\left(1+\frac{sK}{s+\delta}G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)\right)-(sL)G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{I}_L+(1-D)G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{I}_L\left(1+\frac{sK}{s+\delta}G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)\right)}{(sL)+G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{V}+G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{V}(1-D)R_v-(sL)G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{I}_LR_v+\frac{sK}{s+\delta}G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)(sL)+G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\frac{sK}{s+\delta}\bar{V}}$$

$$+\frac{sC((sL)+G_{ci}\bar{V}+(sL)\frac{sK}{s+\delta}G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)+G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\frac{sK}{s+\delta}\bar{V})}{(sL)+G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{V}+G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{V}(1-D)R_v-(sL)G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{I}_LR_v+\frac{sK}{s+\delta}G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)(sL)+G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\frac{sK}{s+\delta}\bar{V}}$$

$$= \frac{G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\bar{V}(1-D)+s(1-D)^2\left(s+\frac{sK}{s+\delta}G_{vm}(s+\omega_{zv})\right)-(sL)G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\bar{I}_L+(1-D)G_{im}(s+\omega_z)\bar{I}_L\left(s+\frac{sK}{s+\delta}G_{vm}(s+\omega_{zv})\right)}{s^2(sL)+sG_{im}(s+\omega_z)\bar{V}+G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\bar{V}(1-D)R_v-(sL)G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\bar{I}_LR_v+\frac{sK}{s+\delta}G_{vm}(s+\omega_{zv})(sL)s+G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\frac{sK}{s+\delta}\bar{V}}$$

$$+\frac{sC(s^2(sL)+s^2G_{ci}\bar{V}+s(sL)\frac{sK}{s+\delta}G_{vm}(s+\omega_{zv})+G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\frac{sK}{s+\delta}\bar{V})}{s^2(sL)+sG_{im}(s+\omega_z)\bar{V}+G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\bar{V}(1-D)R_v-(sL)G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\bar{I}_LR_v+\frac{sK}{s+\delta}G_{vm}(s+\omega_{zv})(sL)s+G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\frac{sK}{s+\delta}\bar{V}}$$

$$s\to 0, Y_T^{P\&D}\to\frac{G_{vm}(\omega_{zv})G_{im}(\omega_z)\bar{V}(1-D)}{G_{vm}(\omega_{zv})G_{im}(\omega_z)\bar{V}(1-D)R_v}=\frac{1}{R_v}$$

A5.2 Droop Control without Passive Stabilisers

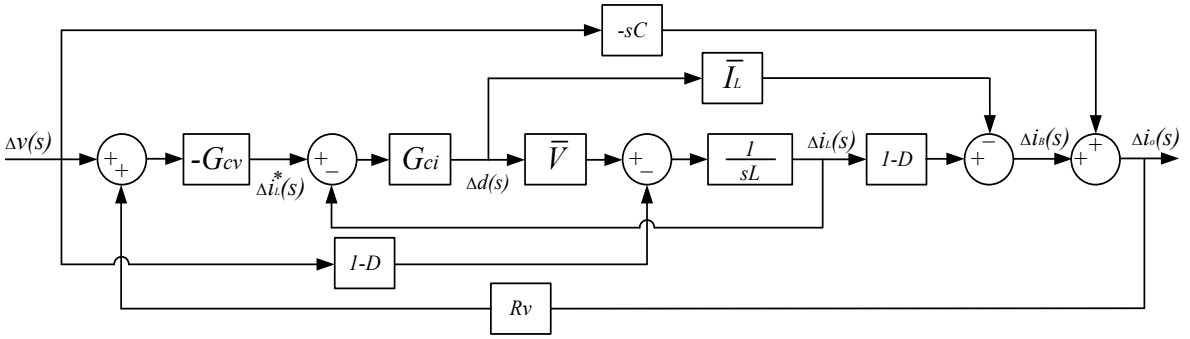

Figure A. 11 Signal flow chart of source side converter - droop controller.

$$Lp_1 = G_{ci}\bar{V}\frac{1}{sL}\cdot(-1)^1$$

$$Lp_2 = -G_{cv}G_{ci}\bar{V}\frac{1}{sL}(1-D)R_v\cdot(1)^1$$

$$Lp_3 = -G_{cv}G_{ci}\bar{I_L}R_v\cdot(-1)^1$$

$$P_1 = -G_{cv}G_{ci}\bar{V}\frac{1}{sL}(1-D)\cdot(1)^1, \Delta_1 = 1$$

$$P_2 = (1-D)\frac{1}{sL}(1-D)\cdot(-1)^1, \Delta_2 = 1$$

$$P_3 = -G_{cv}G_{ci}\bar{I_L}\cdot(-1)^1, \Delta_3 = 1$$

$$P_4 = (1-D)\frac{1}{sL}G_{ci}\bar{I_L}\cdot(-1)^3, \Delta_4 = 1$$

$$P_5 = -sC, \Delta_5 = 1 - Lp_1$$

$$Y_T^D = -\frac{\Delta i_o(s)}{\Delta v(s)} = -\frac{P_1\Delta_1 + P_2\Delta_2 + P_3\Delta_3 + P_4\Delta_4 + P_5\Delta_5}{1 - Lp_1 - Lp_2 - Lp_3}$$

$$= \frac{G_{cv}G_{ci}\bar{V}\frac{1}{sL}(1-D) + (1-D)^2\frac{1}{sL} - G_{cv}G_{ci}\bar{I_L} + (1-D)\frac{1}{sL}G_{ci}\bar{I_L}}{1 + G_{ci}\bar{V}\frac{1}{sL} + G_{cv}G_{ci}\bar{V}\frac{1}{sL}(1-D)R_v - G_{cv}G_{ci}\bar{I_L}R_v} + \frac{sC(1 + G_{ci}\bar{V}\frac{1}{sL})}{1 + G_{ci}\bar{V}\frac{1}{sL} + G_{cv}G_{ci}\bar{V}\frac{1}{sL}(1-D)R_v - G_{cv}G_{ci}\bar{I_L}R_v}$$

$$= \frac{G_{cv}G_{ci}\bar{V}(1-D) + (1-D)^2 - (sL)G_{cv}G_{ci}\bar{I_L} + (1-D)G_{ci}\bar{I_L}}{(sL) + G_{ci}\bar{V} + G_{cv}G_{ci}\bar{V}(1-D)R_v - (sL)G_{cv}G_{ci}\bar{I_L}R_v} + \frac{sC((sL) + G_{ci}\bar{V})}{(sL) + G_{ci}\bar{V} + G_{cv}G_{ci}\bar{V}(1-D)R_v - (sL)G_{cv}G_{ci}\bar{I_L}R_v}$$

$$Y_T^D = \frac{G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{V}(1-D) + (1-D)^2 - (sL)G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{I_L} + (1-D)G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{I_L} + sC((sL) + G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{V})}{(sL) + G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{V} + G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{V}(1-D)R_v - (sL)G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{I_L}R_v}$$

$$= \frac{G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\bar{V}(1-D) + s^2(1-D)^2 - (sL)G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\bar{I_L} + s(1-D)G_{im}(s+\omega_z)\bar{I_L} + sC(s^2(sL) + sG_{im}(s+\omega_z)\bar{V})}{s^2(sL) + sG_{im}(s+\omega_z)\bar{V} + G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\bar{V}(1-D)R_v - (sL)G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\bar{I_L}R_v}$$

$$s \to 0, Y_T^D \to \frac{G_{vm}(\omega_{zv})G_{im}(\omega_z)\bar{V}(1-D)}{G_{vm}(\omega_{zv})G_{im}(\omega_z)\bar{V}(1-D)R_v} = \frac{1}{R_v}$$

A5.3 Passive Stabilisers without Droop Control

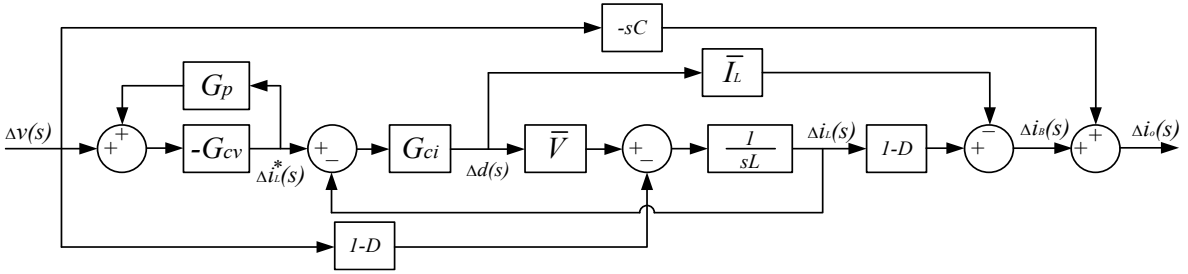

Figure A. 12 Signal flow chart of source side converter - passive controller.

$$Lp_1 = G_{ci}\bar{V}\frac{1}{sL}\cdot(-1)^1$$

$$Lp_4 = -G_pG_{cv}$$

$$LL_{p1} = Lp_1Lp_4$$

$$P_1 = -G_{cv}G_{ci}\bar{V}\frac{1}{sL}(1-D)\cdot(1)^1, \Delta_1 = 1$$

$$P_2 = (1-D)\frac{1}{sL}(1-D)\cdot(-1)^1, \Delta_2 = 1 - Lp_4$$

$$P_3 = -G_{cv}G_{ci}\bar{I_L}\cdot(-1)^1, \Delta_3 = 1$$

$$P_4 = (1-D)\frac{1}{sL}G_{ci}\bar{I_L}\cdot(-1)^3, \Delta_4 = 1 - Lp_4$$

$$P_5 = -sC, \Delta_5 = 1 - Lp_1 - Lp_4 + Lp_1Lp_4$$

So the final output admittance can be attained by following equation,

$$Y_o^{Pa} = -\frac{\Delta i_o(s)}{\Delta v(s)} = -\frac{P_1\Delta_1 + P_2\Delta_2 + P_3\Delta_3 + P_4\Delta_4 + P_5\Delta_5}{1 - Lp_1 - Lp_4 + LL_{p1}}$$

$$= \frac{G_{cv}G_{ci}\bar{V}\frac{1}{sL}(1-D) + (1-D)^2\frac{1}{sL}\left(1+G_pG_{cv}\right) - G_{cv}G_{ci}\bar{I_L} + (1-D)\frac{1}{sL}G_{ci}\bar{I_L}\left(1+G_pG_{cv}\right)}{1 + G_{ci}\bar{V}\frac{1}{sL} + G_pG_{cv} + G_{ci}\bar{V}\frac{1}{sL}G_pG_{cv}} + \frac{sC(1 + G_{ci}\bar{V}\frac{1}{sL} + G_pG_{cv} + G_pG_{cv}G_{ci}\bar{V}\frac{1}{sL})}{1 + G_{ci}\bar{V}\frac{1}{sL} + G_pG_{cv} + G_{ci}\bar{V}\frac{1}{sL}G_pG_{cv}}$$

$$= \frac{G_{cv}G_{ci}\bar{V}(1-D) + (1-D)^2\left(1+G_pG_{cv}\right) - (sL)G_{cv}G_{ci}\bar{I_L} + (1-D)G_{ci}\bar{I_L}\left(1+G_pG_{cv}\right)}{(sL) + G_{ci}\bar{V} + G_pG_{cv}(sL) + G_{ci}\bar{V}G_pG_{cv}} + \frac{sC((sL) + G_{ci}\bar{V} + (sL)G_pG_{cv} + G_pG_{cv}G_{ci}\bar{V})}{(sL) + G_{ci}\bar{V} + G_pG_{cv}(sL) + G_{ci}\bar{V}G_pG_{cv}}$$

$$Y_o^{Pa} = \frac{G_{cv}G_{ci}\bar{V}(1-D) + (1-D)^2\left(1+G_pG_{cv}\right) - (sL)G_{cv}G_{ci}\bar{I_L} + (1-D)G_{ci}\bar{I_L}\left(1+G_pG_{cv}\right) + sC((sL) + G_{ci}\bar{V} + (sL)G_pG_{cv} + G_pG_{cv}G_{ci}\bar{V})}{(sL) + G_{ci}\bar{V} + G_pG_{cv}(sL) + G_{ci}\bar{V}G_pG_{cv}}$$

$$= \frac{G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{V}(1-D) + (1-D)^2\left(1+\frac{sK}{s+\delta}G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)\right) - (sL)G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{I_L} + (1-D)G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{I_L}\left(1+\frac{sK}{s+\delta}G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)\right)}{(sL) + G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{V} + \frac{sK}{s+\delta}G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)(sL) + G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\frac{sK}{s+\delta}\bar{V}}$$

$$+ \frac{sC((sL) + G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{V} + (sL)\frac{sK}{s+\delta}G_{vm}\left(1+\frac{\omega_{zv}}{s}\right) + G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\frac{sK}{s+\delta}\bar{V})}{(sL) + G_{im}\left(1+\frac{\omega_z}{s}\right)\bar{V} + \frac{sK}{s+\delta}G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)(sL) + G_{vm}\left(1+\frac{\omega_{zv}}{s}\right)G_{im}\left(1+\frac{\omega_z}{s}\right)\frac{sK}{s+\delta}\bar{V}}$$

$$= \frac{G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\bar{V}(1-D) + s(1-D)^2\left(s+\frac{sK}{s+\delta}G_{vm}(s+\omega_{zv})\right) - (sL)G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\bar{I_L} + (1-D)G_{im}(s+\omega_z)\bar{I_L}\left(s+\frac{sK}{s+\delta}G_{vm}(s+\omega_{zv})\right)}{s^2(sL) + sG_{im}(s+\omega_{zv})\bar{V} + s\frac{sK}{s+\delta}G_{vm}(s+\omega_{zv})(sL) + G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\frac{sK}{s+\delta}\bar{V}}$$

$$+ \frac{sC(s^2(sL) + sG_{im}(s+\omega_z)\bar{V} + s(sL)\frac{sK}{s+\delta}G_{vm}(s+\omega_{zv}) + G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\frac{sK}{s+\delta}\bar{V})}{s^2(sL) + sG_{im}(s+\omega_{zv})\bar{V} + s\frac{sK}{s+\delta}G_{vm}(s+\omega_{zv})(sL) + G_{vm}(s+\omega_{zv})G_{im}(s+\omega_z)\frac{sK}{s+\delta}\bar{V}}$$

$$s \to 0, Y_T^{HPF-K} \to \frac{G_{vm}(\omega_{zv})G_{im}(\omega_z)\bar{V}(1-D)}{0} \to +\infty$$

A5.4 Initial Double Loop Control

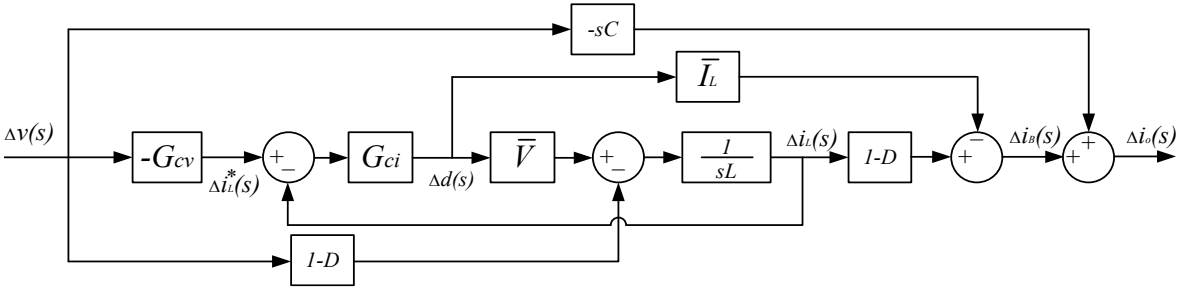

Figure A. 13 Signal flow chart of source side converter - double loop controller.

$$Lp_1 = G_{ci}\bar{V}\frac{1}{sL}\cdot(-1)^1$$

$$P_1 = -G_{cv}G_{ci}\bar{V}\frac{1}{sL}(1-D)\cdot(1)^1, \Delta_1 = 1$$

$$P_2 = (1-D)\frac{1}{sL}(1-D)\cdot(-1)^1, \Delta_2 = 1$$

$$P_3 = -G_{cv}G_{ci}\bar{I_L}\cdot(-1)^1, \Delta_3 = 1$$

$$P_4 = (1-D)\frac{1}{sL}G_{ci}\bar{I_L}\cdot(-1)^3, \Delta_4 = 1$$

$$P_5 = -sC, \Delta_5 = 1 - Lp_1$$

So the final output admittance can be attained by following equation,

$$Y_T^{dbl} = -\frac{\Delta i_o(s)}{\Delta v(s)} = -\frac{P_1\Delta_1 + P_2\Delta_2 + P_3\Delta_3 + P_4\Delta_4 + P_5\Delta_5}{1 - Lp_1} = \frac{G_{cv}G_{ci}\bar{V}\frac{1}{sL}(1-D) + (1-D)^2\frac{1}{sL} - G_{cv}G_{ci}\bar{I_L} + (1-D)\frac{1}{sL}G_{ci}\bar{I_L} + sC(1 + G_{ci}\bar{V}\frac{1}{sL})}{1 + G_{ci}\bar{V}\frac{1}{sL}}$$

$$= \frac{G_{cv}G_{ci}\bar{V}(1-D) + (1-D)^2 - (sL)G_{cv}G_{ci}\bar{I_L} + (1-D)G_{ci}\bar{I_L} + sC((sL) + G_{ci}\bar{V})}{(sL) + G_{ci}\bar{V}}$$

$$Y_T^{dbl} = \frac{G_{cv}G_{ci}\bar{V}(1-D) + (1-D)^2 - (sL)G_{cv}G_{ci}\bar{I_L} + (1-D)G_{ci}\bar{I_L} + sC((sL) + G_{ci}\bar{V})}{(sL) + G_{ci}\bar{V}}$$

$$= \frac{G_{vm}\left(1 + \frac{\omega_{zv}}{s}\right)G_{im}\left(1 + \frac{\omega_z}{s}\right)\bar{V}(1-D) + (1-D)^2 - (sL)G_{vm}\left(1 + \frac{\omega_{zv}}{s}\right)G_{im}\left(1 + \frac{\omega_z}{s}\right)\bar{I_L} + (1-D)G_{im}\cdot\left(1 + \frac{\omega_z}{s}\right)\bar{I_L} + sC((sL) + G_{im}\cdot(1 + \frac{\omega_z}{s})\bar{V})}{(sL) + G_{im}\cdot(1 + \frac{\omega_z}{s})\bar{V}}$$

$$= \frac{G_{vm}(s + \omega_{zv})G_{im}(s + \omega_z)\bar{V}(1-D) + s^2(1-D)^2 - (sL)G_{vm}(s + \omega_{zv})G_{im}(s + \omega_z)\bar{I_L} + s(1-D)G_{im}(s + \omega_z)\bar{I_L} + sC(s^2(sL) + sG_{im}(s + \omega_z)\bar{V})}{s^2(sL) + sG_{im}\cdot(s + \omega_z)\bar{V}}$$

$$s \to 0, Y_T^{dbl} \to \frac{G_{vm}(\omega_{zv})G_{im}(\omega_z)\bar{V}(1-D)}{0} \to +\infty$$

$$Z_T^{dbl} \to 0$$

A6. Signal Series Explanations

Table A- 4 Table of Signal Series Explanations

Sent by IC dominant	Signal series	Sent by IC servant
On-grid operation with IC1 maintaining the bus voltage		
Switch ON IC2, working at power mode and absorb power from grid with 1A.	110000	IC2 ON, working at power mode, and needs to be charged at 1A
Switch ON IC2, working at power mode and absorb power from grid with 2A.	110001	IC2 ON, working at power mode, and needs to be charged at 2A
Switch ON IC3, working at power mode and absorb power from grid with 1A.	111000	IC3 ON, working at power mode, and needs to be charged at 1A
Switch ON IC3, working at power mode and absorb power from grid with 2A.	111001	IC3 ON, working at power mode, and needs to be charged at 2A
N/A	110010	IC2 ON, working at power mode, and able to be discharge at 1A
N/A	110011	IC2 ON, working at power mode, and able to be discharge at 2A
N/A	111010	IC3 ON, working at power mode, and able to be discharge at 1A
N/A	111011	IC3 ON, working at power mode, and able to be discharge at 2A
Switch ON IC2, work at voltage mode with droop mode	1101xx	N/A
Off-grid operation with IC2 maintaining the bus voltage		
Switch ON IC3, working at power mode and absorb power from grid with 1A.	111000	IC3 ON, working at power mode, and needs to be charged at 1A
Switch ON IC3, working at power mode and absorb power from grid with 2A.	111001	IC3 ON, working at power mode, and needs to be charged at 2A
N/A	111010	IC3 ON, working at power mode, and able to be discharge at 1A
N/A	111011	IC3 ON, working at power mode, and able to be discharge at 2A