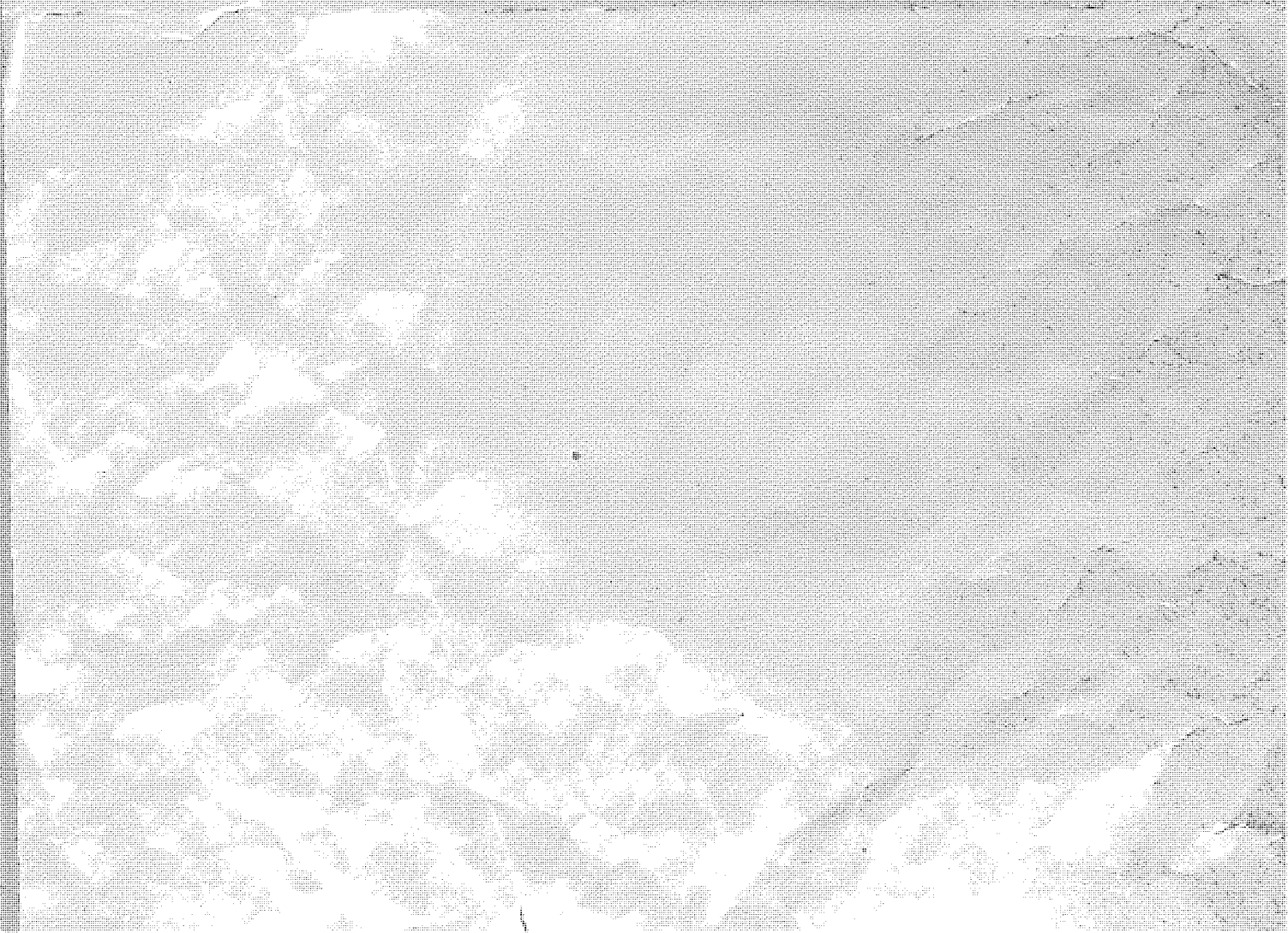

All-optical regenerative memory using a single device

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Doctor of Philosophy

Aston University

October 2009

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In recent years the optical domain has been traditionally reserved for node-to-node transmission with the processing and switching achieved entirely in the electrical domain. However, with the constantly increasing demand for bandwidth and the resultant increase in transmission speeds, there is a very real fear that current electronic technology as used for processing will not be able to cope with future demands. Fuelled by this requirement for faster processing speeds, considerable research is currently being carried out into the potential of All-optical processing.

One of the fundamental obstacles in realising All-optical processing is the requirement for All-optical buffering. Without all-optical buffers it is extremely difficult to resolve situations such as contention and congestion. Many devices have been proposed to solve this problem however none of them provide the perfect solution.

The subject of this research is to experimentally demonstrate a novel all-optical memory device. Unlike many previously demonstrated optical storage devices the device under consideration utilises only a single loop mirror and a single SOA as its switch, whilst providing full regenerative capabilities required for long-term storage. I will explain some of the principles and characteristics of the device, which will then be experimentally demonstrated. The device configuration will then be studied and investigated as to its suitability for Hybrid Integrated Technology

Additional keywords and phrases

Non-linear optics, cross-phase modulation, All-optical memory, Terahertz Optical Asymmetric Demultiplexor, Semiconductor optical amplifiers. Hybrid integrated device.

Acknowledgements

This thesis would not have been possible without the guidance help and support of many people. Firstly, I would like to thanks my parents for always being there. Not only throughout this thesis but also throughout the total duration of all my studies passed, present and future. Secondly, this research would not have been possible or as enjoyable without the help and support from the excellent staff at Aston University. I would like in particular to thank Dr Paul Harper for his knowledge, experience and friendship without which my research would not have been as successful or as pleasurable. I would also like to acknowledge Dr Jim Harrison for his help, friendship and guidance.

I would like to add a special thank you to Professor Keith Blow who has been much more than just a supervisor. I would like to thank him for the patience he has shown throughout my studies; through him I have learn't so much. Throughout my research his guidance and knowledge has made all the difference.

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1. Introduction to optical communications

1.1. Introduction

One of the earliest and most notable events in the history of telecommunications was the laying of the first transatlantic telegraphy cable in 1858. Although this cable provided the first quai-instantaneous (as compared to post) communication link across the Atlantic, it took 2 minutes to send a single word [1]. After three weeks of operation, during which four hundred messages had been sent, the line finally fell silent. Since this major milestone in communications, many advances have been made using different technologies, notably the Guglielmo Marconi first transatlantic commercial radio transmission service in the 1900s [2] and the launch of the first commercial satellite Telstar in 1962 [3].

Since the 1950s the benefits of using light as a transmission median had been understood. It was during the 1970's, however, that the demand for extra capacity led to the discovery that light could be propagated along a fibre with a loss of less than 20dB/km. With the new improved fibre and the advancements of optical amplifiers, ultra fast optical communication became a reality [4].

In comparison to the move of long haul data transmission from the traditional "copper twisted pair" (which has been the backbone of the telecommunications industry for most of the 20^{th} Century), to optical transmission, pre and post transmission processing of the signals is still dominated by electronics. Although processing using electronics is well established and understood it has two major disadvantages. Firstly the speed of the electronics is limited by the switching speed of a transistor, which in high-speed optical terms is relatively slow. In addition this actual process of

transferring a signal from optical to electrical and visa versa produces serious performance bottlenecks [5]. It is these disadvantages that have brought about the interest in all-optical processing [6].

To understand where all-optical processing fits into a high-speed all optical network it is essential to understand some basic system details.

1.2. Optical fibre

A basic optical transmission system consists of three individual components a transmitter, a transport medium and a receiver. The initial component is the transmitter, which converts the payload data to an optical signal that is suitable for optical transmission. The modulated optical signal containing the data, generated by the transmitter, is then sent through a waveguide (typically doped silica fibres) to transport the light signal to its final destination. Finally once the modulated signal has reached its destination the receiver then decodes the received signal and extracts the original data [7, 8].

As the name suggests, a waveguide guides a wave of light in a desired direction. In a modern high capacity optical network this is normally achieved through the use of optical fibre. It is well documented that all optical fibres rely on a phenomenon known as total internal reflection, to contain and direct the propagating light [9-11].

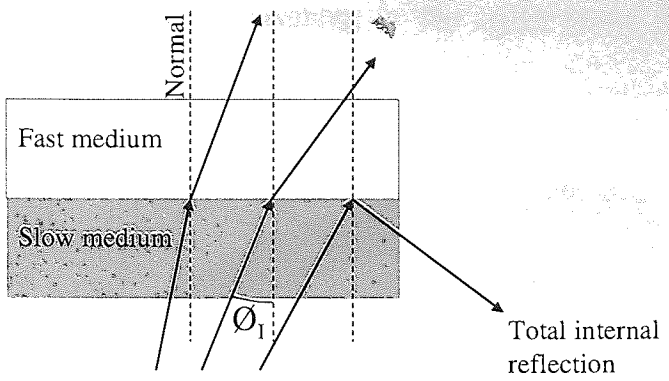


Figure 1-1 Total internal reflection occurs when the angle of incidence ($\varnothing_I$) is equal to or greater than the critical angle.

Optical fibres are made up of two main components: the core, where most of the light propagates; and a cladding, which surrounds the core. The refractive index (which is the ratio of the speed of light in a vacuum and the speed of light in the subject material, a higher index corresponds to a slower medium) of the core is higher than the cladding allowing for total internal reflection to take place. In an optical fibre the critical angle $\varnothing_c$, required for total internal reflection, is dependant upon the refractive index of both the core and the cladding and can be calculated as [11]:

$$\varnothing_c = \sin^{-1}\left(\frac{n_2}{n_1}\right) \qquad (1.1)$$

Where n_1 and n_2 represent the refractive index of the fibre core and the fibre cladding respectfully. Any angle of incidence greater than $\varnothing_c$ will cause the light to reflect inward and therefore be contained within the fibre, hence providing this condition is maintained it is possible to guide light around a bend. Figure 1-2 shows that even though the fibre is curved, providing the bend radius is large enough, light can be guided around a corner using multiple total internal reflections [9]. As the radius is reduced, however, the incident angle is reduced and therefore light will escape the

waveguide causing "bend loss", resulting in the signal being attenuated and a reduction in the received power.

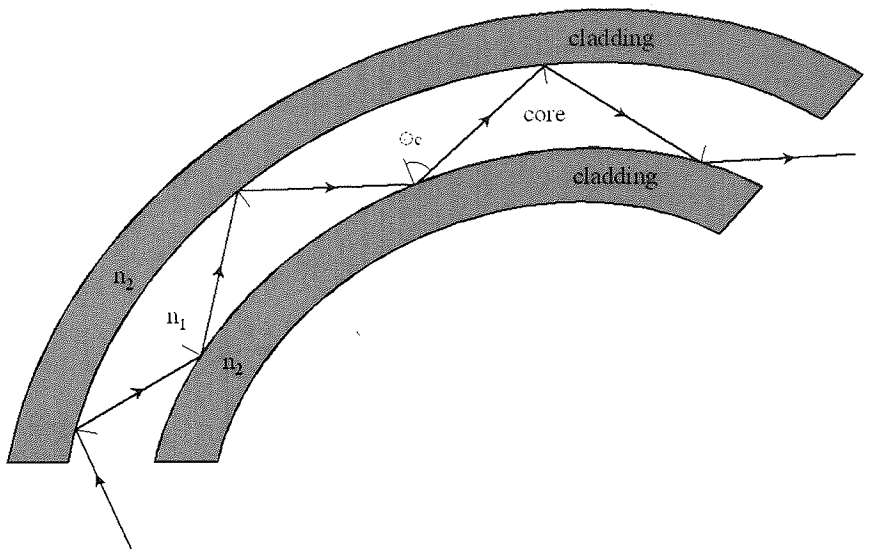


Figure 1-2 Light entering one end of a curved fibre will propagate using internal reflection and exit at the opposite end

The refractive index, or the speed at which light travels through a medium, is dependant upon the material. Usually in optical transmission fibres the core and cladding are made primarily of silica (SiO_2), having a nominal refractive index of 1.45. To allow for total internal reflection the core and cladding must be different and this is usually achieved by doping the core with a few percent of Germanium (Ge) [12].

Although some of the propagating light can be found in the cladding, the signal is mainly transmitted through the core. There are two main categories of optical fibre which are classed as either single mode, commonly used in modern systems, or multimode, as can be found in earlier systems [13]. The category to which a fibre belongs is largely dependent upon the size of the core see Figure 1-3.

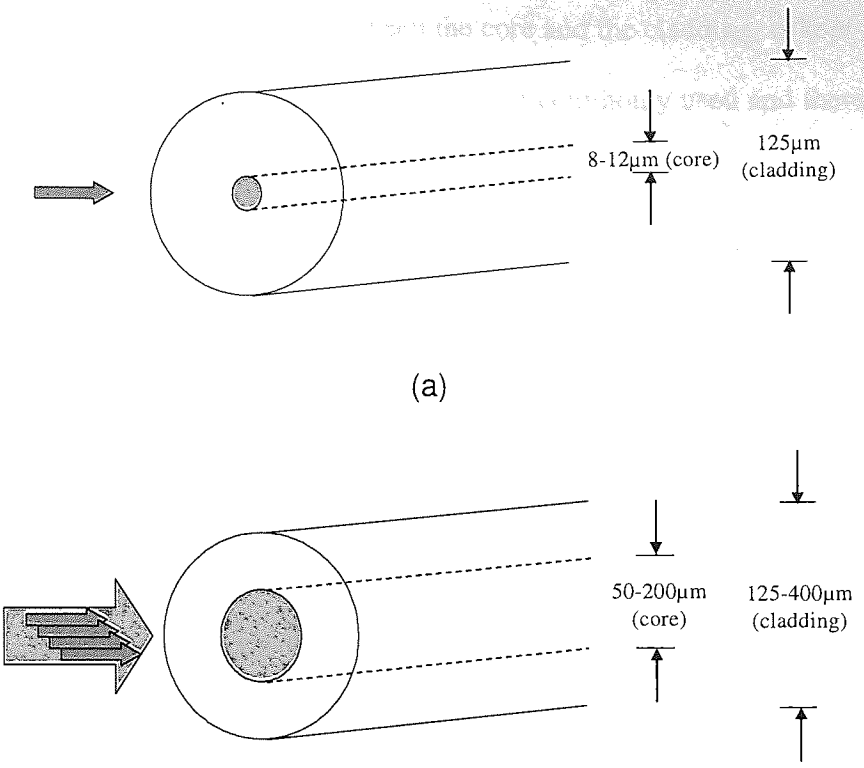


Figure 1-3 Propagation of singlemode (a) and multimode (b) fibres and typical dimensions

The terms multimode and singlemode are derived from the number of fundamental modes that a fibre uses to transfer light. With multimode fibre the light is transferred through a collection of spatial transverse modes unlike a single mode fibre that uses only one mode Figure 1-3. Whether a fibre is single mode or multimode is determined by the V parameter, which can be defined for a perfect "step-index" core as [14]:

$$V = \frac{2\pi a}{\lambda}\sqrt{n_1^2 - n_2^2} \qquad (1.2)$$

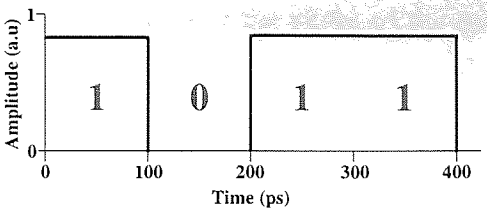
Where a is the fibre radius, λ represents the wavelength of the incident light. Single mode fibres, as the name suggests, have only one fundamental mode. Consequently, for a single mode fibre to exist it must satisfy the condition of $V < 2.405$ [15]. This requirement can be easily achieved, providing the core diameter is kept small and the

difference in the refractive index, between the core and the cladding, is kept low. It is the Single Mode Fibre (SMF), which is now most commonly used and therefore will be used for the rest of this thesis.

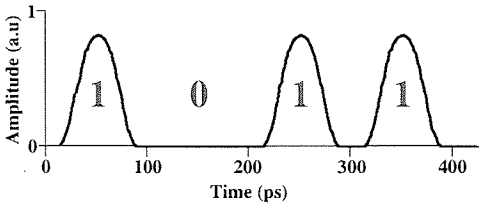
1.3. Digital transmission over optical fibres

The ability to send light long distances is not very useful, in a communications environment, unless the light can be modulated to contain data. There are two main categories of modulation: analogue and digital [16]. In optical communications the preferred modulation technique is normally digital. This method was elected for the same reasons that other transmission media such as radio and copper wire have selected it, for instance the technique is resilient to noise.

One of the most popular and simplest ways of transmitting data digitally through fibre is by using On Off Keying (OOK), where the data consists of a sequence of "0"s and "1"s. When data is applied to a pulse train the absence of light within a bit slot represents a "0" and the presence of light within a bit slot represents a "1".



(a)



(b)

Figure 1-4 10Gb/s (a) Non-Return to Zero (NRZ), (b) Return to Zero (RZ), modulation formats

The modulation technique OOK, can be broken down into two further categories, Non-Return to Zero (NRZ) and Return to Zero (RZ), Figure 1-4 [17]. The NRZ modulation scheme is generally more common than the RZ format. To create a NRZ signal, data is modulated directly onto a Continuous-Wave (CW), Figure 1-4 (a). Again the presence of light ensures a "1" and the absence of light ensures a "0", with the light filling the whole length of the bit slot. Hence, when there are two simultaneous "1"s the signal level does not return to zero. With the RZ format the data is modulated onto a pulse stream, Figure 1-4 (b), usually consisting of gaussian pulses. In this scheme the intensity always returns back to zero. Both the switching devices that are to be used later in this research can only operate when RZ signals are used. Therefore, it is the RZ modulation technique that will be used for the rest of this thesis.

Other modulation schemes include Differential Phase Shift Keying (DPSK) [18, 19] and Quadrature Phase Shift Keying (QPSK) [20], which utilise RZ pulses but unlike

OOK the amplitude remains constant and the phase of the pulses is modulated with the data.

A transmitter will modulate the data onto an optical signal, which then propagates along a transmission medium until it reaches its destination. Once its destination has been reached, a receiver converts the optical data into electrical pulses ready for processing. The receiver achieves this by measuring the intensity of the light at a set timing point for each bit. Once the amplitude has been measured the receiver then has to make a decision as to whether the bit represents a "1" or a "0". To help the receiver make this decision it is provided with a decision threshold level, where pulses measured lower than the threshold level represent a "0" and pulses measured above the threshold level represent a "1". The level at which the decision threshold is set is critical to reduce the numbers of errors received, for instance if the threshold was too low then a "0" could read as a "1" and if the threshold level was too high then a "1" could be read as a "0", hence giving rise to errors.

The extinction ratio is a measure of how much power is in a "1" bit compared to the power in a "0" bit [21]. This is expressed as

$$Ex = \frac{P_1}{P_0} \qquad (1.3)$$

Where P_1 and P_0 represent the power in a "1" bit and a "0" bit respectively. To provide the maximum potential for recovery of data at the receiver, it is desirable to have an infinitely large extinction ratio. However, in reality this is not possible as most sources and modulators generate a non zero optical power output for "0" bits.

To keep the errors received to a minimum it is essential to provide the best quality signal possible. One of the fundamental reasons for a reduction in signal quality is

noise. The noise in a transmission system can come from any of the main components: the transmitter (Laser intensity noise); the transport medium (Crosstalk and Amplified Spontaneous Emission (ASE)) and the receiver (Thermal noise and Quantum noise) [22]. All of these sources of noise reduce the signal quality at the decision point and can potentially cause errors. The proportion of the signal power to noise power is measured as the Signal to Noise Ratio (SNR).

The total noise in a system is a stochastic process which is a combination of both multiplicative and additive components. Multiplicative noise components such as laser intensity noise [22] are only produced in the presence of a signal and additive noise, such as ASE, is produced independently of the presence of a signal.

If the input power to the transmission line is too low and the noise at the receiver is too high then through degradation effects, such as attenuation (section 1.4), the resultant signal present at the receiver is low enough to cause a "1" to be read incorrectly as a "0". Likewise if the input signal power is too high then non-linear effects become prominent, degrading the signal hence increasing the probability of errors (section 1.6). It is these degradation effects which require that the optical signal powers in the network are finely balanced to ensure the probability of receiving an error is kept to a minimum..

1.4. Signal degradation effects in optical fibres

When an optical signal propagates along a length of fibre the signal received is never the same quality as that transmitted. The process of signal propagation can cause degradation effects such as pulse shaping (as caused by dispersion) or nonlinearity. All of these degradation effects can contribute to the generation of errors at the receiver and thus limit the bit rate-distance product. The effect of degradation is

partially reduced through the introduction of repeaters and signal amplifiers situated at various locations along the transmission fibre. After travelling a specified distance the signal enters a repeater where the pulses are regenerated and amplified before re-transmission. Once the regenerated signal exits the repeater it will then continue its propagation along the fibre until it reaches its destination or the next repeater. Repeaters greatly add to the cost of installation and operation of a system [23]. In addition each amplifier located in the repeaters adds self-generated noise in the form of ASE and thus limits the total number of amplifiers, which can be used in a system. Therefore, it is desirable to minimise the degradation effects influencing a propagating signal, thereby increasing the distance that a signal can propagate unaided and hence reduce the number of repeaters required.

Degradation effects are classified as linear and non-linear. The former of the two includes attenuation, which occurs as a result of the losses of the fibre. Attenuation is not dependant upon the signal intensity as opposed to the non-linear effects, such as Four Wave Mixing (FWM) [24] and Self Phase Modulation (SPM) [25].

Due to the short lengths associated with the devices demonstrated in this thesis, the effects of signal propagation are not a salient consideration. However, it is necessary to be aware of the mechanisms, which affect the optical signals. This will provide an understanding of the choice of wavelengths used for telecommunications and the benefits gained from using a regenerative device.

1.4.1. Attenuation

One of the most important considerations when designing an optical based telecommunication system is attenuation. Power is lost simply through the cladding (i.e. bend loss) or through effects such as Raleigh backward scattering [23] or through

normal absorption. Every length of fibre has its associated loss that is normally measured in units of dB/km. Typical values for loss in silica in 1966 measured 1000dB/km. However, during the 1970s through constant development in the purification of silica fibres this value was reduced to approximately 0.2dB/km [26].

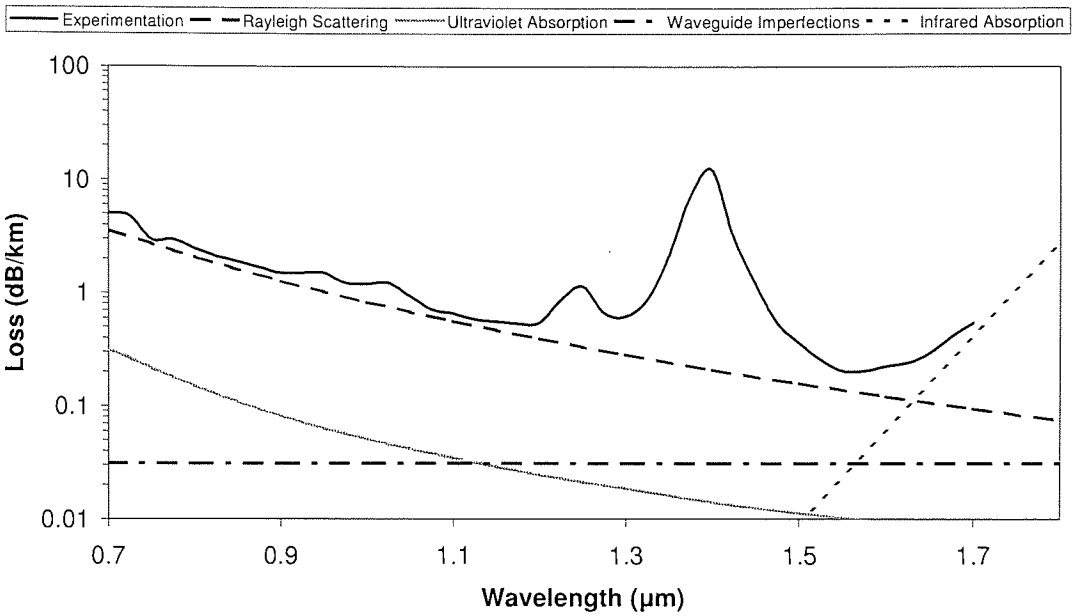


Figure 1-5 Loss spectrum of Single Mode Fibre (SMF) demonstrating wavelength dependant loss mechanisms

Attenuation is wavelength dependant, and therefore the correct wavelength must be chosen to reduce the amount of propagation loss, thus improving the efficiency of the system and reducing the amplification needed. Figure 1-5 shows a typical loss profile for SMF. The graph shows how the four main attenuation influences, Raleigh Scattering, Ultraviolet Absorption, Waveguide imperfections and Infrared Absorption change with wavelength. It is seen from the graph that the window for minimum loss is around 1550nm. The telecommunications industry widely uses wavelengths from 1530nm to 1565nm and this is the International Telecommunication Union ITU-T standard range known as the C band [27]. It is therefore around these wavelengths that the experiments contained in this thesis will be based.

1.5. Chromatic dispersion

The term "Dispersion" now refers to any effect where the components of a signal propagate along a length of fibre at different speeds. An example of dispersion is intermodal dispersion, as inherently found in multimode systems [28-30]. This is where individual modes take different paths of varying lengths through the fibre, hence reaching the receiver at separate times.

There are two main chromatic dispersion mechanisms, material dispersion and waveguide dispersion. Both types of dispersion mechanism affect the spectral components in the signal, causing pulse shaping and potentially reducing the quality of the received signal.

1.5.1. Material dispersion

Normally material dispersion is more influential than waveguide dispersion when considering a single mode system [31]. The speed of light in a fibre is dependent upon the wavelength of light and therefore each wavelength contained in the signal will arrive at its destination at a different time. This version of dispersion is not a problem if the signal had an infinitely small spectral width. Unfortunately in any practical optical fibre system every signal has a spectral width, typically limited by the data bandwidth, containing multiple wavelengths. With each wavelength arriving at different times, the shape of the pulse in the time domain is changed. Normally, when using transform limited pulses, chromatic dispersion causes the pulses to broaden, eventually causing inter-symbol interference and hence producing errors.

In a practical narrow bandwidth system, material dispersion is not an issue, as the variation in the arrival times is not sufficient to cause problems. However, in a wide bandwidth system, where the spectral width is much greater and inter-symbol

interference is a problem, lengths of dispersion compensating fibre are used to reverse the effects of material dispersion. The compensating fibre is ideally designed to have the opposite dispersion (as a function of the wavelength) of the transmission fibre and therefore it reverses the effects of the normal transmission fibre. It is worth noting that in a dispersion compensating fibre the dispersion is normally much larger than in normal SMF and only short lengths of the compensating fibre are needed.

1.5.2. Waveguide dispersion

Waveguide dispersion is normally most evident in single mode transmission and, although it contributes to pulse shaping, its impact is lower when compared to material dispersion. When single mode fibres are used, the entire signal energy is contained in one single mode with the majority of the energy propagating through the fibre's core. The remainder of the energy in the signal propagates through the cladding. It has already been discussed that for total internal refraction to occur the refractive index of the cladding must be lower than that of the core. Therefore, the signal component travelling through the core travels at a different speed to the component travelling through the cladding. Wavelength variation results in a change in the size of the mode and ultimately an alteration to the distribution of the signal between the core and the cladding. The group velocity of the signal is referred to as the "mean velocity" of the signal travelling in both the core and the cladding. The variation in the distribution (as a consequence of a change in the wavelength), causes a change to the group velocity, and ultimately an alteration to the arrival time. As with material dispersion, this variation causes pulse shaping in the time domain, increasing the probability of errors [32].

1.6. Network topology

This section explains how buffering is used in a modern high-speed network.

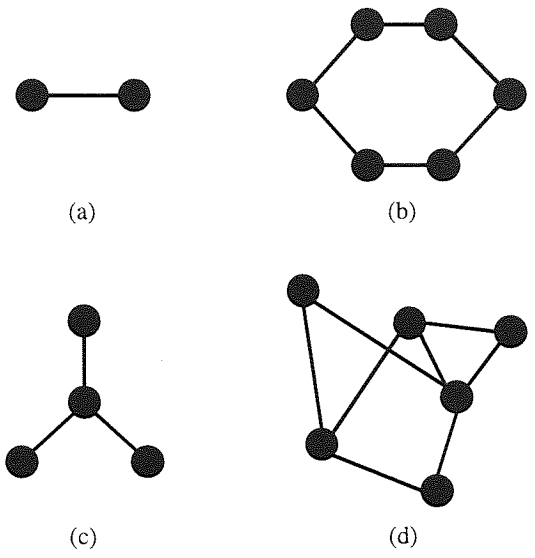


Figure 1-6 Different types of network architecture, (a) Point-to-point, (b) Ring, (c) Star, (d) Mesh

In early telecommunications systems, calls made between two users (nodes) were set up by using a single point-to-point network, where a single wire would be devoted to a single call, see Figure 1-6 (a). In this case the signal was directly sent to its final destination through a dedicated line, therefore there was no requirement to store any data and processing was kept to a minimum. The problem with this type of connection occurs when more nodes are added. Point-to-point networks have poor scalability and very quickly become complex and expensive, as additional nodes are added.

To improve the scalability of networks other architectures have been developed. These include ring, star and mesh, as shown in Figure 1-6 (b), (c) and (d) respectively [33, 34]. Of these four architectures, the mesh network possesses the greater complexity. However, as well as offering improved scalability, this method also provides more than two possible routes by which data can travel to its destination.

With the star network all communication links are routed through the central node. So if this node fails then so does the entire network. With the mesh architecture, there are normally several potential communication routes between two nodes, so a failure of a node will not affect communications between the other nodes. This improves the overall reliability of the network [35]. The disadvantage of using a mesh type architecture, is the complexity of the network management required to ensure maximum operating efficiency. For example, if a particular network node suffers high congestion, due to high demand, then the network management has to recognise this, and divert data down a different path.

In a modern high-speed communication network, calls are connected using virtual path technology. Here a single unmanageable long stream of data is split into smaller manageable frames. Once the original data stream has been split up into sections, a header is added to each packet. The header is essential as it provides vital information such as the address of the original sender and receiver, frame length and error checks [36].

In a mesh network, a frame arrives at a point where more than two network links combine. Once this has happened, the network management decides whether the frame has reached its final destination, and if not, which output path it should take. Making these decisions, the network router (located at each junction), is one of the most important components in a modern network.

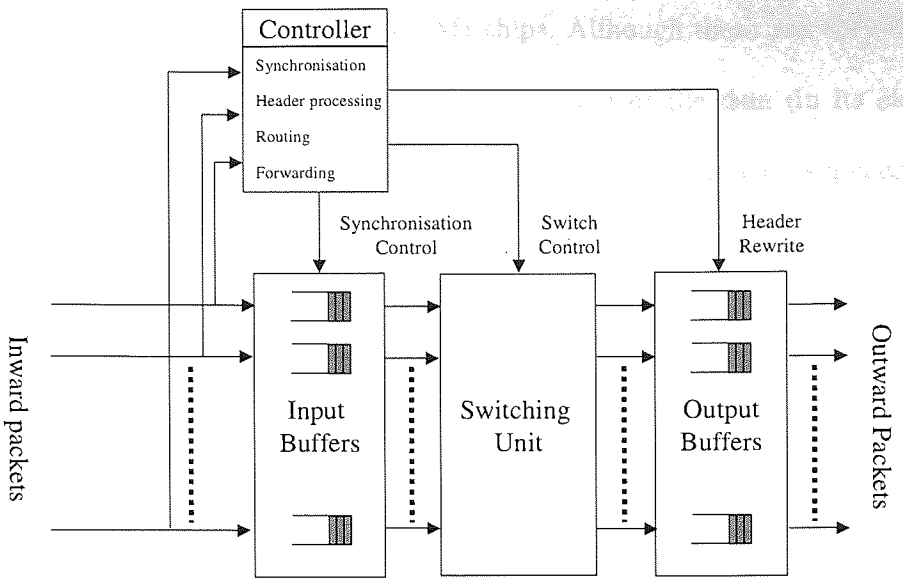


Figure 1-7 A schematic of a network node showing the Switching unit, Controller, Input and Output buffers

The schematic shown in Figure 1-7 is of a typical router. The router consists of four main sections: the controller, input/output buffers and the switching unit. Once a data packet arrives at the router, the packet is split into two, separating the header and the payload. The information contained in the header is then sent to the controller. While the header is waiting to be processed, the remaining section of the original packet (which contains the payload) is stored in the input buffer. After the header has been processed and the output path is determined, the payload data exits the input buffer and the switching unit directs the payload to the appropriate section in the output buffer. At this point a new header is added to the packet where it waits in the output buffer, until the destination path becomes clear [37]. Throughout the whole process it is essential to keep the data synchronised. This is to ensure that the packet is completely switched and the new header is temporally aligned with the data frame.

The input and output buffers are one of the most crucial components in a router. Without them, there would be nowhere to store the payload whilst the header is being processed. This provides the potential for lost packets. Currently the buffers consist of

electronic Random Access Memory (RAM) chips. Although these are very flexible, and the technology well known, the actual processing of the data (in its electrical form) is time consuming and energy inefficient [38]. Therefore, there is a need for an all-optical alternative [39].

1.7. Types of optical memory

Unfortunately, it is very difficult to stop and store a photon, Consequently, another method of storing data optically has to be found. There are two main categories of optical memory, these are pulse preserving and pulse regenerating.

1.7.1. Pulse preserving

The simplest method of storing data optically is to send the signal down additional lengths of transmission fibre (the further a signal has to travel the longer it takes to reach its destination). This type of buffer, commonly known as a passive delay line, is adequate for short delay periods [40]. However, extended storage periods are limited by the signal degrading effects normally associated with long distance transmission, such as dispersion and attenuation. Another disadvantage with the passive delay line is the access time. Once the signal is sent down a length of fibre the data cannot be accessed until the other end is reached. Therefore, with this type of optical memory the storage time cannot be dynamically changed, once storage is taking place. Additional storage time can only be achieved by passing the signal through another length of fibre.

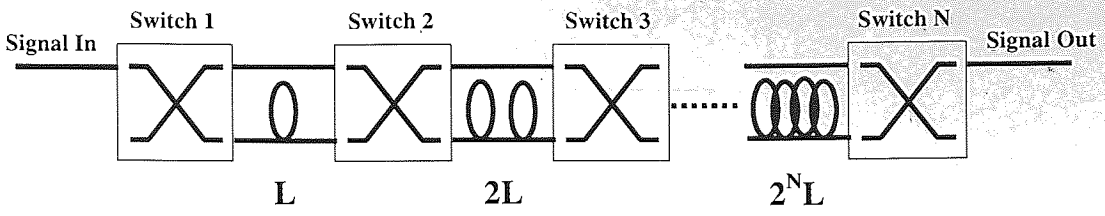


Figure 1-8 A feed-forward tuneable delay line using 2 x 2 cross switch

An improvement of the simple passive delay line is obtained by combining multiple passive delay lines with 2 x 2 optical cross switches, as shown in Figure 1-8 [41]. The schematic shows an example of a programmable optical delay line in the configuration of a feed-forward tuneable delay line. In a device such as this, the packet is delayed by sending it through a combination of varying lengths of fibre. With the use of optical 2 x 2 cross switches in this configuration, the maximum delay length would be $(1+2....+2^N)L$ or $(2^{N+1}-1)L$. This allows the possibility to delay the signal in time from 0 to a maximum of $(2^{N+1}-1)nL/c$ in steps of nL/c, where n is the refractive index of the fibre and c is the speed of light in a vacuum [42].

The main disadvantage associated with the feed-forward technique is the limited storage time. Once the signal has reached the end of the device no further delay time is applied. It is also impossible to apply additional short lengths of delay time < L, due to the inline configuration of ever increasing lengths of fibre. This means that the total delay time required to be imposed upon a signal needs to be known before the packet enters the device.

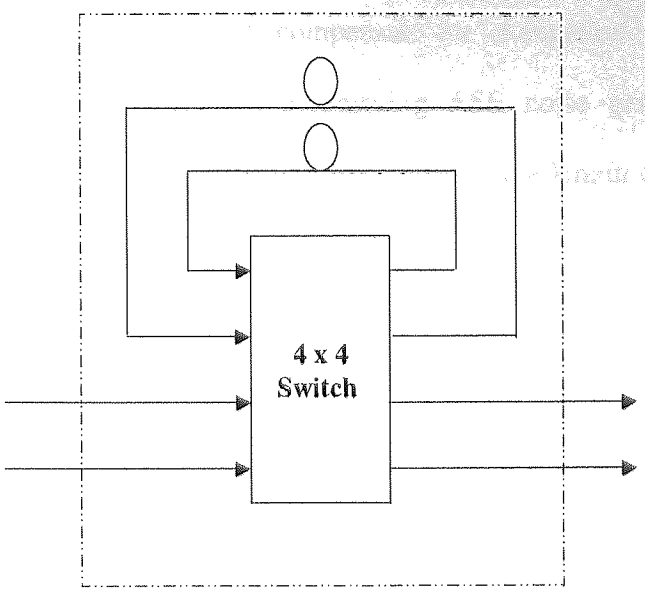


Figure 1-9 A feedback delay line architecture using a 4x4 cross connect switch

An improvement over the feed-forward programmable delay line would be the feedback delay line as shown in Figure 1-9 [43, 44]. Storage is achieved by using a switch to direct an incoming signal along a delay line. Unlike with the feed forward architecture, the output of the delay is looped back into the input of the switch. This feedback enables the switch to redirect a signal, exiting from the output of the delay line, back into the input, should further storage time be required. The advantage this architecture has over the feed-forward delay line is that the feedback architecture is dynamic and therefore the signal is stored until it is required. In addition if the loop were made as small as possible (the maximum length of the packet is determined by the length of the loop) then the access time would be equal to the length of the packet.

The problem with all the pulse-preserving techniques concerns the maximum time that the data can be stored for. Effectively, long-term storage is achieved by sending a signal over a long distance, for example 10μs of storage time requires 2km of fibre. Therefore the same effects, which limit long transmission distances, such as attenuation and chromatic dispersion, limit the maximum storage times. Introducing

an amplifier into the delay line can compensate for attenuation. However, as the storage time increases so does the propagating ASE noise generated from the amplifiers. With the feedback architecture the choice in the length of the feedback is critical. The smaller the length of the feedback the quicker the signal exits the delay line, which is desirable in the terms of access time. The trade off with the improved access time is the number of times the signal has to pass through the switching module per length of storage time. The switching module generally has an associated high loss and therefore the more times the signal has to pass through the switching module per delay time the more amplification is needed in the feedback loop.

1.7.2. Pulse regeneration

The alternative to the pulse preserving technique is to regenerate the pulses. Ideally, the data is 3R regenerated after a certain period of time (3R is classed as resetting the pulse shape, pulse energy and resynchronisation of the timing jitter. Thus an EDFA is a 1R regenerator as it only resets the pulse energy). By refreshing the pulses the effects of long transmission lengths are reduced to potentially negligible levels. There have been a number of different types of regenerative memories proposed, which include an all-optical regenerative memory using multiple devices [45, 46] and an all-optical all-fibre shift register with an inverter [47, 48]. However these either use multiple loops or are inverting (The classification "inverting" and "non-inverting" refers to the method the device uses to store the data and will be described later in this thesis). In this thesis we will concentrate on a single loop, which is non-inverting. Previously a non-inverting optical memory has been demonstrated [49, 50] using an ultra fast non-linear interferometer configuration, however the operation of this device requires long lengths of birefringent fibre that would make hybrid integration difficult. The device studied in this thesis is a new non-inverting optical memory

device that has the advantage of being fully 3R regenerative and provides the potential for hybrid integration.

1.7.3. Slow light

One area of potential research in optical buffering, which uses a different technology, is to use a slow light scheme. As its name suggests, slow light exploits the technology of reducing the group velocity of light. There are two main techniques for achieving this; coupled resonant structures (CRS) and Electromagnetically Induced Transparency (EIT) [51]. These techniques have been demonstrated to reduce the group velocity down to 17m/s using an ultra cold atomic gas [52]. Although great progress has been made in this technology it is still in its infancy and many issues need to be addressed before this could become a potential solution [53].

1.8. Basic operation and types of interferometers

The interferometer is one of the most important devices used in optics. It comes in many forms and has many uses, both in optical communications and non-communications applications. One example of an interferometer in a communication application includes a Michelson interferometer, which is widely used for all-optical DPSK to OOK conversion [54]. The interferometer which is to be used in this thesis is the Mach-Zehnder Interferometer (MZI) and its variant the Sagnac loop mirror.

1.8.1. The Mach-Zehnder interferometer

The MZI is the simplest form of interferometer and is favoured as the preferred device for hybrid integration [55, 56]. The device consists of two couplers, which are connected together as shown in

Figure 1-10.

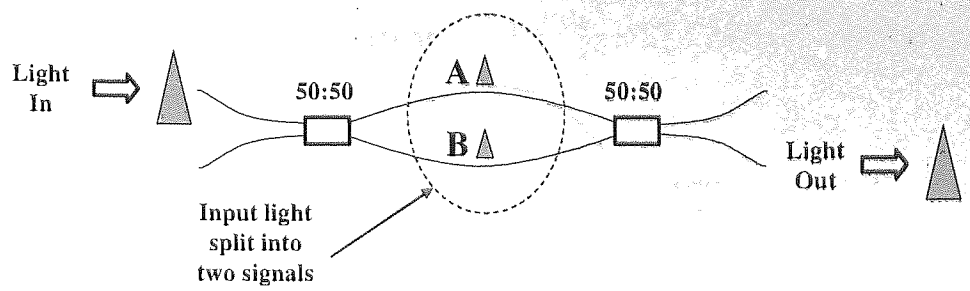


Figure 1-10 Mach Zehnder interferometer. Light entering the device through the first 50:50 coupler is split into two identical signals A and B. These signals propagate through two identical arms and recombine in the second 50:50 coupler to exit solely out of one port.

After entering the first coupler through one of the input ports, the optical signal is split into two equal signals A and B (providing a 50:50 coupler is being used). The resultant optical signals propagate along each of the interferometer arms until they reach the second coupler, see

Figure 1-10. Providing the two arms of the interferometer are identical, both signals A and B recombine in the second coupler and exit solely through one output arm. It is the effects of the conservation of energy and the result of (constructive or destructive) interference, which takes place in the two couplers that makes this possible. Introducing a differential π phase shift between the two arms will switch the signal from one output to the other. The theory of the interferometer shall be discussed later in this section where the proof of principle will be mathematically demonstrated.

1.8.2. Sagnac loop mirror

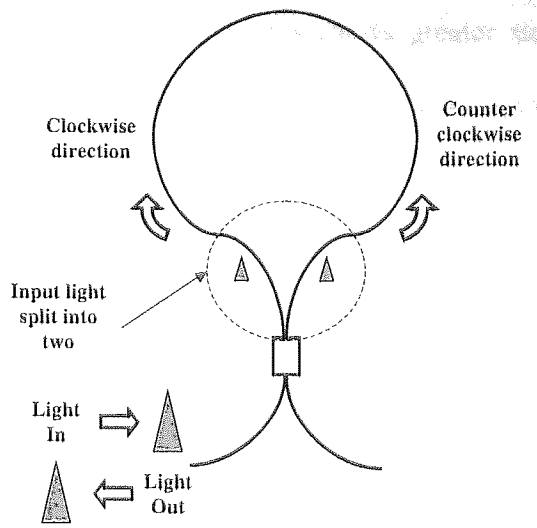


Figure 1-11 Sagnac loop mirror. Light entering the input port will split into two, propagate around the loop and recombine in the coupler and exit through the initial input port

The Sagnac loop mirror is another kind of interferometer, Figure 1-11. This type of interferometer has many uses, such as all-optical demultiplexing and high speed sampling oscilloscopes [57, 58]. The operating principles are exactly the same as the MZI, however the layout is different. Instead of two couplers in series only one coupler is used, with outputs connected together to form a loop.

Light injected into the loop mirror is split into two signals. These then propagate separately around the loop in clockwise and anticlockwise directions until they return to the coupler. As before, interference within the coupler means that the light will then exit solely through the port which it originally entered (hence the signal is reflected thus the device is called a loop mirror). As with the MZI, applying a differential π phase shift between the two counter propagating pulses causes the output to switch from one arm to the other.

In experimental situations where the devices are made of discrete components, the loop mirror is the preferred option, as this shows greater stability. With the MZI unwanted changes in one of the arms, e.g. caused by thermal expansion or vibrations, will generate an unwanted random differential phase shift, thus reducing the stability of the device. For this reason the use of MZI's is limited to devices that have been constructed using Hybrid Integration technology. With the Sagnac loop mirror the two signals propagate along the same length of fibre, therefore any environmental effects applied to the fibre are seen equally by the two pulses (this is strictly only true for low frequency variations, the loop is still susceptible to effects where the fluctuation frequency is larger than one over the round trip time of the loop). It is for this reason that the majority of the experimental work will be carried out using a Sagnac loop mirror interferometer.

1.8.3. Interferometer theory

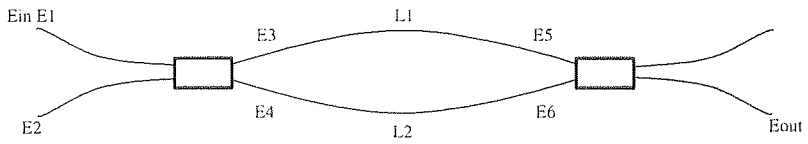


Figure 1-12 Mach-Zehnder interferometer (MZI)

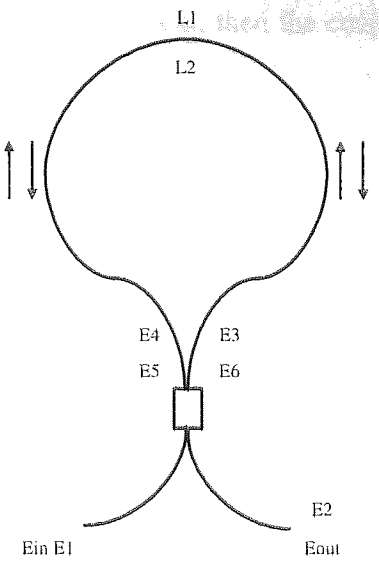


Figure 1-13 Sagnac loop interferometer

In this section we provide the mathematical equations describing the principle of the interferometer. Although the theory will be based around a MZI, for clarity, it can also be applied to the Sagnac loop mirror see Figure 1-12 and Figure 1-13

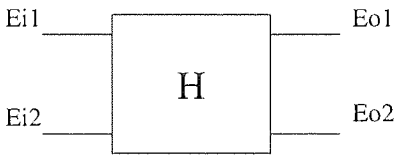


Figure 1-14 Schematic of a simple 2 x 2 coupler with two inputs and two outputs

Figure 1-14 shows a 50:50 coupler as a system, where Ei1 and Ei2 represent the electrical fields at the input and Eo1, Eo2 correspond to the resultant electrical fields at the outputs. Using matrices the coupler can be represented as

$$\begin{bmatrix} Eo1 \\ Eo2 \end{bmatrix} = H \begin{bmatrix} Ei1 \\ Ei2 \end{bmatrix} \qquad (1.4)$$

Here H represents the response of the system. To satisfy the conservation of energy the differential phase shift applied to the resultant output signals must be $\pi/2$ see

appendix C. If α is the coupling coefficient, then the coupler response can be written as

$$H = \begin{bmatrix} (\alpha)^{\frac{1}{2}} & (1-\alpha)^{\frac{1}{2}} e^{i\frac{\pi}{2}} \\ (1-\alpha)^{\frac{1}{2}} e^{i\frac{\pi}{2}} & (\alpha)^{\frac{1}{2}} \end{bmatrix} \qquad (1.5)$$

Where $(\alpha)^{\frac{1}{2}}$ and $(1-\alpha)^{\frac{1}{2}} e^{i\frac{\pi}{2}}$ represent the proportional of the input signal coming from the outputs. Therefore replacing H into the original coupler equation (1.4) The resultant matrix can be expanded to give

$$Eo1 = (\alpha)^{\frac{1}{2}} Ei1 + (1-\alpha)^{\frac{1}{2}} e^{i\frac{\pi}{2}} Ei2 \qquad (1.6)$$

$$Eo2 = (1-\alpha)^{\frac{1}{2}} e^{i\frac{\pi}{2}} Ei1 + (\alpha)^{\frac{1}{2}} Ei2 \qquad (1.7)$$

In the case of the MZI and the Sagnac loop mirror the input Ei2 is zero so we can simplify the equations as follows

$$Eo1 = (\alpha)^{\frac{1}{2}} Ei1 \qquad (1.8)$$

$$Eo2 = (1-\alpha)^{\frac{1}{2}} e^{i\frac{\pi}{2}} Ei1 \qquad (1.9)$$

Now that we have the full equation for a single coupler we will now look at the interferometer configuration. In this case the inputs to the second coupler are the outputs from the first coupler, to create an interferometer. Any differential phase shift seen between the two MZI arms will be represented as Ø, see Figure 1-15.

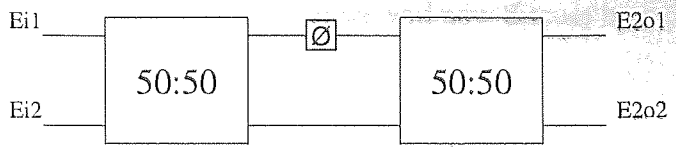


Figure 1-15 Schematic of an interferometer, two 2 x 2 couplers connected output to input.

With H_2 representing the response of the second coupler the output of the interferometer can be represented as

$$\begin{bmatrix} E_2o1 \\ E_2o2 \end{bmatrix} = H_2 \begin{bmatrix} Eo1 \\ Eo2 \end{bmatrix} = \begin{bmatrix} (\alpha)^{\frac{1}{2}} & (1-\alpha)^{\frac{1}{2}} e^{i\frac{\pi}{2}} \\ (1-\alpha)^{\frac{1}{2}} e^{i\frac{\pi}{2}} & (\alpha)^{\frac{1}{2}} \end{bmatrix} \begin{bmatrix} (\alpha)^{\frac{1}{2}} Ei1 \\ (1-\alpha)^{\frac{1}{2}} e^{i(\frac{\pi}{2}+\varnothing)} Ei1 \end{bmatrix} \quad (1.10)$$

Where θ allows for any additional differential phase shift on the input Eo2 including any additional phase shift required for switching. The matrix can then be simplified to

$$\begin{bmatrix} E_2o1 \\ E_2o2 \end{bmatrix} = \begin{bmatrix} \left[\alpha + (1-\alpha)e^{i(\pi+\varnothing)}\right] Ei1 \\ \alpha^{\frac{1}{2}}(1-\alpha)^{\frac{1}{2}} \left(e^{i\frac{\pi}{2}} + e^{i(\frac{\pi}{2}+\varnothing)} \right) Ei1 \end{bmatrix} \quad (1.11)$$

After multiplying by the complex conjugate field, the powers are given by

$$|E_2o1|^2 = \left[\alpha^2 + (1-\alpha)^2 + 2\alpha(1-\alpha)Cos(\pi+\varnothing)\right] Ei1^2 \quad (1.12)$$

$$|E_2o2|^2 = \left|2\alpha(1-\alpha) + 2\alpha(1-\alpha)Cos(\varnothing)\right| Ei1^2 \quad (1.13)$$

As we can see with a 50:50 coupler and a phase shift of $\varnothing=\pi$ would result in the switching of the output ports from port 2 to port 1.

1.9. Non-linear elements

Previously we have discussed how a differential phase shift of π applied to one of the arms of an interferometer would cause the output of the device to switch from one

output port to the other. In the next section we will now discuss how the π phase shift is accomplished.

In a fibre there are two main ways of inducing a phase shift, SPM and Cross Phase Modulation (XPM). SPM is a result of the Kerr non-linearity effect, where the refractive index of fibre is dependant upon the intensity of the signal passing through it [59]. The intensity dependant refractive index can be calculated as:

$$n(E) = n + n_C I = n + n_C \frac{P}{Aeff} \qquad (1.14)$$

Where n is the ordinary refractive index of the fibre and n_C is non-linear index co-efficient. The signal intensity I is equal to the signal power P divided by the effective area A_{eff}. In most fibres the non-linear refractive index has a typical value of 2.2 to $3.4 \times 10^{-8} \mu m^2/W$. Therefore, to use the Kerr non-linearity to generate a π phase shift, in a propagating signal, would require long lengths of fibre and high input powers.

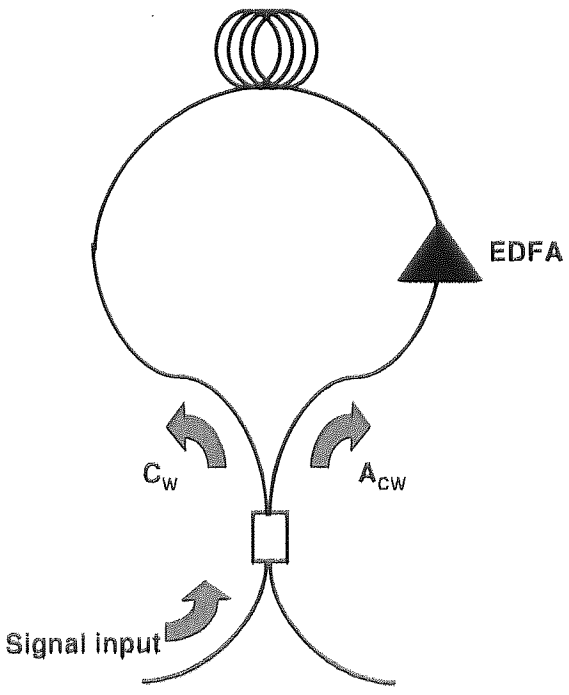


Figure 1-16 Non-linear Amplified Loop Mirror (NALM)

An example of a device utilising SPM is the Non-linear Amplified Loop Mirror (NALM). Figure 1-16 shows a Sagnac loop mirror in the configuration of a NALM. The signal entering the loop mirror is separated into two components which travel in a clockwise (C_W) and anticlockwise (AC_W) direction. An amplifier, which is typically a bi-directional Erbium Doped Fibre Amplifier (EDFA), is located in an offset position from the centre of the loop [60]. The amplifier is used to unbalance the loop and allows self-switching to take place. In the configuration described in Figure 1-16 the C_W signal will not enter the amplifier until it has passed through the majority of the fibre. In contrast the AC_W signal will enter the amplifier first so that it will have a greater intensity in the fibre than the C_W signal and thus experience a greater amount of SPM. If this difference in the amount of induced SPM is sufficient enough to generate a full differential π phase shift, then the signal will be transmitted instead of reflected. This configuration is used mainly for noise reduction [61].

The NALM is a self-switched device where the power of the input signal determines the level of switching. A controlled switched device provides the ability for the signal to be switched by a separate control signal. An example of this type of device is the Non-linear Optical Loop Mirror (NOLM) as shown in Figure 1-17. To generate the differential π phase shift the NOLM uses Cross Phase Modulation (XPM), also derived from the Kerr non-linearity. XPM is generated through the same non-linear effects as SPM, with the exception that a second pulse (control pulse) is propagated in parallel with the signal.

When a control pulse is used, both the signal and the control pulses propagate along the fibre at precisely the same time and speed (providing they are the same wavelength or have the same group velocity). The signal co-propagating with the

control pulse experiences a long interaction length whereas, the counter-propagating signal sees only a very brief interaction with the control pulse and this leads to a differential phase shift. In Figure 1-17 the NOLM is shown with two ports which are used to inject and remove the control pulse.

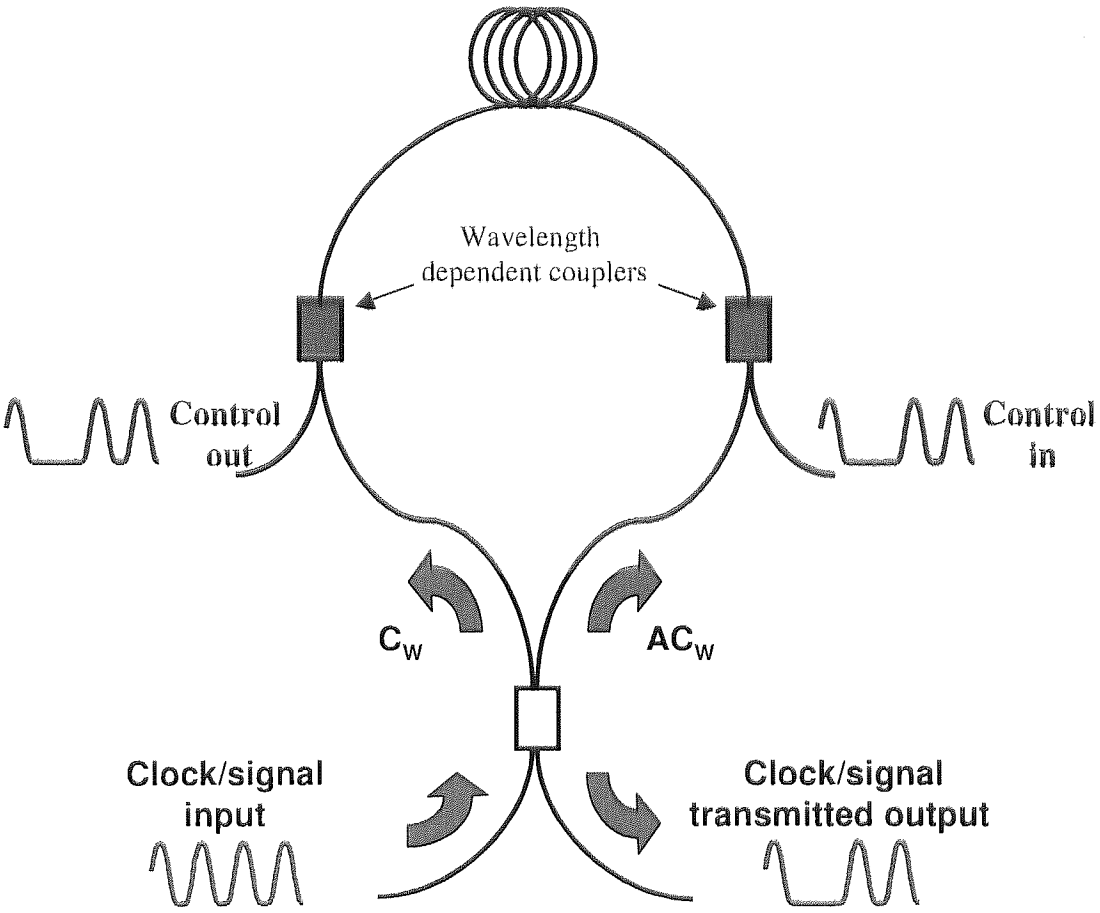


Figure 1-17 Non-linear Optical Loop Mirror (NOLM) using separated wavelengths for the control and clock signals

The main advantage of using this method is the potentially high switching speeds. The response time of silica is in the femtosecond region and devices using this technique have already been demonstrated to successfully operate at speeds of up to 640Gbits/s [62]. However, there are many disadvantages associated with such a device. As with the NALM, the low non-linearity of the fibre means that the device requires high pulses energies and long lengths of fibre. Typically 1km of fibre is required for

40Gbits/s operation using High Nonlinearity Dispersion Shifted Fibre [63]. For complete switching it is essential that the control pulse propagates along the non-linear fibre in complete temporal alignment with the signal pulse. Any slight misalignment between the pulses will reduce interaction length, and hence result a reduction in the transmitted output power (providing the differential phase shift is less than π). This makes the device susceptible to both walk-off and timing jitter. Broadening the pulses will reduce this sensitivity however, although the energy of the broader pulse remains the same the peak power is reduced. This reduction in peak power decreases the XPM effect, reducing the switching efficiency.

For optical processing to become a true alternative to electronics the power requirement must be low and the physical size of the device minimised. A non-linear element, which satisfies these requirements, is a Semiconductor Optical Amplifier (SOA). The SOA has been successfully used in both the Sagnac loop mirror and the MZI configurations [64, 65] and will be demonstrated in both configurations in this thesis.

1.10. The Semiconductor Optical Amplifier

The main aim of any amplifier design is to increase the input signal strength with minimal loss of quality. Optical amplifiers are split up into two basic categories, Optical Fibre Amplifiers (OFA) and SOAs. The OFA has a much lower level of nonlinearity, when compared to SOAs, reducing effects such as chirp and SPM. The SOA is a highly non-linear device and although this causes problems when operating as an inline amplifier, it does allow for effective non-linear switching [66-68]. A typical device length ranges from 1 to 2mm in length (although ultra-long SOAs have been demonstrated [69]). As a consequence of the high nonlinearity, it is still possible

to generate a π phase shift. In addition the power required for switching is also greatly reduced, when compared to a fibre equivalent. The small physical size and material properties of the SOA also makes hybrid integration possible.

Figure 1-18 (a) Fabry-Perot (FP-SOA), (b) Travelling Wave TW-SOA

There are two types of SOAs: the Fabry-Perot (FP-SOA), Figure 1-18 (a), and the Travelling Wave (TW-SOA), Figure 1-18 (b). In the FP-SOA device, high reflectivity coatings are used at either end of the active region, causing light to be reflected back into the device. By generating multiple passes of the signal through the active region large values of gain are achieved with low bias currents. The problem associated with this type of device, however, is its susceptibility to fluctuations in bias current, temperature and polarisation. The device also suffers from ripples in the gain curve caused by the reflective facets. Unlike the FP-SOA, the TW-SOA uses anti reflective coatings which result in the signal passing through the device once only. Although high bias currents are needed, when compared to the FP-SOA, the device has greater stability. It is for this reason that the TW-SOA has replaced the FP-SOA for most practical applications [70] (it is this type of SOA which is used in the experimentation and therefore will be the subject of discussion from this point).

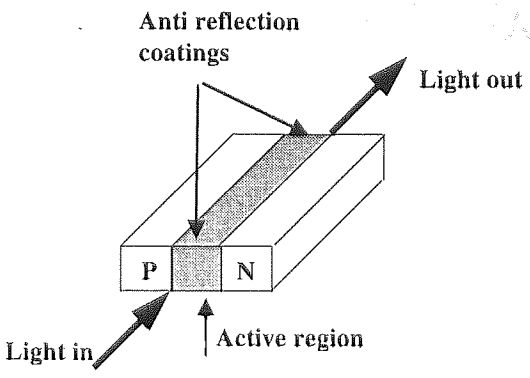


Figure 1-19 PN junction of an SOA showing the active region and the anti-reflection coatings

An SOA is constructed from two semiconductors, an n-type and a p-type, structured in a PN junction, see Figure 1-19. The depletion layer formed between the two semiconductor materials acts as an active region and it is this active region which forms the SOA. Amplification is achieved by passing the signal through the active region, which has a typical length of 1 to 2mm. As the amplifier is bi-directional the signal can enter the active region from either end. Using the same amplification process as found in fibre based amplifiers, the signal propagates through the active region and is amplified through stimulated emission. SOAs differ from fibre based amplifiers in the way that they achieve population inversion. Instead of using ions in varying energy states SOAs use carriers consisting of electrons or holes.

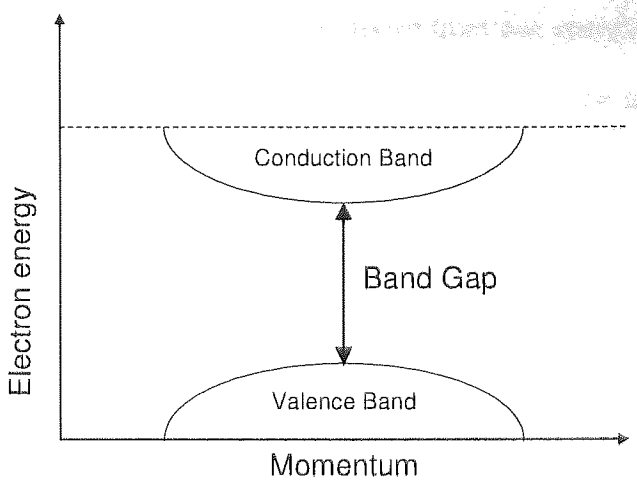


Figure 1-20 Showing the energy bands of an AGaS SOA, when sufficient energy is absorbed by the electron the electron will move from the Valence Band to the conduction band.

There are two energy bands for semiconductor materials: the lower energy level is referred to as a valence band and the higher being a conduction band, see Figure 1-20. When sufficient energy is absorbed by an electron located in the valence band the electron will move from the valence band to the conduction band. The band gap represents the minimum quantity of energy required to make this transition possible. Whilst the electron is in the conduction band the electron is known as a carrier. The carrier density, which determines the refractive index of the SOA and ultimately the phase shift applied to a signal, refers to the number of carriers located in the conduction band (per unit volume).

Gain is generated when a photon of sufficient energy and wavelength causes an electron/carrier to transit from the conduction band to the valance band, in a process known as stimulated emission. The resultant transfer in energy states will cause the electron to release its energy in the form of a photon. This released photon will be identical to the inducing photon in frequency, phase and direction. In such a device one of the most critical features is the band_gap. This defines the quantity of

transferred energy needed for the electron to move from one energy state to the other and hence defining the maximum wavelength at which gain can be achieved.

Other than stimulated emission a photon can be released randomly through a process called spontaneous emission. In this process the carrier will spontaneously move from the conduction band to the valence band causing a photon to be released, which has no correlation with the signal. After being spontaneously released, the released photons propagate through the remainder of the active region and as they travel they initiate stimulated emission. This stimulated emission causes the noise signal, consisting of the spontaneously released photons, to be amplified. The resultant signal, which is emitted by the SOA, is called ASE.

1.10.1. Wavelength conversion

In multipath networks the ability to transfer data from one wavelength to another is becoming more and more essential. In the past, wavelength conversion was achieved by converting the optical signal to an electrical signal and then converting the electrical signal back into an optical signal at the final desired wavelength. The cost and complexity of such Optical Electrical Optical (OEO) conversion lead to research into other technologies including SOAs [71].

When a signal passes through an SOA the carrier density is depleted, reducing the gain available in the amplifier. Therefore, any subsequent signals entering immediately after, before the SOA has recovered, will not be exposed to the full gain of the amplifier. This characteristic of Cross Gain Modulation (XGM) can be harnessed to produce wavelength conversion.

The SOA plays the role of an optically controlled gate; transferring data stored on one signal, the "control", to another signal, the "probe". The probe normally consists of

RZ pulses set at a different wavelength to the control signal, which is typically an RZ signal containing data. The probe and the control signals are injected into the SOA with the probe being slightly delayed, relative to the control, to provide the maximum effect of XGM. In this setup an inverted copy of the data is applied to the probe. Where a pulse is present in the control pulse the probe records a "0" and where there is an absence of a control pulse the probe records a "1", hence inverting the signal.

There are two modes of operation with respect to control and the signal pulses: co-propagation and counter propagation. In the case of co-propagation, the probe must be of a different wavelength or polarisation so that the signals can be separated by filtering. For counter propagation the signal and the probe enter the SOA from two different sides, hence there would be no need for filtering, so the same wavelength could be used. Although, this would not provide any wavelength conversion it would provide a basic not gate function.

An alternative method of generating wavelength conversion is to use FWM. This is a non-inverting method that can be easily demonstrated using highly non-linear fibre such as Dispersion Shifted Fibre (DSF). However, this fibre technique requires relatively large lengths of fibre and high power. As mentioned previously, an SOA has a much greater value of non-linearity than a fibre so that FWM can be easily achieved over short distances using low power. The three signals have wavelengths related by the following equation

$$\frac{1}{\lambda_{Pout}} = \frac{1}{\lambda_P} + \left(\frac{1}{\lambda_P} - \frac{1}{\lambda_{In}} \right) \qquad (1.15)$$

Where λ_{In}, λ_P and λ_{Pout} are the data input signal, probe signal and resultant signal wavelengths respectively. From Equation (1.17) the output wavelength is dependent on the input signal wavelength. Therefore, constant tuning of the probe signal is required to keep the output wavelength constant. Additionally, the use of filters, required to filter out the signal, makes implementation complex [72].

1.10.2. Basic SOA equations used for modelling an SOA in a loop mirror

As discussed in an earlier section the phase shift, applied to a signal entering an SOA, is dependant upon the SOA's carrier density. A simple rate equation for the carrier density N is given by [73]

$$\frac{dN}{dt} = \frac{I_f}{eAl} - \frac{N}{\tau} - \frac{P(t)\Gamma g}{h\nu A}(N - N_T) \qquad (1.16)$$

Where the first term I_f represents the current injection, e the unit electric charge, A the cross sectional area of the active region and l the device length. The second term represents the number density dependant loss, via spontaneous emission, through the carrier lifetime τ. The final term accounts for the loss through optical pumping where, P is the optical input power, Γ is the confinement factor, g is the gain coefficient, $h\nu$ the photon energy and N_T is the carrier density at which transparency would be achieved (transparency is defined as the point where an input signal would undergo no loss or gain within the SOA). Without any incident optical power the carrier density will eventually reach a state of equilibrium (SOA is fully recovered), which is represented as N_0 and can be defined as

$$N_0 = I_f \tau / eAl \qquad (1.17)$$

Let n = $(N-N_T)/N_T$, then equation (1.16) can be written as

$$\frac{dn}{dt} = K - \frac{n}{\tau} - \alpha P(t)n \qquad (1.18)$$

Where

$$K = \left(\frac{No - N_T}{\tau N_T} \right) \quad \text{and} \quad \alpha = \frac{\Gamma g}{h\nu A} \qquad (1.19)$$

In the numerical simulations the optical pulses are represented as Dirac delta functions, and can be expressed as

$$P = \sum_j Ej\,\delta(t - jT), \qquad (1.20)$$

where T is the time between pulses and E_j is the energy in each pulse. By using Dirac delta functions all pulse shaping effects, generated as the pulses propagate through the SOA, are ignored [73]. This is a valid assumption provided that the effective recovery rate of the SOA is greater than the pulse width. There are two states, which the SOA undergoes: when there is a pulse and when there is not. From the equation (1.18) the first state where P=0 can be solved to obtain the carrier density n^-

$$n^- = K\tau(1 - e^{\frac{-t}{\tau}}) + n^+ e^{\frac{-t}{\tau}} \qquad (1.21)$$

In the simulation t represents the time elapsed since the last pulse transited the amplifier and n^+ represents the carrier density immediately after the last pulse. The second state involves a single pulse entering the SOA thus, depleting the carrier density n^+ which again is generated from equation (1.18). To give

$$\frac{dn}{dt} = -\alpha n E \delta(t - jT) \qquad (1.22)$$

Which when solved gives n^+ as

$$n^+ = n^-(e^{-\alpha E}) \qquad (1.23)$$

In a loop mirror configuration, if the refractive index in the SOA is linearly dependent upon the SOA carrier density then the phase difference experienced by the two propagating pulses can be obtained as

$$\theta = \Theta(n^{cw} - n^{ccw}) \qquad (1.24)$$

where n^{cw} is the carrier index experienced by the clockwise pulse, n^{ccw} is the carrier density experienced by the counter clock wise pulse and

$$\Theta = \frac{2\pi}{\Gamma n_{eh} l \lambda}, \qquad (1.25)$$

where n_{eh} is the constant of proportionality relating the refractive index to the carrier density and λ represents the incident light wavelength.

By combining and simplifying the equations for reflection and transmission (1.12) and (1.13) we get

$$R = \frac{1}{2}(1 + \cos\theta) \text{ and } T = \frac{1}{2}(1 - \cos\theta) \qquad (1.26)$$

(Assuming that a coupling ratio of 50:50 is used).

1.11. Discussion

In this initial chapter we have covered basic fibre optic principles ranging from how light propagates along a fibre to the linear and non-linear effects which the light is exposed to during its transmission. Discussions were then made regarding the requirement of buffering in a modern high-speed optical network. Varying types of possible storage techniques have been studied with comparisons to the main advantages and disadvantages.

The majority of the work undertaken in this thesis is based around an optical interferometer, therefore various types of interferometer have been discussed and the basic mathematical principles have been shown. It has been shown how a nonlinear element included in an interferometer could be used for switching. Multiple types of possible non-linear elements have been analysed. Taking into consideration the advantages and disadvantages of the non-linear elements the SOA will be used in all experimental work.

To promote understanding, the construction and operation of an SOA has been discussed and basic theoretical and numerical considerations have been made. All these components will be combined in the next chapter where we will discuss the Terahertz Optical Asymmetric Demultiplexor (TOAD), which will form the basis of the initial all-optical regenerative memory experiment.

2. Terahertz Optical Asymmetric Demultiplexer proof of principle and setup

2.1. Introduction

In the previous chapter we looked at varying types of interferometers and the associated non-linear elements. In this thesis the experimental work will be based around two types of interferometer, the MZI and the Sagnac loop mirror. Although both configurations have advantages and disadvantages, as discussed earlier, the Sagnac loop mirror will be the main device under study. Accompanying the Sagnac loop mirror, the non-linear element will be provided by an SOA [74]. This combination of an SOA in a Sagnac loop mirror has been used for many applications [75-77] commonly referred to as a TOAD [78]. The TOAD is well known for its all-optical regenerative capabilities [79, 80]. To gain full understanding of the optical memory demonstrated in this thesis, it is imperative to fully comprehend the operation of the TOAD. Therefore, in this chapter we look at both the operating principles of a TOAD and describe some of the methods used in constructing and characterising the experimental device.

2.2. The loop mirror

Forming the basis of the TOAD is a Sagnac loop mirror (as described section 1.8). A signal enters the coupler, located at the base of the loop and is then separated into two equal signals. These signals propagate around the loop in opposite directions until they return to the coupler. Upon re-entering the coupler the signals then interact with each other and experience destructive and constructive interference. If the loop is perfectly balanced, the loop will act as a mirror and all the light will be directed out of the port which it originally entered (also known as the reflected port). It is worth

noting that for a loop to be perfectly balanced, the coupler (located at the base of the loop) would have to be exactly 50:50 and as these only exist in theory any experimental loop would not be perfectly balanced. In the case of a TOAD, the signal entering the base of the loop is usually in the form of a constant stream of RZ pulses. This signal will be referred to as the clock from this point forward.

2.3. *Controlled switching configuration*

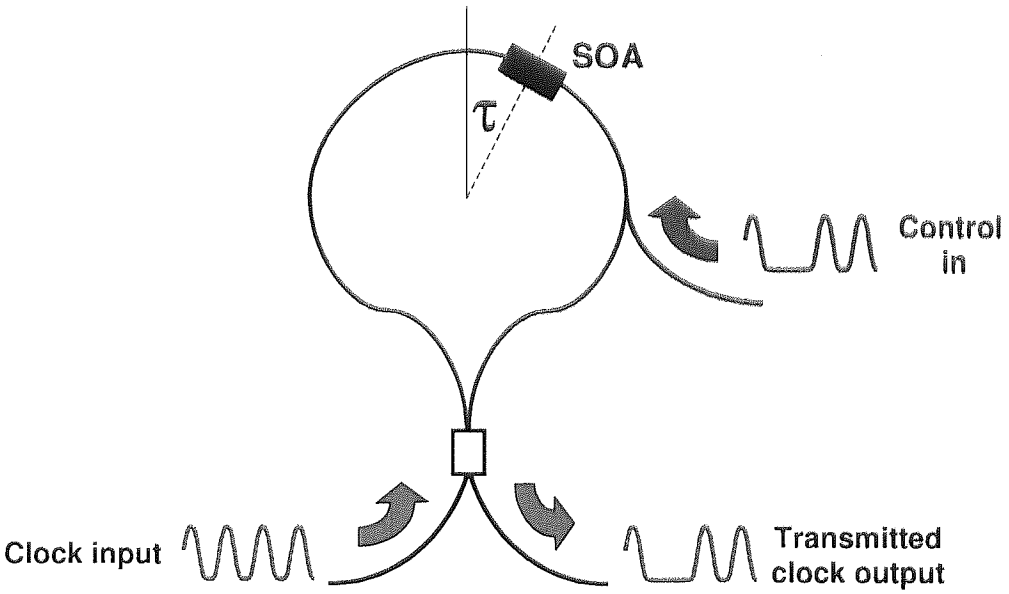


Figure 2-1 Controlled switching configuration using the two different wavelengths for the clock signal. The control signal separation is achieved using a bandpass wavelength filter on the output

In a similar way to a NOLM, a TOAD is a device that allows a control signal to decide whether the clock pulses (contained in the clock signal) will be reflected or transmitted. The control signal, consisting of an RZ signal modulated with data, is injected into one side of the loop through a coupler, shown in Figure 2-1. The offset of the SOA from the centre of the loop τ will ensure that the two propagating clock pulses (C_W and AC_W) arrive at the SOA at different times.

When there is no control pulse present, the propagating clock pulses navigate the loop under identical conditions (providing the clock powers are kept low enough to prevent self switching, discussed later in this chapter) therefore, the clock is reflected. A control pulse enters the device through the coupler located on one side of the loop; see Figure 2-1. Once this control pulse has entered the loop it will propagate around the loop and pass through the SOA. The control pulse has a higher power than the clock pulses (normally sufficient to saturate the SOA) and thus depletes the SOA, reducing the carrier density. The timing of the control pulse is such that it arrives at the SOA before a propagating clock pulse. This following clock pulse will pass through the SOA before the amplifier has had time to recover. Whereas, the clock pulse propagating in the other direction will enter the SOA at two possible opportunities: before the control pulse or after the control pulse when the SOA has recovered. The different carrier densities, experienced by the propagating clock components, result in a differential phase shift. When this differential phase shift reaches a value of π, complete switching is achieved (complete switching is only achieved if the gains seen by the clock pulses are equal. In reality the different carrier densities experienced by the clock pulses result in different gains. Hence, when the pulses recombine at the 50:50 coupler they will have different energies thus, making complete switching impossible.)

The switching window is a period of time, relative to the clock pulses, where the arrival of a control pulse can cause switching. In the case of the NOLM, which uses Highly Non Linear Fibre (HNLF), this window is relatively small. This is because switching is reliant upon the clock and control pulses propagating through the non-linear element in perfect alignment. Any variation in alignment, such as caused by timing jitter, would cause the XPM effect to be reduced, thus causing a reduction in

the amount of phase shift experienced by the clock pulse. In comparison, the relatively slow response time of the SOA ensures the switching window for a TOAD is greater than that found in a NOLM hence the TOAD is less susceptible to timing jitter. The response time of the HNLF is in the femtosecond regime and this enables very high bit rates, however the short response time has a disadvantage. The peak power mainly generates the switching (as opposed to the energy of the pulse) and therefore requires large amounts of average signal power.

The SOA has a much longer response time, compared to HNLF; therefore it is the integrated power of the control pulse which determines the amount of switching. This ability for the SOA to utilize a greater percentage of the pulses energy, results in less signal power required for switching (when compared to a HNLF based device.) However, the maximum possible bit rate is limited by the SOA recovery time of the SOA typically lager than 15ps.

After a clock pulse has passed through a depleted SOA, it is essential that the SOA has fully recovered from the effects of the control pulse before the next clock pulse arrives from the opposite direction. If the SOA does not recover in time then the subsequent pulse shall encounter a reduced carrier density resulting in either cross talk between individual bits or a reduction in switching (the result of which is dependent upon which side of the loop mirror the SOA is offset, discussed later in the chapter.)

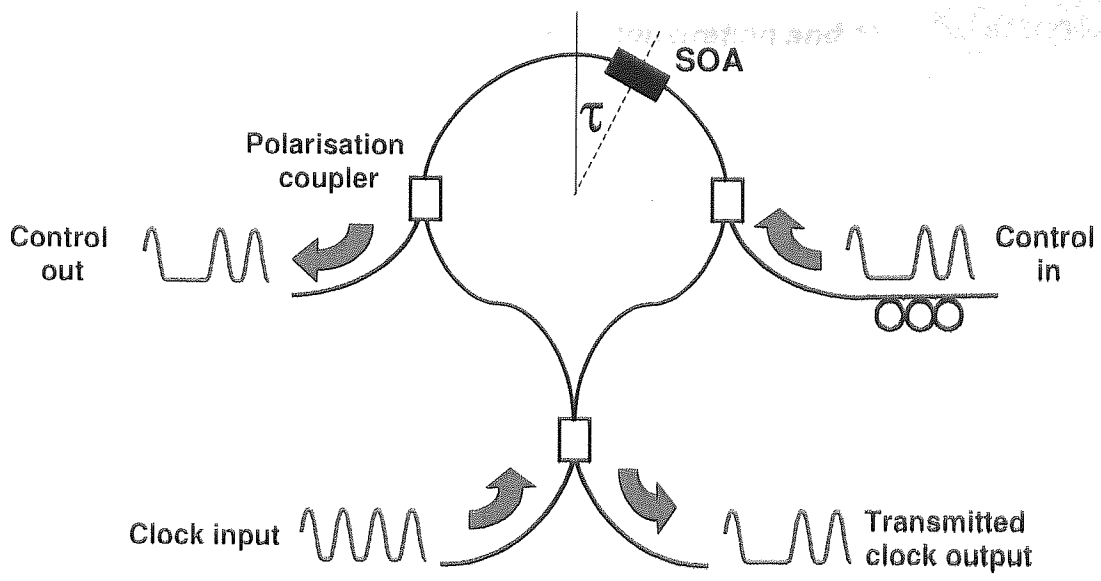


Figure 2-2 Controlled switching configuration using the same wavelength for both data and clock signals. The original data is split from the clock using polarisation couplers.

In most cases it is not desirable to have the control pulse present at either the reflected or the transmitted ports. In the case where the control and the clock signals are operating at a different wavelength, this problem can be simply solved with the use of band pass filters located on the output ports. However, when they have the same wavelength then a different method has to be used. Figure 2-2 demonstrates an arrangement where two polarization couplers are used to separate the two signals. The control input coupler, located in the loop, is replaced with a polarisation beam combiner. The output of the beam combiner is such that the polarisations of the clock and control signals are set to be orthogonal to each other. After the two signals have passed through the SOA they are then separated through the second polarisation beam splitter (located on the opposite side of the loop) ensuring that none of the original control signal is present at either the reflected or the transmitted outputs (although practically the splitter does not provide perfect extinction therefore, leakage will always be present.)

2.4. Self-switching experimental demonstration and characterisation

When setting up a TOAD the initial experiments normally involve operating the device in a self-switching configuration. The results generated from the initial experiment will provide vital practical information on both the maximum clock input power (which can be used in a controlled switching configuration) and present an accurate location of the SOA in relation to the centre of the loop.

Self-switching of a loop mirror, where the SOA provides the non linear element, is a phenomenon where switching is dependent upon the intensity of the clock. As with any loop mirror configuration, operation begins with a clock pulse entering the loop coupler. The pulse is then split into two propagating pulse which travel around the loop in opposite directions. The propagating pulses will pass through the SOA and continue around the loop until they recombine in the coupler and exit through the appropriate port (defined by the differential phase shift applied to the two pulse halves.)

Two conditions must be met before self-switching will occur; firstly the SOA must be offset to unbalance the loop and secondly the clock power must be high enough to promote the non-linear effects of the SOA. If the intensity of the incident clock pulse is low then the reduction in the carrier density will be low. Consequently, on the condition that the SOA offset is large enough to provide sufficient time for the carrier density to recover, the SOA will be in the same condition for both propagating pulses. This will keep the loop balanced hence, self-switching will not occur. A higher clock power would cause a greater reduction in the carrier density. The further the carrier density is reduced, the longer the time required for the SOA to fully recover. If the

SOA cannot recover in time, the following propagating pulse will encounter a reduced carrier density level. This would result in a differential phase shift between the two propagating pulses, unbalancing the loop, generating switching.

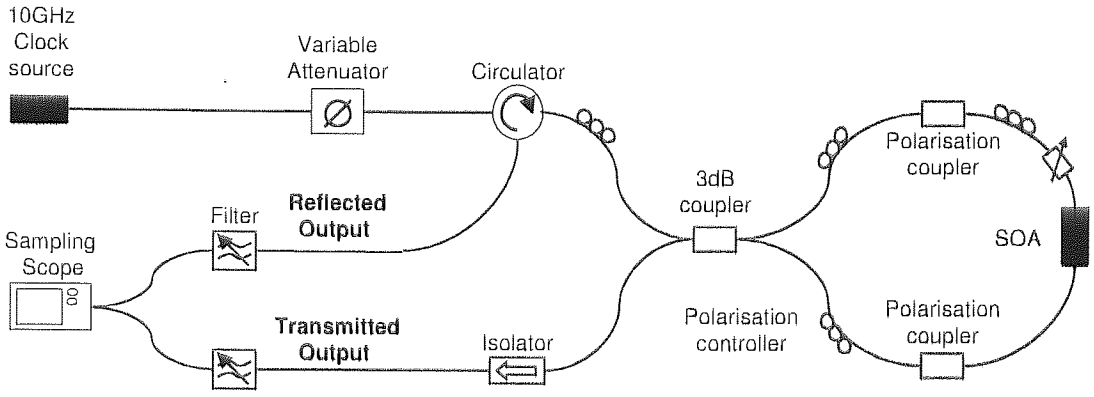


Figure 2-3 Experimental setup used for self switching configuration results

Figure 2-3 shows the experimental setup for the self-switching measurements. The clock source is a 10GHz fibre ring laser providing RZ pulses with 7ps Full Width Half Maximum (FWHM) pulse width at a wavelength of 1550nm. A circulator is located in the input path to provide a method of measuring any reflected signal. The SOA offset was set such that it was off centre according to the requirement discussed earlier, which in this case was ~10ps. The length of the SOA used in all the experiments in this thesis has a length of 1.6mm and will in all experiments in this thesis unless otherwise stated, be operating with a forward bias current of 160mA.

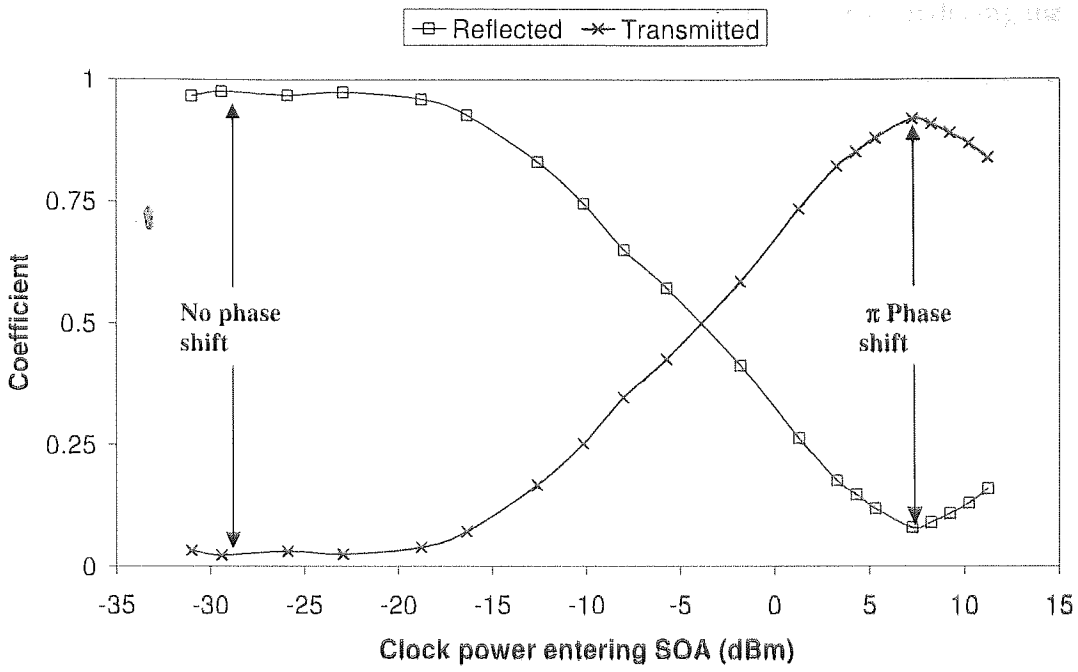


Figure 2-4 Self-switching output co-efficient for increasing clock powers. As the clock power increases a phase shift is generated so the output is switched from the reflected to the transmitted port

The results shown in Figure 2-4 are a measure of the reflection coefficient Pr/(Pt+Pr) and the transmission coefficient Pt/(Pt+Pr) as a function of increasing clock power (where Pt represents transmitted output power and Pr represents reflected output power.) At low clock powers (<-20dBm) most of the power is reflected and hence no self-switching is taking place. With clock powers higher than -20dBm self-switching starts to become apparent, indicated by the increase of the clock signal at the transmitted port. This switching of output powers continues until a level of ~-4dBm of clock power when equal amounts of clock signal exit through both reflected and transmitted ports. Further increases eventually result in maximum switching-here the output from the reflected port is at a minimum and the output at the transmitted port is at a maximum.

When working with TOADs self-switching is an important consideration. For example, if the clock power is too high self-switching becomes dominant reducing the extinction ratio. It is therefore desirable to have a clock power that is low enough not to cause self-switching. Care must also be taken to choose a clock power which is not too low. The power of the switched out clock pulses is proportional to the clock input power. Since the transmitted output will often be used to create a new control pulse we need the power to be as high as possible with maximum extinction ratio. Also, at very low clock input powers the ASE noise of the SOA will dominate the transmitted signal. Further studies of this effect can be found later in this chapter, where we will investigate and discuss how the position of the SOA can be optimised to satisfy both the requirement for a non-self-switching device and a transmitted output with a high SNR.

Although self-switching is a disadvantage in the operation of a TOAD it can also serve as a useful tool when setting the required offset position of the SOA. Self-switching can be used to accurately locate the centre of the loop mirror, or τ=0, to within approximately 2ps. From this reference point we can then set the SOA to the desired value of τ.

Using techniques such as pulse timing and physical measurements we can provide an initial indication of the location of the SOA to within ~50ps. However, when using high bit rates a more exact location of the SOA is required. By setting the clock pulses to a high enough power to generate self-switching (>-20dBm see Figure 2-4), we can plot the intensity of the self-switching for varying SOA offset times.

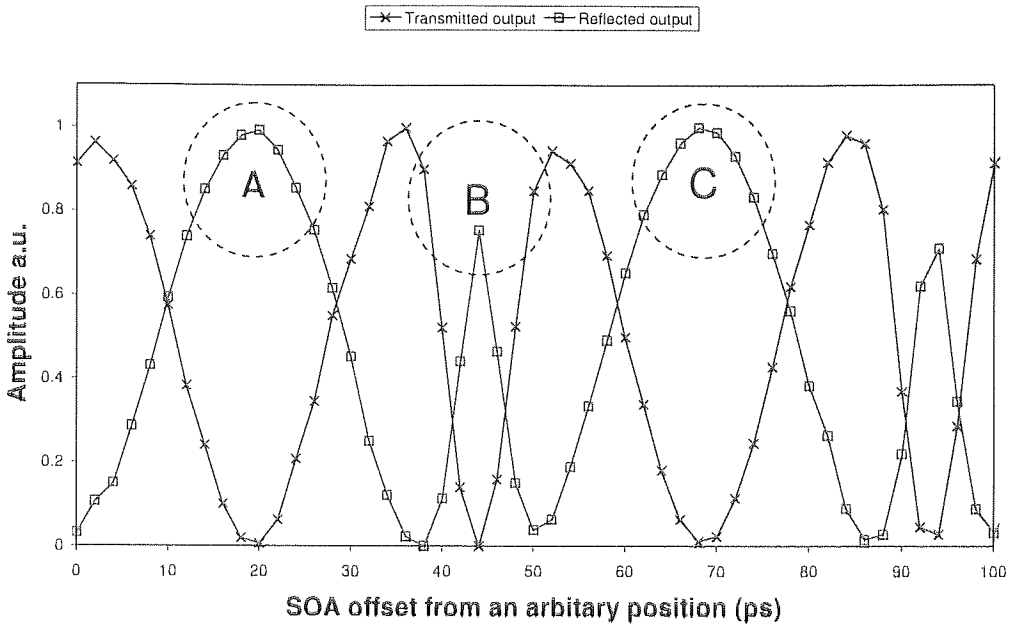


Figure 2-5 Self-switching against SOA offset, "A" and "C" shows the SOA 25ps from the centre of the Sagnac loop, "B" shows SOA in centre of the Sagnac loop

Figure 2-5 shows the results taken for self-switching as a function of SOA offset time. As stated previously the clock consists of RZ pulses operating at 10GHz with the clock input power set to 7dbm (from the previous experiment this power is known to cause self switching). Both transmitted and reflected output powers have been normalised for comparison. The horizontal axis refers to the offset of the SOA from an arbitrary position (not necessarily from the centre of the loop). This position was found to be close to the centre using basic measurements such as pulse timing.

Switching occurs when the two propagating pulses arrive at the SOA at separate unequal times. However, switching does not occur when the pulses enter the SOA at the same time or at equally spaced intervals determined by the bit rate. As can be seen from the graph there are three significant points of maximum reflection at 19ps (point A), 43ps (point B) and 68ps (point C). The fourth point at 92ps is where the SOA is offset from the loop centre greater than one bit and hence is neglected (we know this

from using approximate measurement techniques such as physical measurements and pulse timing.)

If we look at the regions immediately before and after the points of maximum reflection, we see that points A and C are of a similar quadratic shape. In contrast to the other two points the region near point B appears to be a cusp. This variation allows us to distinguish between pulses arriving at the SOA at the same time or at equally spaced intervals.

When the SOA is at τ=0 the pulses arrive at the same time, making it impossible for a differential phase shift to occur. Consequently, there is maximum reflection and minimum transmission. A small change in SOA offset means that one pulse arrives immediately after the other and as a result the two pulses will experience a large difference in SOA carrier density. This characteristic can be identified as a cusp like shape as found in point B. For points A and C the pulses arrive at alternate equal time intervals, meaning an offset value of $\tau = B_R/4$, where B_R represents the bit rate period. The time between the two propagating pulses arriving at the SOA is calculated as:

$$T_{cw,ccw} = 2\tau \qquad (2.1)$$

Thus, when $T_{cw,ccw} = B_R/2$ the time period between each pulse arriving will be equal. A small change in the offset from this position will mean that there is still a long time period between the two propagating clock pulses hence, resulting in the quadratic nature of the extremal point.

From the results taken in Figure 2-5, the location of the centre of the loop is at point B (44ps from the arbitrary position). With points A and C, 19ps and 69ps respectfully,

signifying the position where $\tau=B_R/4$ (this will be confirmed later in the thesis using a separate technique.)

2.4.1. SOA offset positioning

When setting up the memory, it is useful to know how a change in clock power affects the levels of self-switching. For varying values of τ, a sweep of clock powers was injected into the loop and using a sampling oscilloscope the peak level of the reflected and transmitted pulses was recorded. An attenuator situated just after the source Figure 2-3 controls the intensity of the clock.

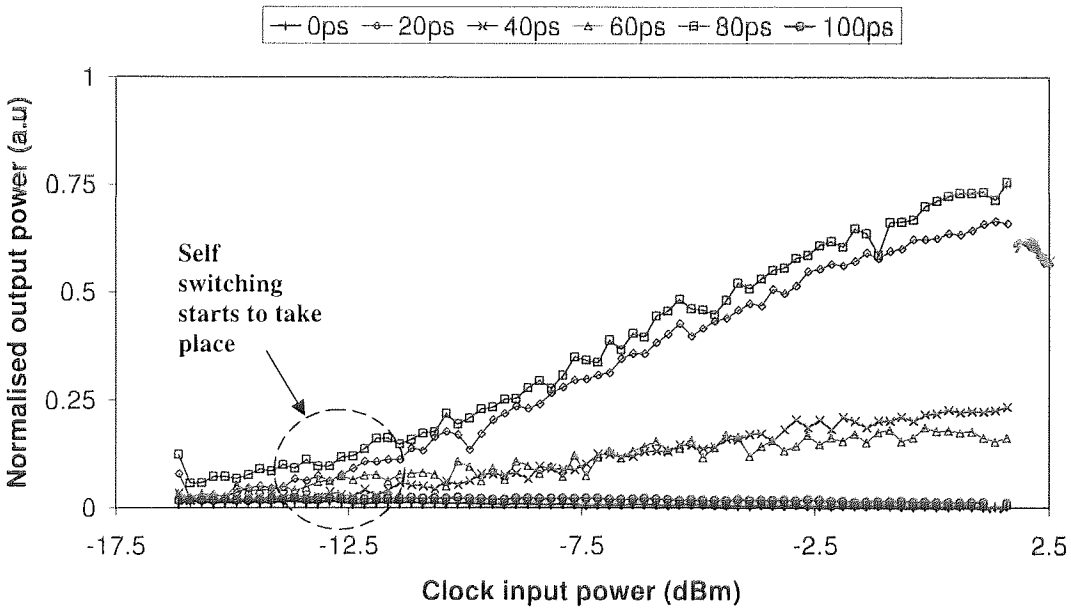


Figure 2-6 Self switching transmitted outputs for various SOA offsets values of τ

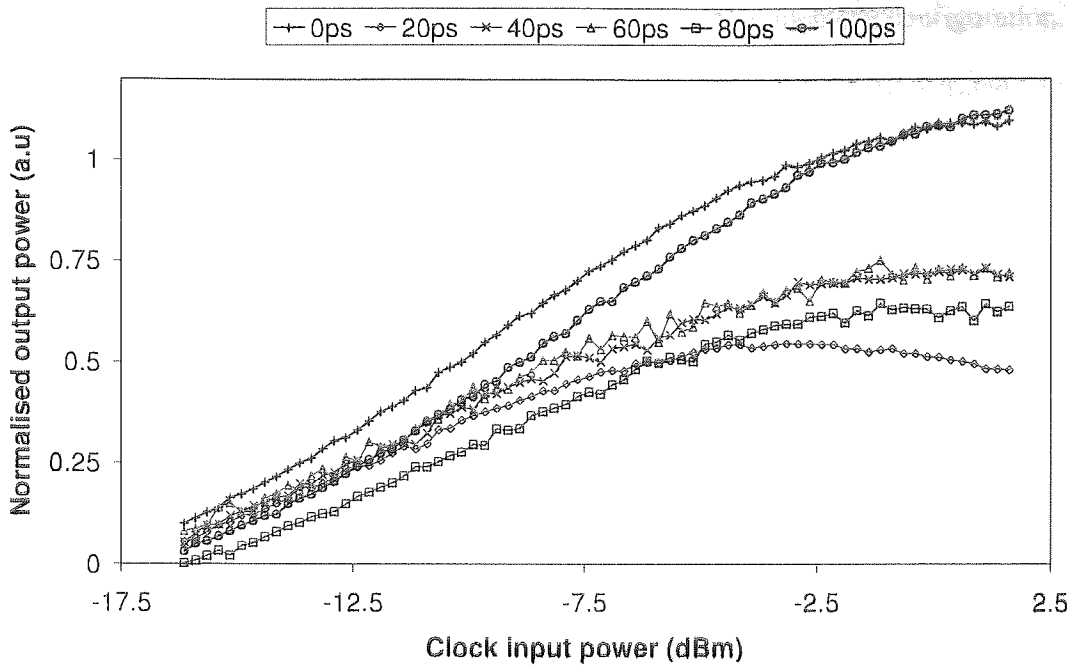


Figure 2-7 Self switching reflected outputs for various SOA offset values of τ

From the two graphs in Figure 2-6 and Figure 2-7 it can be seen that when τ equals 0 and 100 there is very little switching, confirming that this position represents an offset where the pulses arrive at the SOA at the same time. It can also be seen from the graph of transmission output that the maximum self switching is measured at τ of 20ps and 80ps and that they also have similar characteristics which means they are symmetrical around a point where maximum reflection is achieved. From the results it can be seen that a clock input of -12.5dBm is the clock power at which the self-switching starts to take place (it is at this point in the curve Figure 2-7 where the gradient changes discontinuously indicating that switching is starting to take place.)

2.5. Controlled switching experimental demonstration and characterisation

In the previous section we demonstrated the operation of the SLALOM where switching of the clock pulses was determined by the input pulse power. Future experiments will be mainly based around the TOAD. Therefore, it is essential that the

operation is understood before moving on to the non-inverting memory configuration. In the next section the experimental operation of the TOAD will be demonstrated and some of its basic characteristics will be investigated.

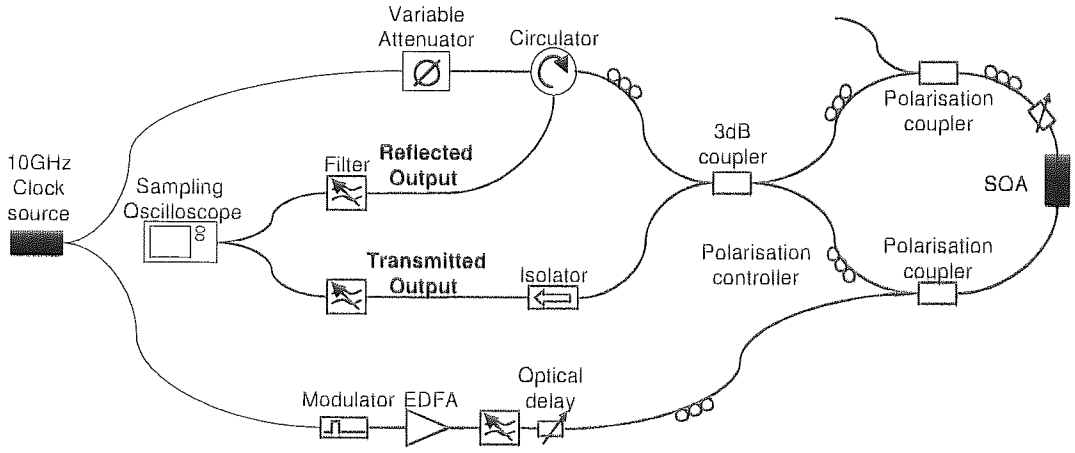


Figure 2-8 Schematic of the experimental TOAD

Figure 2-8 shows the experimental setup of the TOAD. As can be seen, a fibre ring laser supplies a 10GHz RZ pulse stream for both the clock and the control signals. The RZ pulses have a FWHM of ~7ps at a wavelength of 1556nm. The RZ pulse stream is modulated with data using a lithium niobate modulator to generate a control signal (In these initial tests the control signal will have no data and will consist entirely of ones.) The clock and control signals are set to have orthogonal polarisations. Located on either side of the loop are polarisation couplers which combine and separate the two orthogonal signals (In the normal TOAD configuration only a polarisation coupler on the control output is required and the input coupler can be replaced with a standard coupler. However in the memory configuration the input polarization coupler is also used to further reduce some of the noise propagating around the loop.)

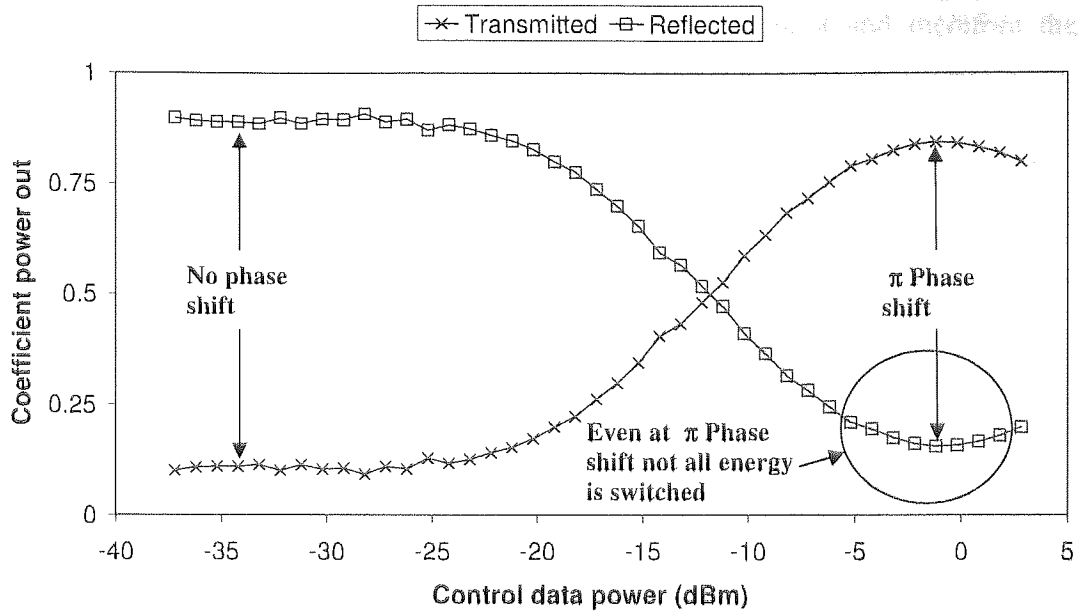


Figure 2-9 Measured transmitted and reflected coefficient for the controlled switching of a TOAD.

Switching is achieved through the presence of control pulses, which are used to deplete the SOA's carrier density before the arrival of the clock pulse. The reduction in the carrier density is dependent upon the intensity of the control pulse, therefore, the more power in the control pulse the greater the differential phase shift.

Figure 2-9 shows the switching coefficient for the TOAD. Initially with low control powers the reduction in the carrier density is low enough for the SOA to recover before the following clock pulse enters the SOA. However, at approximately -25dBm the SOA is beyond the limit where full recovery can take place and hence will remain saturated for the following pulse. It is at this point where switching starts to take place and some light exits from the transmitted output. At -12dBm of control power, the clock output powers on the reflected and transmitted ports are equal. Maximum switching is achieved at -1dBm (or 80fJ) indicating a differential phase shift of π,

beyond this level the differential phase shift is greater than π and therefore the switching starts to reverse.

In any experimental system the clockwise and the anticlockwise propagating clock pulses will each experience a different gain when switching is required. As a result the pulses will have different energies when recombining in the loop coupler. The consequence of the loop mirror characteristic ensures that perfect switching (that is all the clock pulse energy is switched to the transmitted port) cannot occur Figure 2-9.

2.5.1. Control pulse timing and SOA offset characterisation

The switching efficiency of the TOAD is highly dependent upon both the SOA offset and the arrival time of the control pulse. When the control pulse enters the SOA it will saturate the amplifier generating a period of time where the SOA has a reduced carrier density. To enable switching to take place it is within this period of saturation (the switching window) that only one clock pulse must enter. If the timing is incorrect then there will not be a differential phase shift between the propagating clock pulses and hence switching will not occur. Subsequently when researching the operation of a TOAD it is important to understand the timing characteristics of SOA offset against the timing of the control pulse.

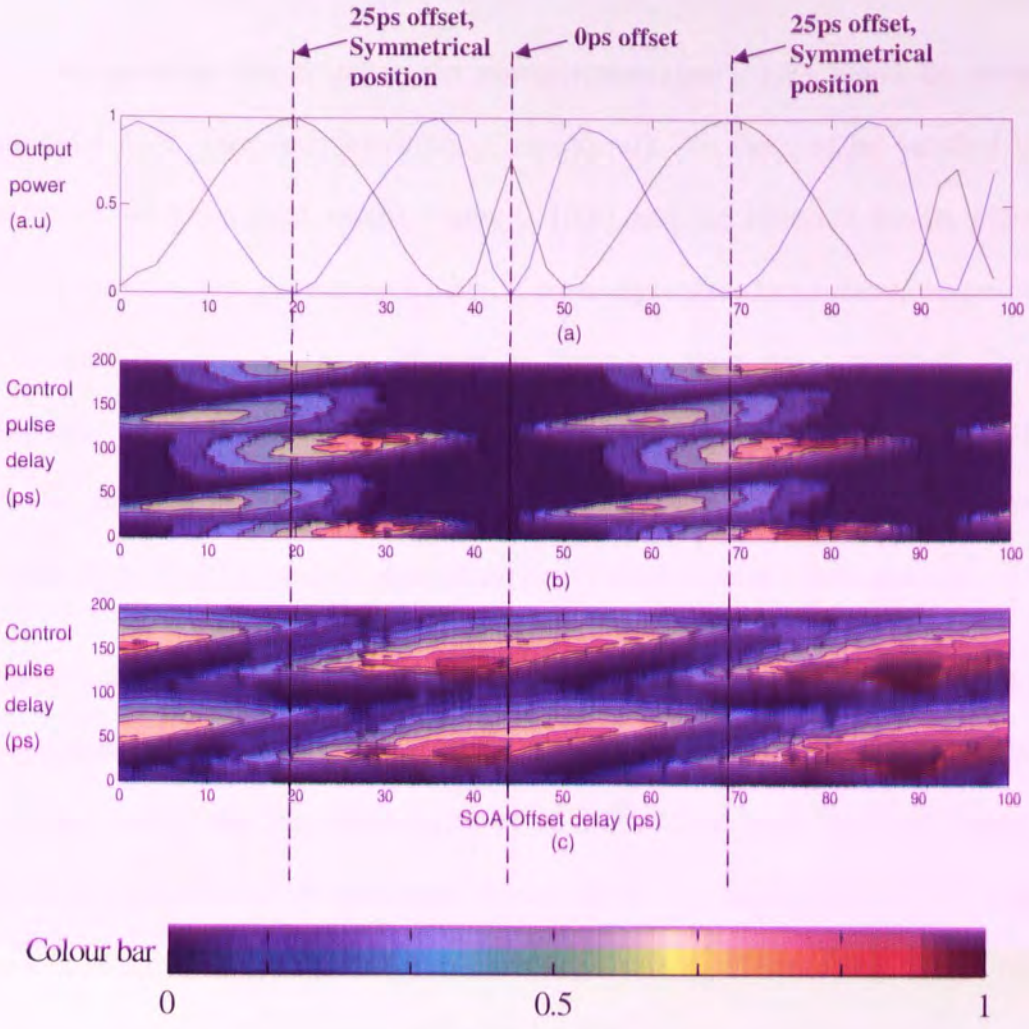


Figure 2-10 Chart (a) shows the self-switching outputs for the reflected and the transmitted outputs, for varying SOA offsets. (b) Shows the transmitted output map for varying offsets and control pulse delays, with (c) showing the output for the reflection.

Using the experimental setup shown in Figure 2-8 the relationship of the control pulse delay and the SOA offset position was investigated. The peak power at both the reflected and the transmitted outputs was measured for each of the timing and offset positions. Figure 2-10(b) shows the results for the recorded peak powers for the transmitted port and Figure 2-10(c) shows the results for the recorded peak powers for the reflected port. In order to ensure that a complete map is produced we chose a total range for both the control pulse delay and τ of 200ps.

The two equations which define the power transmitted (1.13) and the power reflected (1.12) are complementary. Consequently, for these to be satisfied the pattern of the transmitted results Figure 2-10(b) and the reflected results Figure 2-10(c) must also complement each other. If we analyse these two figures, we can see that largely this rule has been adhered to. However, there are exceptions. These exceptions arise because in reality the total amount of signal power exiting the reflected and transmitted ports is not constant (this signal power is dependent upon the gain from the SOA which is determined by the timing of the control pulse.)

There is only one condition of SOA offset where switching cannot be achieved and is independent of the control pulse arrival time. This condition occurs exclusively when the offset is such that the pulses arrive at the SOA at the same time and hence a switching window cannot be generated. Figure 2-10(a) is a copy of the self-switching result shown in section 2.4. The two conditions where self-switching cannot take place are either when the pulses arrive at the SOA at the same time or at equally spaced intervals. It was described that these conditions can be differentiated through observing the regions of peak reflection (cusp or quadratic). Also in this section we discovered that the SOA would be in the centre of the loop at around ~44ps from the arbitrary reference point. If we compare the three plots in Figure 2-10 we can see that at ~44ps, when using the TOAD configuration, there is no output on the transmitted port for all control pulse arrival times, hence, confirming the SOA is at τ=0 in the self switching experiment.

If we analyse these results closely we can see that even when τ=0 the reflected output power does not remain constant even though there is no evidence of output power on the transmitted port. This is one of the exceptions mentioned in a previous paragraph

where the control pulse is affecting the total amplifier gain seen by the clock. Hence, for position τ=0, the control delay where reflection is at minimum output power indicates the control pulse arriving at the SOA depleting the carrier density, immediately before the clock pulses arrive. Therefore, both propagating clock pulses would see a lower gain and the total output signal power would be reduced.

The second point where self-switching could not be generated was at SOA offset positions of τ=25ps for a 10GHz system or ¼ bit rate period, from the centre of the loop. Here the clock pulses arrive at the SOA at equal alternating intervals so self-switching could not be generated. If we analyse the controlled switched results for these positions of SOA offset we can see that controlled switching is possible. This is because the clock pulses arrive at the SOA at different times and provide the potential for a control pulse to open a switching window. It is also worth noting that the control pulse can open two distinctive switching windows, depending upon its arrival time. The two windows refer to the reality that either of the two (counter/co) propagating clock pulses can potentially experience the reduced carrier density (this being dependant upon the arrival time of the control pulse.) It is this offset position which will be used in the final memory configuration as it can provide controlled switching whilst remaining independent of self-switching. This decision will be justified in the next section.

2.6. SOA symmetrical offset position demonstration

With any switch design one of the main considerations would be the extinction ratio of the output. When considering a TOAD this can be either the output for the reflection or the transmission ports (In the case of the TOAD the switched extinction ratio can also be simultaneously measured across both the reflected and transmitted

ports, for example the ratio between the maximum output power on the transmitted port, at full reflection, and the output power on the reflected port. However, in the case of the memory this is not a required consideration.) The extinction is defined to be the ratio of the power in a bit level 1 and a bit level 0 [81] and can be expressed as:

$$R_{ext} = \frac{P_1}{P_0} \qquad (2.2)$$

where P_1 represents the power of the ones and P_0 represents the power of the zeros. The output extinction ratio of a switching device is extremely important when the output of the device is to be used as control pulses for future processing, such as a cascade configuration [82]. If in the case that the extinction ratio was low and further devices reduce the extinction ratio further, then the quality of the signal would degrade until the extinction is too low and the data will be lost.

Many applications involve feedback or looped arrangements [45, 83] including the memory device under study in this thesis. Under such conditions the optimal operation of the TOAD has two conflicting requirements; 1) the clock pulses must be kept at low power in order to avoid saturation of the SOA resulting in the generation of self-switching and 2) the switched clock pulses need to be amplified to act as subsequent control pulses. Since the control pulse energy is fixed, reducing the clock power to satisfy condition 1 means increasing the loop gain to satisfy condition 2. This inevitably leads to an increase of the noise level and reduces stability. In this section we look at a novel operating regime which allows higher clock powers while avoiding saturation effects. We also show that the extinction ratio is improved.

We now describe a simple model of the effect of suppressing the self-switching on the extinction ratio. The equation for the differential phase shift applied to the clock pulses is:

$$\Delta\varphi = F_{pc} + \Gamma P_S , \qquad (2.3)$$

where F_{pc} is the effective differential phase shift generated by the saturation effects of the control pulse and Γ is a coefficient determining the phase shift caused by self switching, as described above, defined by the SOA offset position τ. With the device set up in the non-symmetrical position then Γ will be non-zero and hence the total phase shift will be linearly dependent on the clock power P_S. If, however, the symmetrical position is used then Γ would be zero and hence the total phase shift is independent of signal power. The calculated value of $\Delta\varphi$ can then be used to determine the transmission coefficient of the loop mirror as

$$t = \frac{1 - 4\alpha(1-\alpha)\cos(\Delta\varphi)}{2}, \qquad (2.4)$$

where α represents the coupling ratio, set to 0.5 in the simple model. If we include the power of the noise floor for the device and receiver P_N, the total extinction ratio of the peak power for a "1", P_1, against the peak power of a "0", P_0, present at the transmitted output and can be defined as:

$$E = \frac{P_1}{P_0} = \frac{t_1 P_S + P_N}{t_0 P_S + P_N} \qquad (2.5)$$

Each operating point corresponds to a different value of Γ, zero for the symmetrical position and non-zero for the traditional position. We can now plot the extinction ratio 10 Log E against clock power P_S

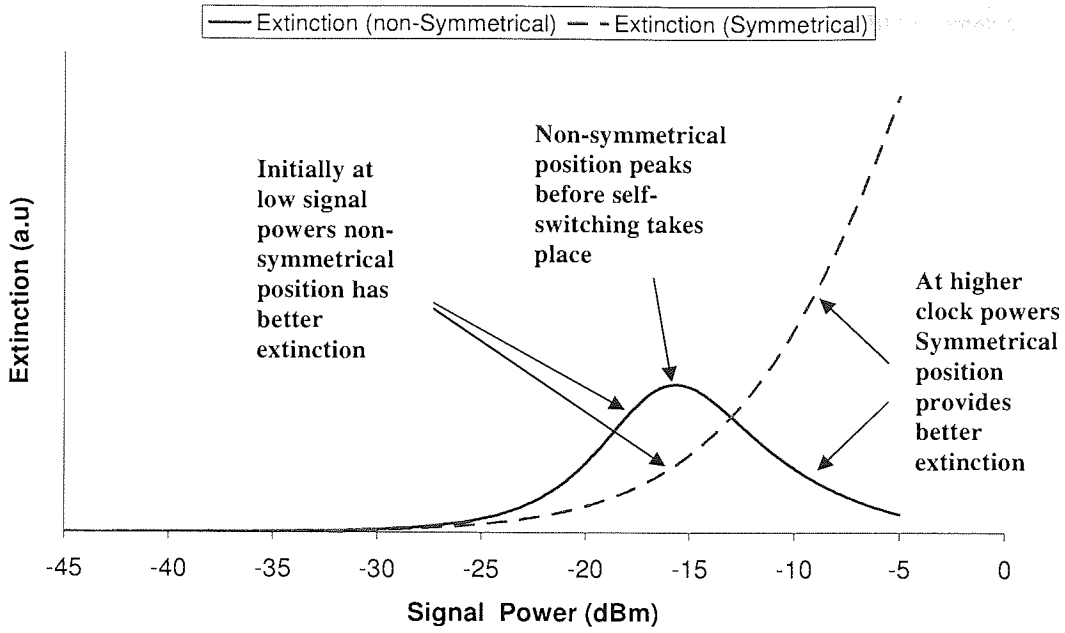


Figure 2-11 Extinction ratio 10 Log E for varying clock powers for two values of Γ showing the effects of self switching upon the extinction ratio

As we can see from Figure 2 11, for small clock powers (<-16dBm) the extinction appears to be better in the traditional set up. However, further increases in clock power reduce this advantage as the self switching component starts to quickly dominate. This eventually results in the reduction of the extinction ratio. As self switching is not present when the SOA is in the symmetrical position the extinction ratio increases monotonically as the signal power increases (at least for small signal powers). Plotting P_0 and P_1 for the symmetrical and the non-linear operating points Figure 2-12 shows us how the extinction ratios vary.

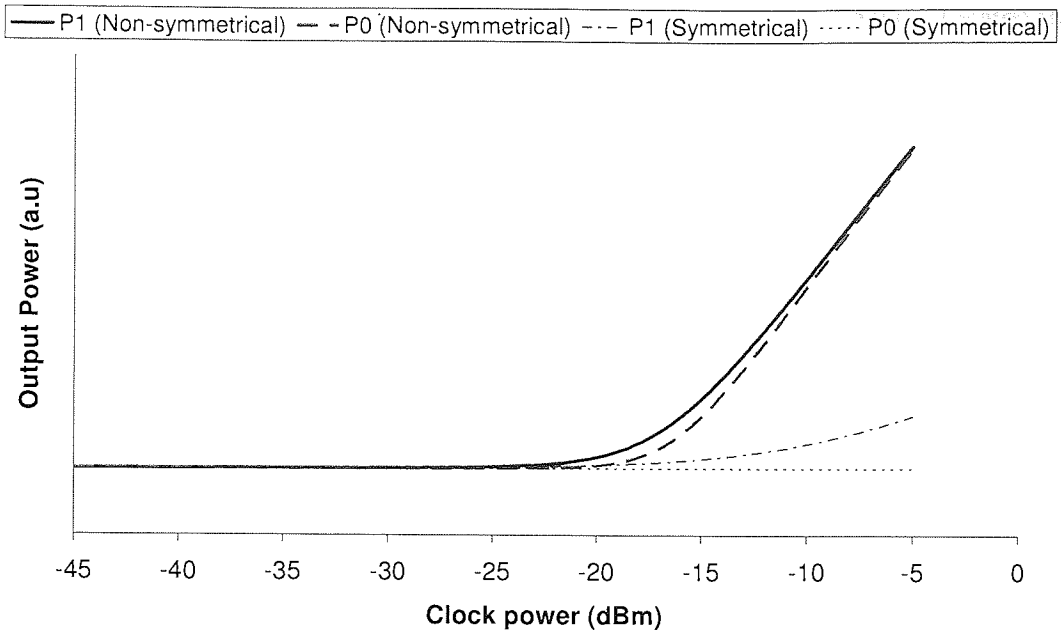


Figure 2-12 Shows the values for P_0 and P_1 for the symmetrical and the nonlinear operating points against signal power

——— = P1 — — — = P0 (non-symmetrical position)

——- = P1 ---------- = P0 (symmetrical position)

If we look at the traditional (non-symmetrical) SOA position, we can see although the output power is high for P_1, because of the self switching, the output power for P_0 is also high making the extinction ratio low. Whereas in the symmetrical position because there is no self switching P_0 remains at 0 for all signal powers and therefore as the signal increases so will P_1 and hence there is an increase in the extinction ratio. In practice, as we will see, the extinction ratios at low signal powers are determined by leak through of the pulse (for example caused by imperfect loop coupling ratio), but this simple model captures the main features.

To confirm the results from the simulation a simple experiment was made using the TOAD. The TOAD was set up as mentioned previously; the source for the signal and the control was a fibre ring laser operating at 10GHz producing pulses which were broadened to 14ps FWHM using dispersion compensating fibre. The control pulse

arrival time and SOA offset were adjusted using two variable optical delays located in the control input path and the loop mirror respectively. The signal and control power were varied using variable optical attenuators. The two offsets to be compared were 9ps for the traditional operation and 25ps, for the novel symmetrical excitation.

The control and signal power was varied in the experiments for both SOA offset conditions 25ps and 9ps. The peak transmitted output power was recorded and the maximum extinction ratio calculated for a range of control input powers, the results are shown in Figure 2-13.

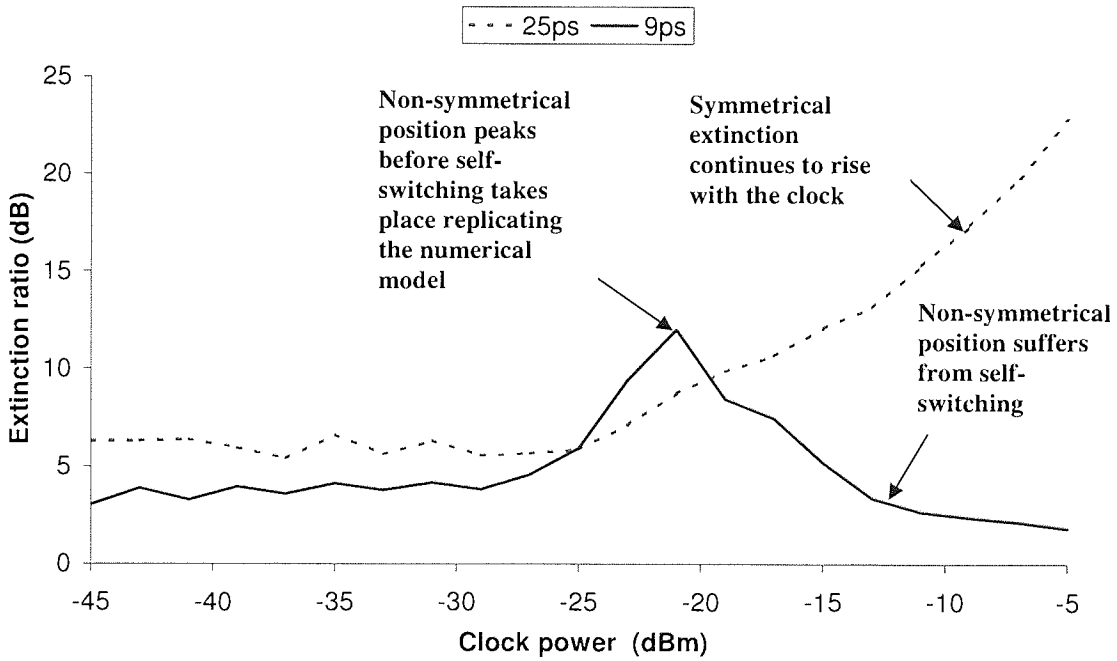


Figure 2-13 Extinction ratios for varying signal input powers at 9 and 25ps offsets

These results show that for the 9ps SOA offset, the extinction ratio increases with signal power until the point at which self-switching occurs and then a further increase in signal power actually decreases the extinction ratio. Conversely, at a 25ps SOA offset no self-switching is observed for an increase in signal power, while the

extinction ratio increases to the point limited by the maximum specified input power of the SOA.

It has been demonstrated that by setting the SOA's offset so that the arrival time of both the C_W and AC_W pulses are at equal intervals, a much greater extinction ratio can be achieved compared to a conventional TOAD configuration. Although initially at lower signal powers it seems that the more conventional approach provides better extinction ratio's, as the signal power increases and self-switching becomes prominent the extinction ratio actually reduces. Alternatively, with the new offset position, because self-switching does not occur, the TOAD is able to switch out larger signal powers without degrading the extinction ratio. The results show that an increase of 10dB in extinction ratio is possible while simultaneously allowing for a 16dB increase in input signal power (limited by the SOAs specified maximum input power). These results are significant to any system where high extinction ratio is desirable, such as the memory. It is the 25ps offset position, which is used for all following experiments.

2.7. Clock power characterisation

Previously in this chapter we have discussed the effect the clock power has on self-switching and how this effect can reduce the extinction ratio of the transmitted output. Using the symmetrical position demonstrated in the previous section to eliminate self-switching, we will now look at another main influence the clock power has on the switching of the TOAD.

When we describe the basic operation of a TOAD we generally assume that the clock pulse is of such small power that the reduction in the carrier density caused by the clock pulse is negligible and has no effect on the operation of the TOAD. If we use

high clock powers then the reduction in the carrier density caused by the propagating clock pulses increases and starts to make a considerable contribution to the operation of the TOAD.

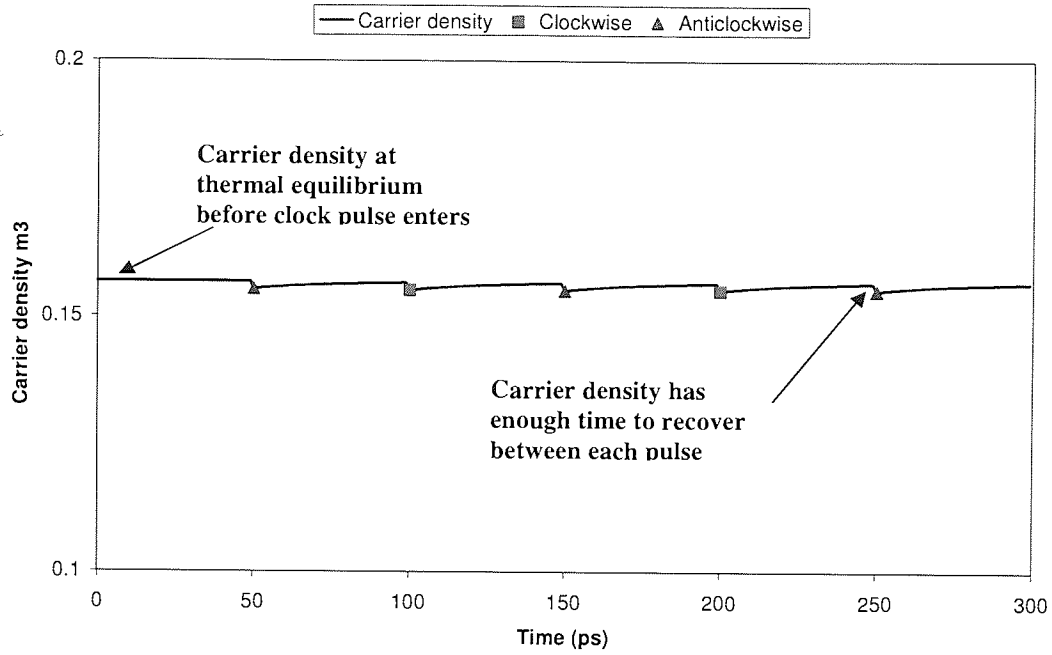


Figure 2-14 Evolution of the SOAs carrier density when the clock is small enough to allow the carrier density to recover between each pulse.

Any pulse entering the SOA causes the carrier density to reduce (we are only interested in the regime where the SOA provides gain.) From this reduced state the carrier density starts to recover. When small clock powers are the carrier density is reduced by only a small amount and, therefore, the SOA has sufficient time to recover before the next pulse has arrived. If large clock powers are used then the reduction in the carrier density is greater and as a result a longer time is required to obtain full recovery. If the SOA does not fully recover before the next pulse then the next pulse experiences the reduced carrier density and causes a further reduction. This will continue until a state of equilibrium is reached between the recovery of the SOA and the reduction in the carrier density caused by the clock pulse. Although the

relationship between the phase shift and the carrier density is linear, the relationship between the carrier density and the input pulse energy is not, see Equation (1.23) and Equation (1.24).

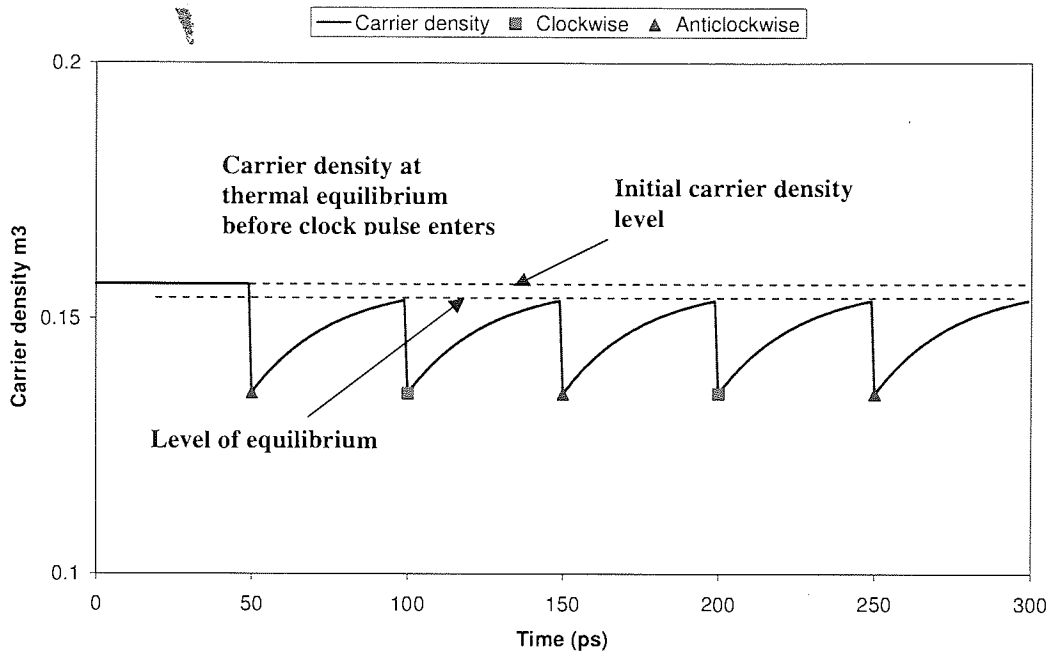


Figure 2-15 Evolution of the SOAs carrier density when the clock is high enough not to allow the carrier density to recover between each pulse.

This non-linear relationship means that high power clock pulses reduce the equilibrium. Therefore greater control powers are required to provide a similar level of switching for high power clock pulses.

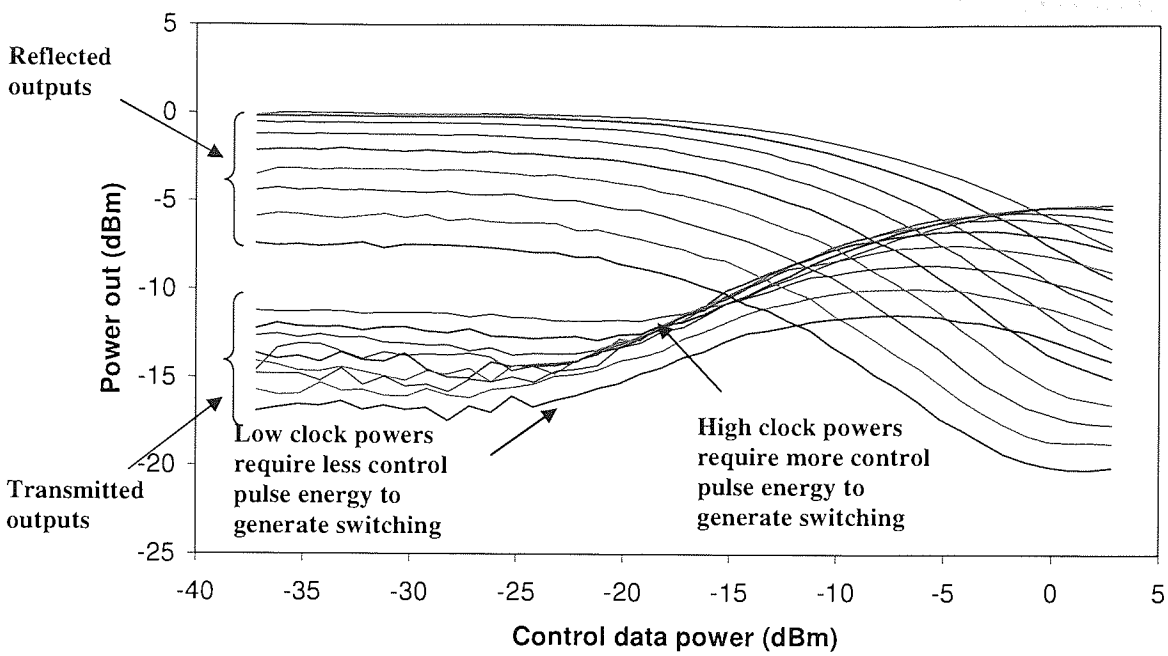


Figure 2-16 Controlled switching for varying clock powers showing the reflected and transmitted outputs

Figure 2-16 shows the switching curves for varying clock powers. We can see that at control powers <~-20dBm, where no switching is taking place, that when the clock powers increase the output level of the reflected port is also increased. Theoretically at these low control powers there should be no increase in the transmission output as there should be no trace of the clock pulse on the transmitted port. However, in practice this is not true. The extinction ratio of a TOAD is not infinite and therefore leak through is always present at the transmission output which becomes prominent as the clock power is increased.

If we turn our attention to the point at which a full π differential phase shift is achieved (point of maximum transmission), we can see that as the clock power increases so does the control power required to provide the same level of phase shift. This can be clearly seen when the coefficients are plotted in Figure 2-17. Here we can

see the point at which the transmission and the reflection meet at 0.5 requires more control power as the clock power is increased.

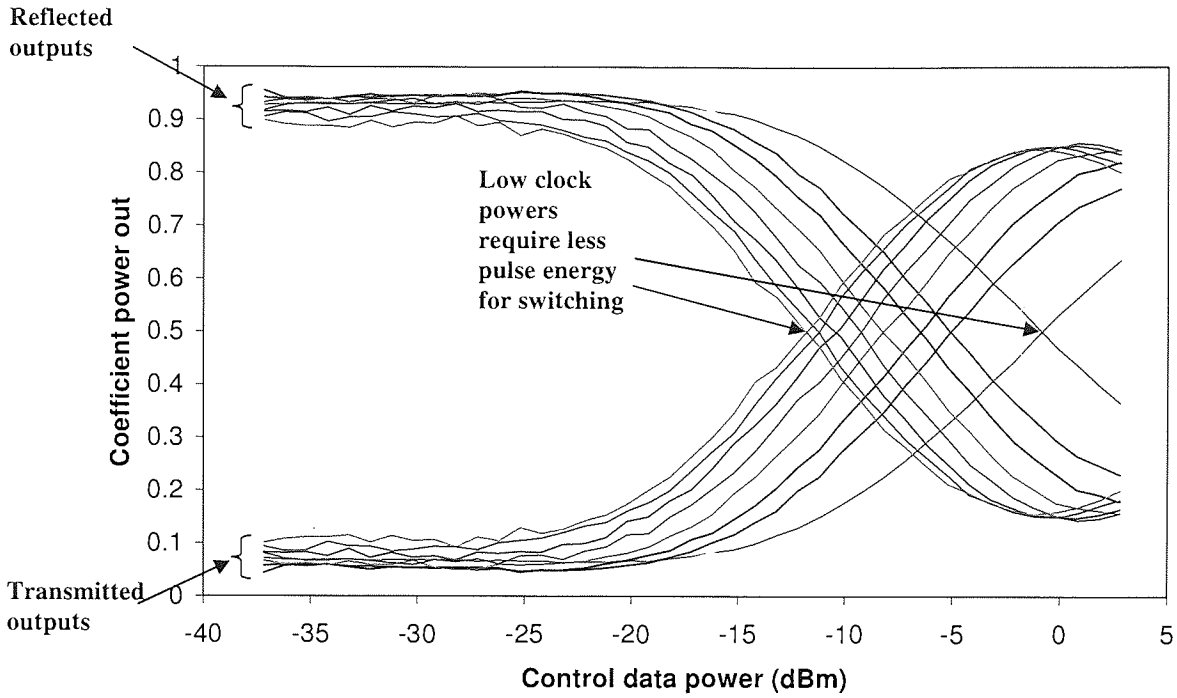


Figure 2-17 Reflected and transmitted coefficients of switching for increasing clock powers. Low clock powers require less control pulse energies to provide switching

2.8. SOA recovery measurements and influences

The SOA's recovery rate is a fundamental consideration when developing an SOA based optical switch and in most cases it is this characteristic that defines the maximum operational bit rate for the device. During the operation of a TOAD the level of switching is defined by the differential phase shift between the two propagating clock components. It is important that once the SOA has been saturated, the gain levels are recovered sufficiently for the next clock pulse. Otherwise the next clock pulse will be affected causing inter-bit cross talk that could corrupt the data. It is this recovery time which affects the optimum bit rate. For complete switching one of the propagating clock pulses must pass through a recovered SOA and the other pulse must experience a depleted SOA.

Up until now we have assumed that the SOA has had enough recovery time to ensure the following set of clock pulses, which will form the next bit slot, will pass through the SOA in a fully recovered state. As we increase the bit rate the time allowed for recovery is reduced. Therefore, it is important to understand how the operation of the device is affected, when the allowed recovery time is too short and the SOA cannot fully recover between bits. In this section we investigate how a slow SOA recovery rate affects the function of the TOAD and how this will ultimately affect the operation of the memory device. We will initially describe the effects using a simple numerical model, which will then be confirmed experimentally.

As discussed in the previous chapters the gain available in the SOA and the refractive index of the SOA depends upon the carrier density. For a fixed bias current, the maximum gain is available when the carrier density of the SOA reaches equilibrium between the effects of the pump current and the spontaneous emission. The carrier density where equilibrium is achieved N_{eh} can be expressed as

$$N_{eh} = \frac{If\tau}{eAl} \qquad (2.6)$$

Where If is the current, τ is the carrier lifetime, e is the electronic charge, A is active region area and l the length [84].

The recovery rate of the SOA can be defined as the slope for carrier density against time after the SOA has been saturated, due to a pulse of light travelling through the active region and reducing the gain available. The rate equation (1.16) describes the recovery of the carrier density. Between each pulse there is no incident light therefore the rate equation can be simplified to

$$\frac{dN}{dt} = \frac{If}{eAl} - \frac{N}{\tau} \qquad (2.7)$$

As we can see from the rate equation the carrier density of the SOA recovers exponentially. Therefore, the SOA will strictly require an infinite length of time before equilibrium N_{eh} is reached. It is for this reason that the recovery rate of the SOA is specified as the time it takes for the carrier density to recover from saturation level up to 1/e of N_{eh}. It is worth noting that by increasing the bias current the initial recovery rate will also increase, however, this will also result in an increase in N_{eh}. Furthermore, the greater the physical size of the active region the longer the device takes to recover. The recovery time of the SOA is determined by the carrier lifetime τ where an increase in the carrier lifetime will result in a longer recovery time (although in the simplified rate equation the carrier life time is independent of the carrier density in reality the carrier life time reduces as the carrier density increases).

2.8.1. SOA recovery rate measurements

To allow for true comparison between the simulation and the experimental results it is necessary to measure the recovery rate of the experimental SOA. This can be achieved by taking pump probe measurements. This measurement requires two input signals: a pump and a probe. The pump consists of a single RZ pulse and is injected into the SOA depleting the carrier density. A second RZ pulse, known as the probe, follows the pump pulse and the peak output power of the probe pulse is measured. By measuring the probe pulse at varying delay times from the pump pulse, we can plot the amount of gain available to the probe as a function of time. As we know the amount of small signal gain applied to an incident signal is proportional to the carrier density, therefore we can infer the recovery time of the carrier density from the gain dynamics.

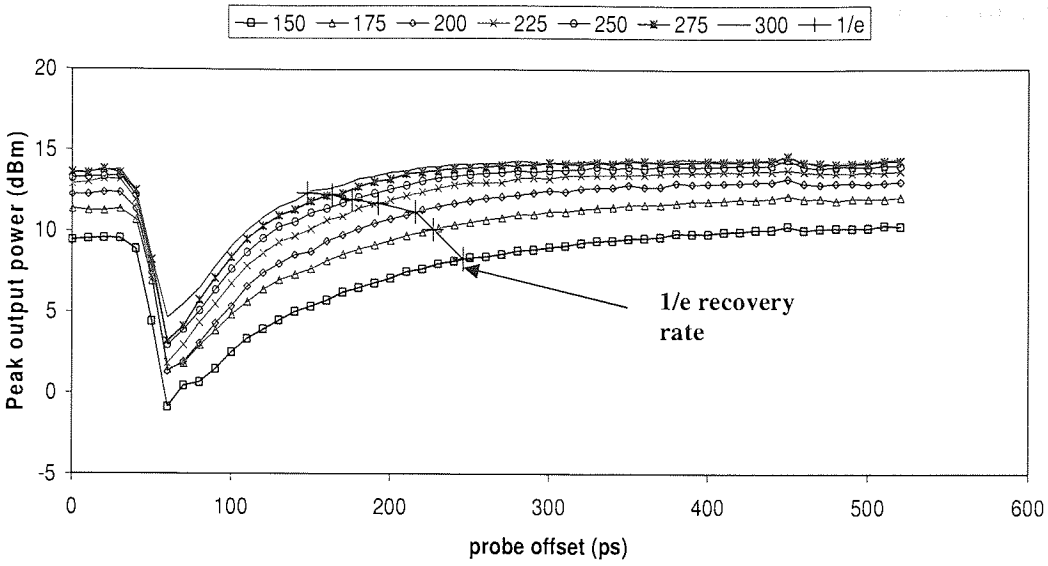


Figure 2-18 Pump probe results showing the gain recovery of the SOA

From the rate equation (1.16) we can see that as the electrical bias current applied to the SOA increases so does the initial recovery rate. Figure 2-18 shows the pump probe results measuring the change in the recovery for various SOA bias currents and a fixed probe power. It is the intention of the experiment to measure how long the SOA takes to recover from a fixed level of SOA depletion; therefore the pump powers were changed to ensure that the gain available immediately after the pump was the same for all currents. Along with the results the 1/e times are shown for each of the current powers. The results show that increasing the current from 150 to 300mA reduces the 1/e recovery rate from 240ps to 140ps. In both cases this is not fast enough to produce pattern independent switching at 10Gb/s as this would require a recover rate of <100ps.

It is also worth noting at this point that as the current is increased the gain available increases. However, this is not a linear process and as the current is increased the gain per mA reduces. If we plot the 1/e recovery rate against the SOA current we can see that within the specified operating range of the SOA the recovery improves linearly.

Thus, from the slope of the graph we can see an improvement in the recovery time of ~0.65ps/mA see Figure 2-19.

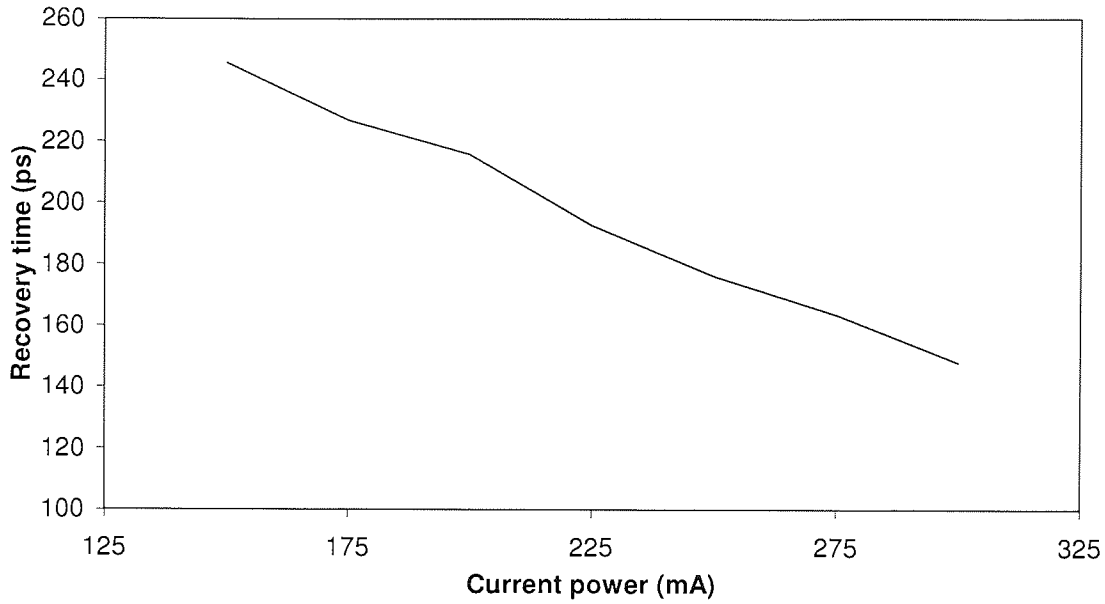


Figure 2-19 Plotted recovery time for 1/e for varying forward biasing currents

2.8.2. Numerical simulations demonstrating the effect of a slow SOA on the operation of a TOAD

In this section it will be demonstrated through numerical modelling how a slow SOA affects the operation of a TOAD. The model will be based around the equations derived in section 1.10. If the SOA is fast enough there should be no evidence of the data being corrupted from inter-bit interference. The condition will be demonstrated where the SOA does not recover in time and inter-bit interference will occur. The affect this characteristic has on the operation of the TOAD shall also be investigated.

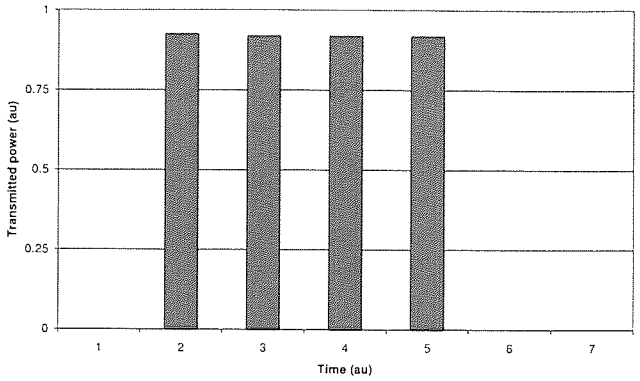


Figure 2-20 Results of a four bit word (1111) switched out from a TOAD operating at 300ps slow enough for the SOA to fully recover between each bit

Figure 2-20 shows the result of a simulation of a 4bit word pattern containing 1111 when the device is working at a 3.33GHz bit rate, that is 1 pulse every 300ps. Each bar represents the power of the pulse exiting through the transmission port. As can be seen from the results, all of the amplitude levels of the pulses are the same - which is what we would expect if the device is working correctly and the SOA has had time to recover between each of the pulses. We can monitor the recovery of the SOA by plotting the carrier density. While this information would be difficult to generate experimentally, numerical calculations provide a suitable way to demonstrate the effects of a slow recovery rate.

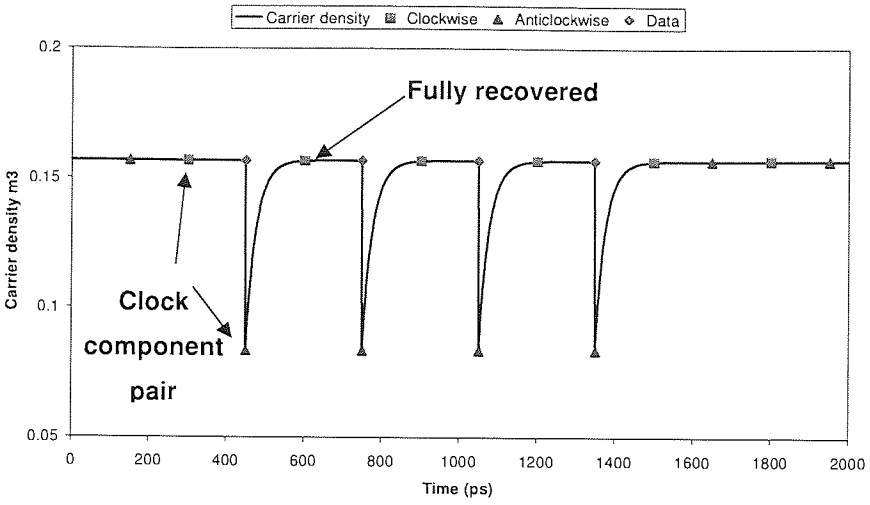


Figure 2-21 Carrier density chart for the four bit word found in Figure 2-20 demonstrating complete SOA recover between bits.

Figure 2-21 is the associated time dependant carrier density for the four-bit word operating at the 3.3GHz. Of the two counter propagating clock pulses it is the clockwise pulse that enters the SOA first thus experiencing the SOA in its fully recovered state. When switching is required the clockwise pulse is followed by the data pulse. The data pulse depletes the SOA, thus the following anticlockwise pulse will pass through the SOA in a saturated state. No inter-bit interference is achieved at this speed because there is enough time for the SOA to recover before the clockwise pulse belonging to the next bit enters the SOA. (Although this configuration allows extra time for the SOA to recover, an increase in bit rate would reduce the available time for the SOA to recover. If the SOA cannot recover between clock pulses then modulation will occur.)

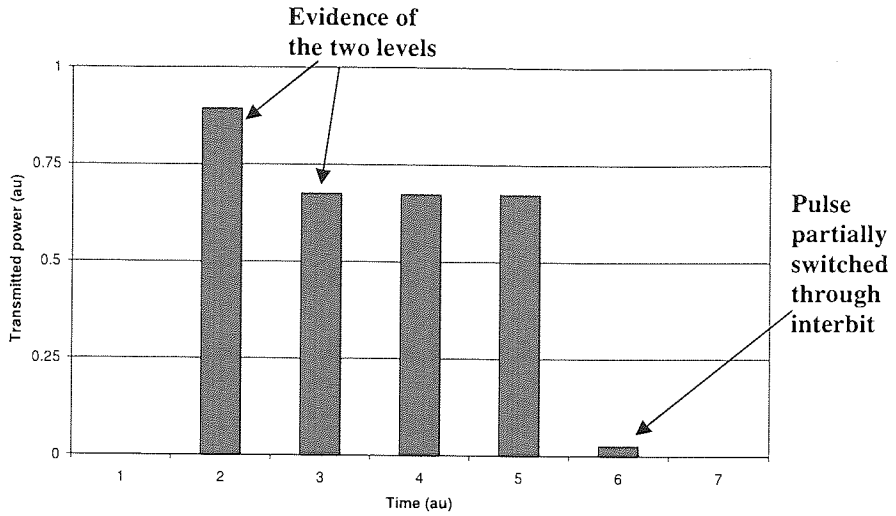


Figure 2-22 Demonstration of a four bit word consisting of (1111) with a higher bit rate 10GHz

Figure 2-22 shows the output to the same four bit word as previously described but this time with the bit rate increased to 10GHz (100ps bit period). Unlike the previous results for 3.3GHz bit rate, here the output has multiple amplitude levels hence indicating some level of inter-bit inference. We can see the mechanism which causes the multiple amplitude levels if we look at the recorded carrier density.

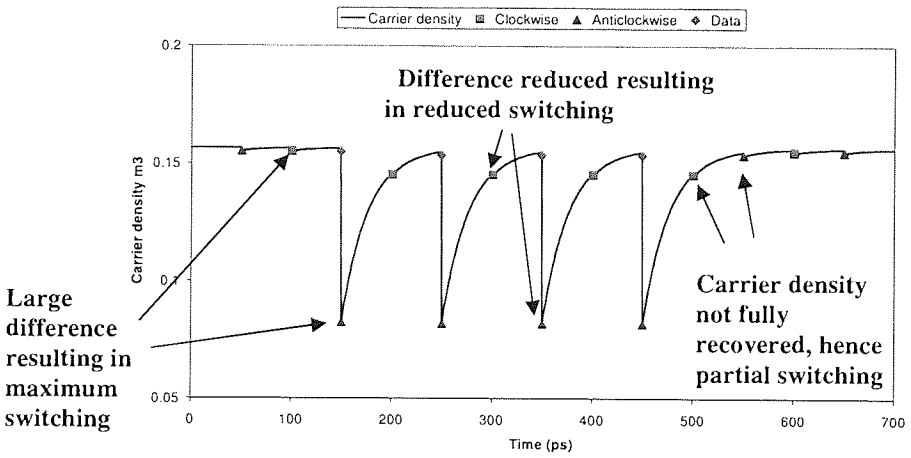


Figure 2-23 Carrier density map for a four bit word 1111 at a higher bit rate

Figure 2-23 shows the calculated time dependant carrier density for the 100ps bit period. As can be seen from the graph, the clockwise pulse of the first switched clock pulse experiences the SOA in a fully recovered state whilst the anticlockwise pulse

passes through the SOA at its maximum depleted state. This difference in the carrier density experienced by the clockwise and anticlockwise pulses generates optimum switching hence maximum amplitude on the output. However, for the following clockwise pulse the SOA has not had time to fully recover. Consequently, the second clockwise pulse will experience the SOA in an already partially depleted condition. Therefore, the difference between the second clockwise pulse and the following anticlockwise pulse is reduced hence, optimum switching is not achieved. This cycle then continues producing reduced switching until there is a 0 in the data. The first clockwise pulse following the final "1" will experience a partially recovered SOA as before, however, as the data consists of a "0" (i.e. no data pulse present to deplete the SOA before the anticlockwise pulse) the anticlockwise pulse will experience a fully recovered SOA. This small difference in the carrier density will cause a small amount of switching, hence the trace of switching on the first "0" after the sequence of ones.

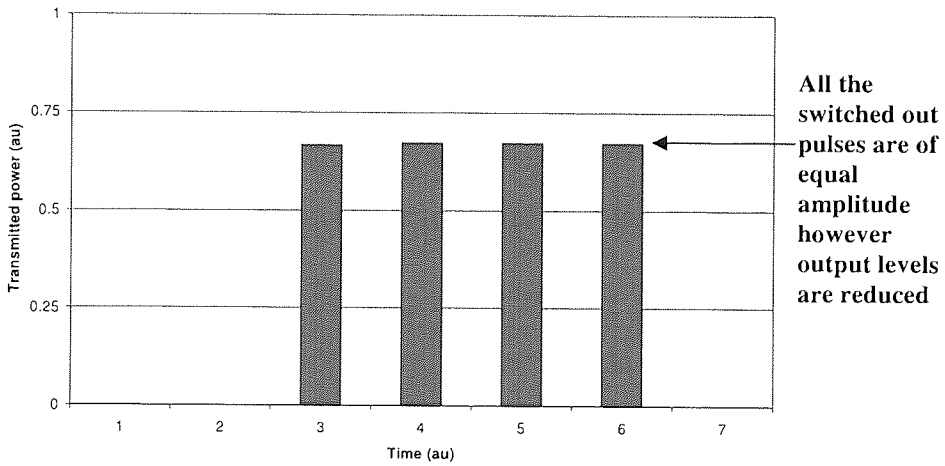


Figure 2-24 Results of the TOAD operating at 10Gb/s using the four bit word "1111" when the data pulse arrives before the clockwise pulse

In previous results the timing of the data ensured that the data pulse arrived in between the pair of clockwise and the anticlockwise pulses. In Figure 2-24 the control pulse timing has been changed so that now it arrives immediately before the

clockwise pulse. As can be seen there is only one transmitted level and after an initial inspection, perfect switching appears to have taken place. However, it is noticeable that there is a reduction in the transmitted power suggesting that complete switching has not been achieved.

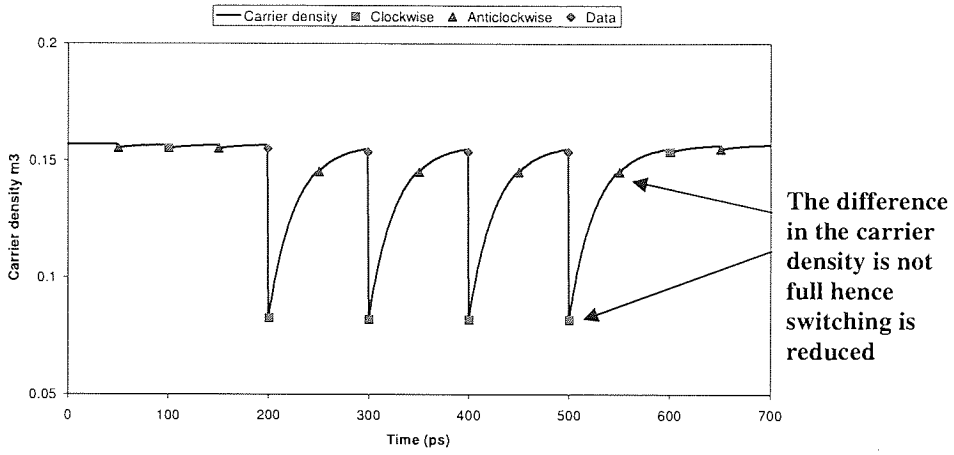


Figure 2-25 Carrier density map showing the carrier density for the four bit pattern with the data pulse arriving at the SOA at the same time.

If we look closer at the carrier density evolution in Figure 2-25 we can see the reason for the reduction in the amplitude levels. It can be seen that although the first clockwise pulse experiences a fully depleted SOA, the SOA has not had time to recover before the arrival of the anticlockwise pulse. As a result, the anticlockwise pulse encounters the SOA in a partially saturated state, hence the differential phase shift is not sufficient to create full switching. By the time the next clockwise pulse arrives the SOA has had enough time to recover and thus no bit interference is evident.

Although this data pulse timing solves the occurrence of the multiple levels caused by the slow SOA, it comes with two main disadvantages. Firstly, because complete switching is not achieved the device is operating on a steep part of the switching curve thus reducing the devices ability to cope with amplitude jitter. Secondly, when

the TOAD is to be used in a cascade configuration the reduction in the transmitted power would result in a greater level of gain required, hence providing more noise potentially causing errors.

2.9. Discussion

With all non-regenerative all-optical storage devices the quality of the stored data decreases with storage time. With the device under study a TOAD is used to regenerate the signal at regular intervals. Therefore, it is important to optimise the TOAD to extract its full regenerative capabilities.

We have shown that by using the symmetrical operating position we can generate maximum extinction ratio on the transmission output. Not only will this improve the quality of the device output but it will also improve the memory storage capabilities through the enhanced quality of the data used for switching.

Using a numerical model of the TOAD, investigations were made regarding the effect of a slow SOA. It has been demonstrated that when the SOA recovery is too slow, inter-bit interference occurs, resulting in pattern dependant multiple bit amplitude levels. The memory, which is the subject of this thesis, feeds the output of the TOAD back into the loop as control pulses, thus any defects in the switching will be exaggerated through successive circulations, as will be discussed in the next chapter.

3. Introduction to the non-inverting memory

3.1. Introduction

In chapter 1 we discussed into the reason why some form of memory is used in an all-optical network system. Also we have looked at different types of all optical memory and their associated advantages and disadvantages. In this chapter a novel non-inverting all-optical memory, constructed of only a single loop mirror, will be introduced. Here the concept will be described and basic characterisations made. Additionally in this chapter the non-inverting memory will be experimentally demonstrated by storing a basic block of data for extended periods of time.

3.2. Inverting memory

It has been demonstrated that a memory function can be achieved by simply connecting the reflected output of a TOAD to the data input as shown in Figure 3-1[85]. More commonly known as the inverting shift register this inverting memory has been demonstrated and investigated many times [86-89]. The inverting memory is equivalent to a shift register with a logical inverter connecting the output to the input.

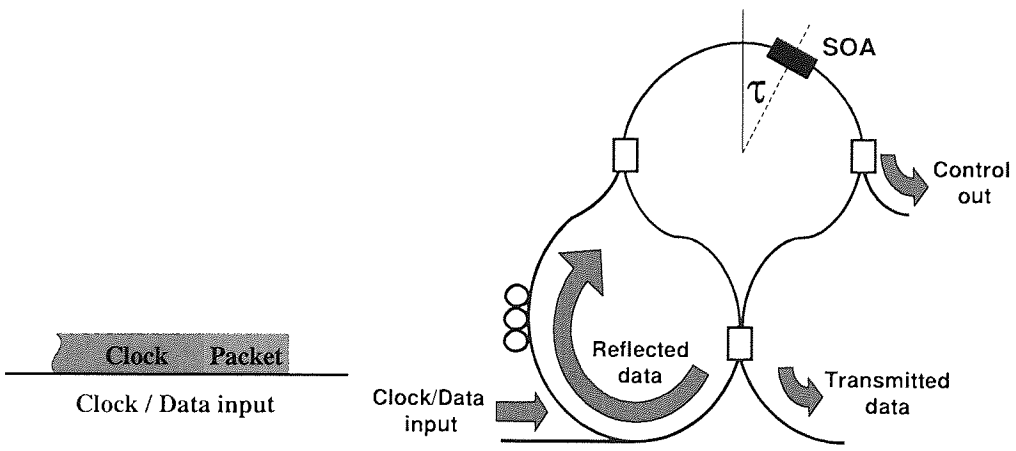


Figure 3-1 Inverting shift register with the reflected port connected to the feedback

With this type of device data is stored by following a sequence of events: firstly the clock supply is turned off. When the clock supply is suspended all data previously stored in the device is removed effectively providing a reset function. Secondly, the initial data, which is to be stored, is injected into the Clock/Data input followed immediately by a sequence of clock pulses, see Figure 3-1. After propagating around the loop the initial data will exit the loop mirror through the reflected port as there are no other pulses to generate switching. A circulator located in the Clock/data input path directs the reflected initial data pulses into the feedback loop where they will be utilised as control pulses. These control pulses are then used to switch out the following stream of clock pulses. The switched out clock pulses will exit through the transmitted port and the remaining clock pulses will exit through the reflected port. The result of this process is that a copy of the data is available at the transmitted port and an inverted copy of the data exits through the reflected port. The inverted copy of the data is directed by the circulator into the feedback loop and will be used as control pulses to continue the storage cycle.

The length of both the loop mirror and the length of the feedback loop determines the storage capacity, S_c, of the device which is given by $S_c = T_l/B$, where B is the bit period and the loop length T_l is defined as the time it takes for a clock pulse, which has not being switched, to travel from the SOA through the reflected output port, around the feedback loop and back to the SOA as the control pulse.

The process described above provides a storage time equal to the round trip time of the memory. However, continuous dynamic storage is only achieved by repeating the cycles until the data is to be retrieved. The inverted copy of the data, generated from the first cycle, exits the feedback loop and enters the loop through the control port.

The pulses contained within the inverted copy will saturate the SOA and switch out the next section of clock pulses. This time the data used to switch out the clock pulses will be an inverted version of the original data. Consequently, an inverted copy of the original data will exit from the transmitted port and a non-inverted copy of the original data will exit through the reflected port providing the next set of clock pulses. This process will then keep repeating itself whilst there are clock pulses supplied to the loop. However, with this form of memory, every time the data is regenerated it is inverted, thereby generating a toggling effect.

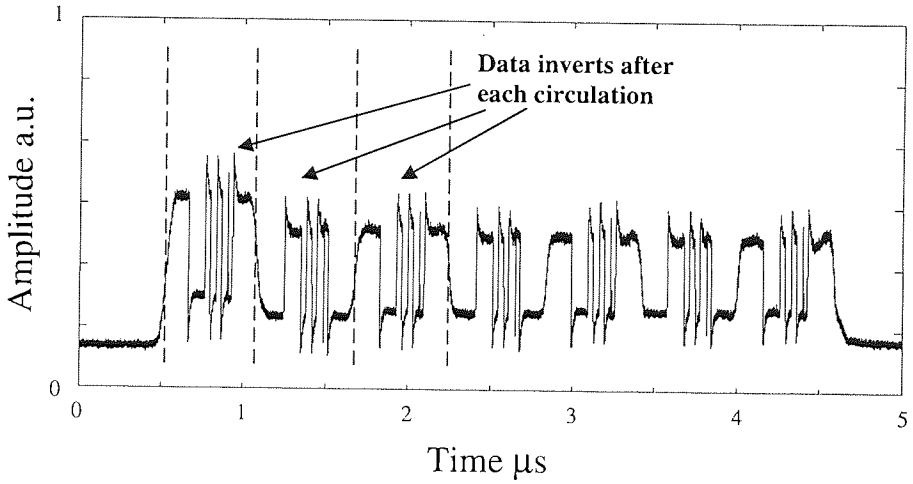


Figure 3-2 Switched output from the inverting memory device. After each circulation the data inverts

Figure 3-2 shows a typical example of data being stored using a shift register device. In this example, the trace is taken from a coupler located in the feedback loop, with the initial cycle showing the first switched out clock pulses. As can be seen, every time the data is regenerated the stored data is inverted.

The characteristic inverting of the data associated with the shift register, results in a higher access time when compared to a non-inverting equivalent. When assessing a storage device one of the most important requirements is the access time (which is

the time it takes to read off the data from the storage device once it has been requested.) With the data inverting, the access time is potentially twice as long compared to a non-inverting device. Additional monitoring of the data's condition (inverted or non-inverted) is also required, adding cost and complexity to the device controller.

3.3. *Non-inverting memory*

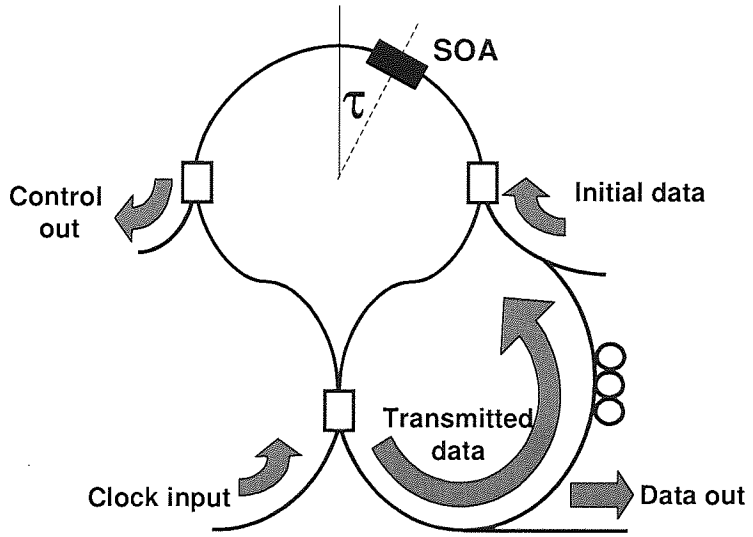


Figure 3-3 Schematic of the non-inverting memory

In the previous section we have seen how data can be stored by connecting a feedback loop to the reflected output. We have also discussed how the data is inverted after every cycle. In this section we will look at a configuration that is non-inverting and hence reduces the disadvantages associated with the inverting configuration. The main difference between the inverting and the non-inverting configurations is the feedback connection. With the inverting memory the feedback is connected to the reflected port, Figure 3-1. Whereas, with the non-inverting memory the feedback is connected directly to the transmitted port, see Figure 3-3. It is this non-inverting configuration that will be the study of this thesis.

As can be seen from Figure 3-3 the data and the clock are now independent and enter the device through two separate ports. If the initial data entered the device through the clock input (as with the inverting memory) it would propagate around the loop and then exit through the reflected output port where it would be lost.

Before any data can be stored the device has to be reset (this ensures that there are no unwanted pulses present in the device which could cause potential errors.) This can be achieved in two ways. Firstly, by stopping the clock supply no residual data can continue to be stored and thus once the data has left the feedback loop it will be cleared from the device. Secondly, interrupting the feedback loop will prevent any control pulses from entering the loop resulting in all the clock pulses departing through the reflected port, thereby clearing the device. Once the loop has been cleared then either the clock supply is resumed or the feedback reconnected (depending upon the method used for reset) this final action serves to complete the reset sequence.

Initially after reset all the clock pulses are reflected and the feedback loop remains empty. Injecting a control pulse will switch a clock pulse out of the transmitted port into the feedback loop. The switched clock pulse will then be directed back into the loop mirror, this time as a control pulse. This single control pulse will then switch out another clock pulse starting a cycle effectively storing data contained in the original pulse. Each time the data is passed around the loop it is regenerated hence; theoretically this data could be stored for an infinite period (in practice the storage time will be limited by the bit error rate of the regeneration process.)

3.4. Numerical simulation

In this section it is the intention to demonstrate the operation of the memory using a simple mathematical model developed using some of the equations already described

in this thesis [73]. The mathematical model will not only demonstrate the operating principles but will allow some simple characterisations to be made.

For simplicity the optical pulse train will be modelled as a set of Dirac delta functions. It is acknowledged that by using a Dirac delta function the effects of pulse shaping and temporal overlap, caused by a small SOA offset and a slow SOA, are not taken into consideration however, for the scope of this model this is acceptable.

The length of the feedback loop is M pulses long and is set to an integer value to ensure synchronous feedback. The carrier density before the *jth* control pulse can be calculated as:

$$N_j^- = K\tau(1-e^{\frac{-B}{\tau}}) + N_{j-1}^- e^{\frac{-B}{\tau}} e^{-\alpha E_{j-M-1}} \qquad (3.1)$$

Where K is defined as equation (1.19) and B represents the bit rate period. $E_{j\text{-}M\text{-}1}$ represents the energy in the j-M-1th pulse that has been fed back into the system. There are no previous pulses at the start of the sequence therefore the equation can be simplified to:

$$N_j^- = K\tau(1-e^{\frac{-B}{\tau}}) + N_{j-1}^- e^{\frac{-B}{\tau}} \qquad (3.2)$$

The carrier density after the control pulse can be derived from equation (1.23) and is defined as:

$$N_j^+ = N_j^- e^{-\alpha E_{-m}} \qquad (3.3)$$

The output of the loop mirror is defined as the power reflected (Pr) and power transmitted (Pt) with Pr calculated as:

$$\mathrm{Pr} = P(1 + Cos(\theta N_j^{-}(e^{-\alpha E_{j-M}} - 1)))/2 \qquad (3.4)$$

where P is represented as the clock power. Pt is defined as:

$$Pt = P(1 - Cos(\theta N_j^{-}(e^{-\alpha E_{j-M}} - 1)))/2 \qquad (3.5)$$

Located in the feedback loop is a gain element to allow for flexibility of the control pulse power. Thus the control pulse power can be calculated as:

$$Pc = GPt \qquad (3.6)$$

As with the experimental device the feedback loop is connected to the transmitted port. To generate storage the initial data is directly injected into the device transferring some of the clock pulses from the reflected port to the transmitted port starting the storage cycle. In all the simulation results in this chapter the initial data packet is recorded as the first circulation of data.

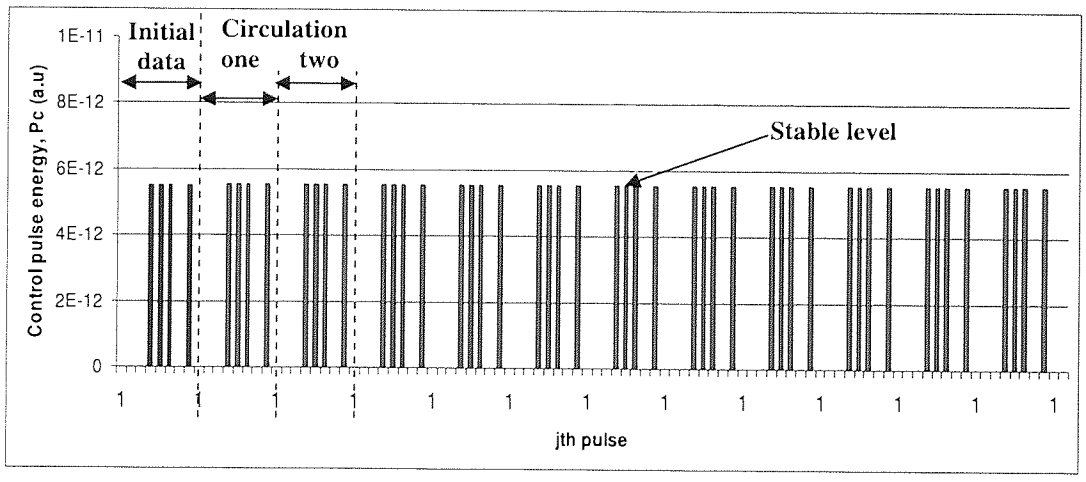


Figure 3-4 Results for the basic numerical simulation for a device with a length of M = 8 bits

The results in Figure 3-4 demonstrates the storage of an 8 bit word "0 0 0 1 1 1 0 1", in a device with a length of M = 8 bits long. Here the initial data input can be seen as

the first circulation of storage. As can be seen, the energy in the initial data matches the energy which is being circulated in the feedback loop, thus no settling time is required.

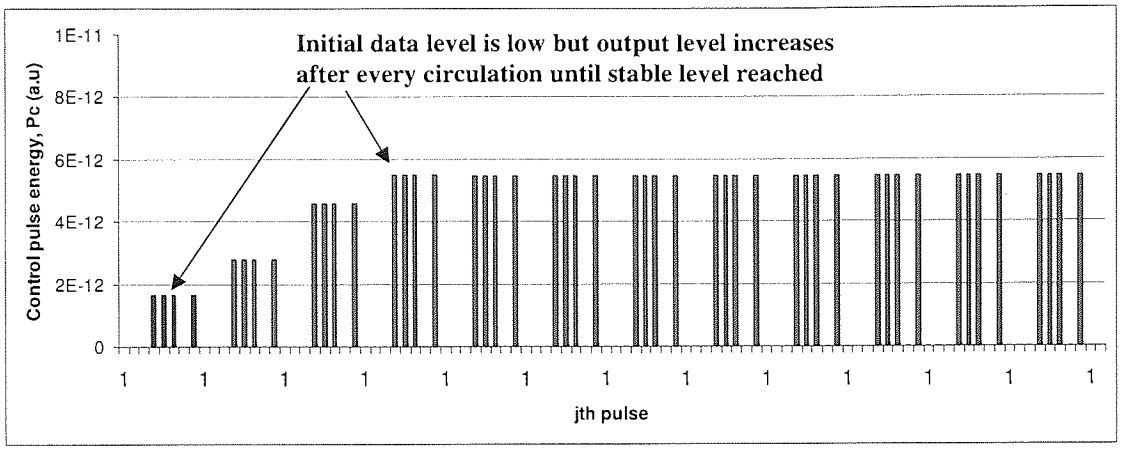


Figure 3-5 Storage of the data for reduced data input

In Figure 3-5 the initial data is reduced to a power that is 1/3 lower than the one used for the results in Figure 3-4. Here we see that although the initial data power is lower the successive circulations of storage increase the power of the stored signal until it reaches the same level as in the previous results. It is here that we first see evidence of a self-stabilising phenomenon. Whereby, within a range of input power levels, after a number of circulations, the power of the stored data resolves to a stable level which is independent of the initial data input power. This also works for a data power that is higher than the stable level however; the observed evolution is slightly different.

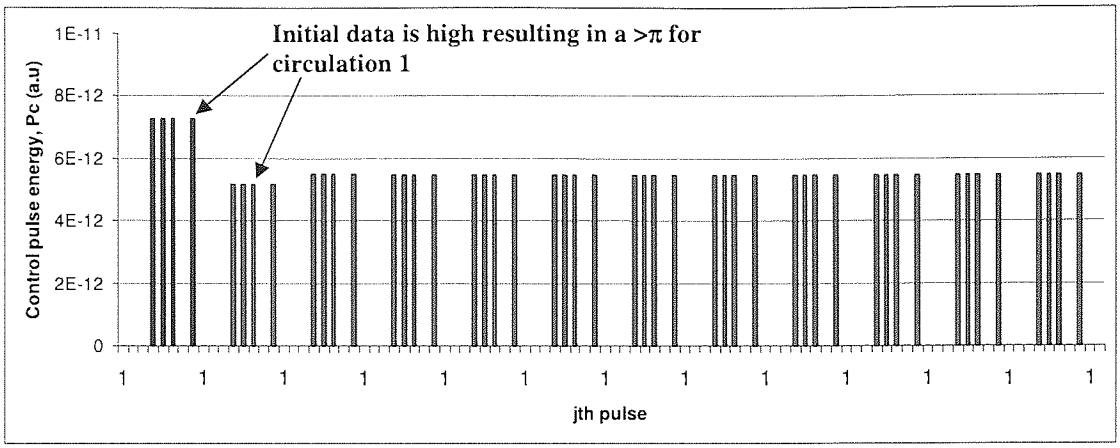


Figure 3-6 Results showing high data input power. The initial data power results in a > π phase shift resulting in a reduction in the output of circulation 1

Figure 3-6 shows the evolution of the control pulse when the initial data input power is higher than the stable level. Although the initial data power is high the stable power level is still reached. With the lower initial data power the successive stored energy levels increased monotonically until the stable power level is reached, as shown in Figure 3-5. However, in Figure 3-6 circulation 1 following the initial data input is lower than the stable level as the transient is now oscillatory.

The numerical simulation used is setup to ensure that the stable power level represents approximately a differential π phase shift. Therefore any control pulse which is higher than the stable level will result in a phase shift greater than π. As we have seen previously a differential phase shift of >π will result in reduced switching. Thus the energy output from the first circulation is lower than the stable level. For the second circulation however the stable level is reached.

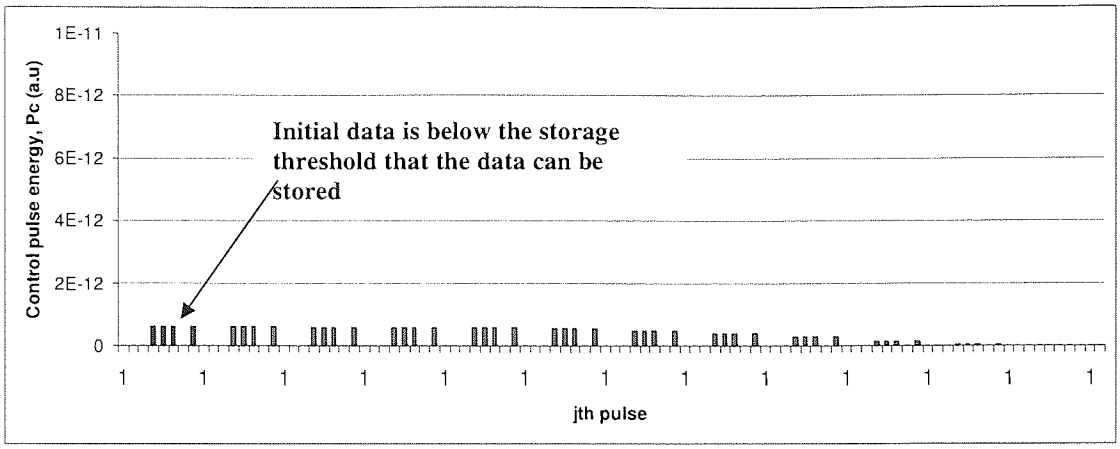


Figure 3-7 Initial data power too low thus the data is not stored

Even in a noise free system, not all initial powers will result in the successful storage of the data. Figure 3-7 shows the results for an initial data power which is too low for the data to be stored (it is worth reiterating that only the initial data power has been changed from the previous simulations all other values remain the same). The switching response for a TOAD means that for control powers operating at the bottom of the switching curve the output energy is lower than the input. Here the initial data power is too low and hence the subsequent control pulse in the next circulation is reduced, this cycle continues until the data is completely lost. Although this limitation provides a lower limit for the control power, this characteristic can be useful to help reduce build-up of ASE and improve the quality of the stored signal when a poor initial data signal is used.

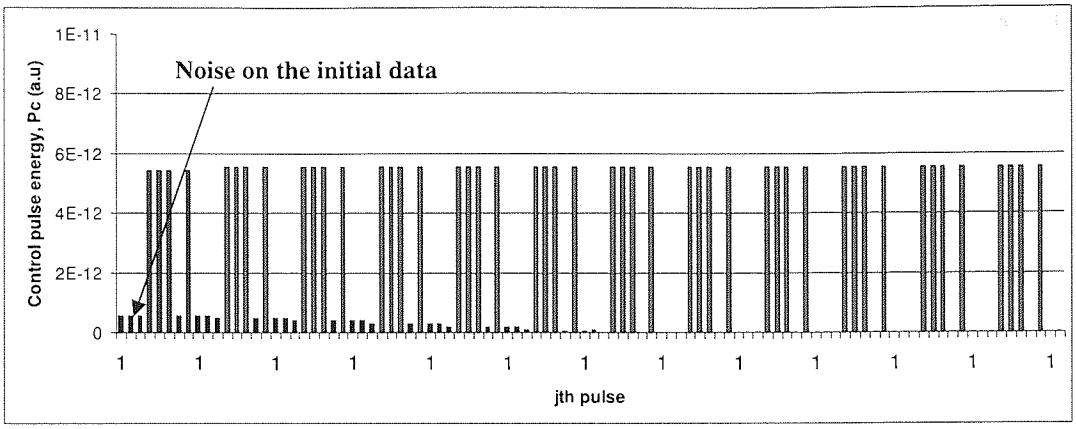


Figure 3-8 Poor extinction ratio on the initial data. The noise is not above the threshold for storage hence no errors.

In Figure 3-8 the extinction ratio of the initial data power has been reduced to provide a non-zero level of the zeros. As we have seen in previous results the signal has levelled off at the stable power level. The energy contained in the noise on the zero level however has reduced through successive circulations, increasing the extinction ratio. This is because the energy in the zero is below the threshold level required for storage, as previously seen in Figure 3-7.

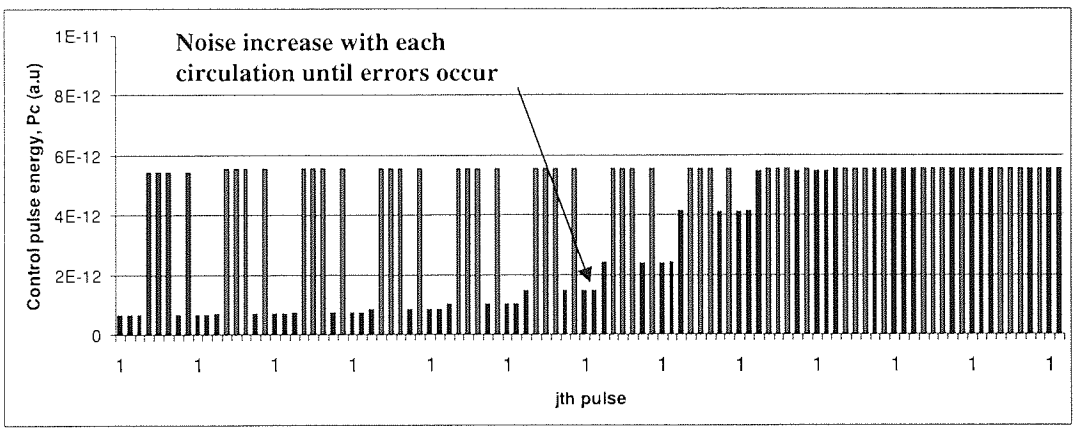


Figure 3-9 Demonstrating the effect of poor extinction ratio on the storage of data. Noise on the zeros is high enough for errors to occur

If the extinction ratio is further reduced by increasing the energy in the noise then eventually the initial zero level will be above the storage threshold. Therefore, the noise will be stored as a bit value of "1" and the extinction ratio will be reduced with

every circulation. This will cause errors and eventually the data will be lost completely as can be seen in Figure 3-9.

In previous simulations we have concentrated on the effects of changing the initial data input power and extinction ratio. These results were taken when the gain in the feedback was set to 1:1, the remaining simulations in this chapter will briefly demonstrate the effect of changing the gain in the feedback.

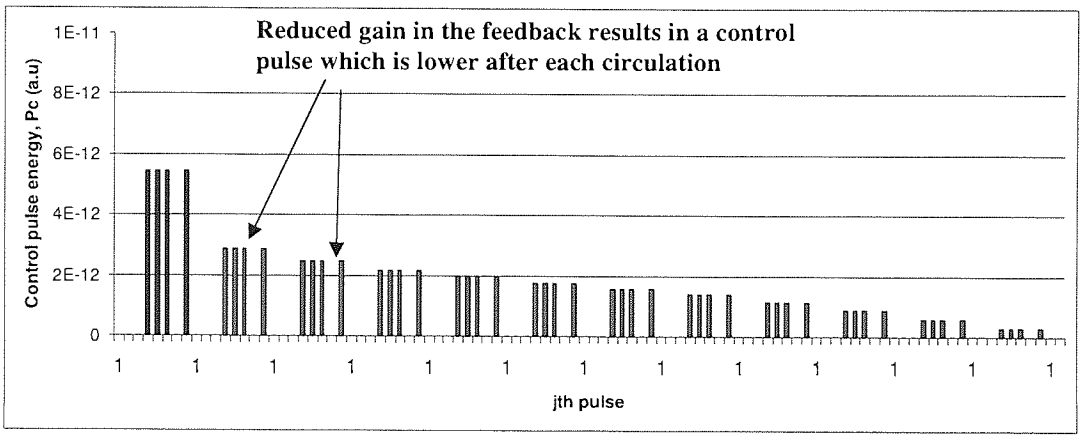


Figure 3-10 Data power is high enough but there is not enough gain in the feedback loop to allow for continuous storage

The overall gain/loss in the feedback loop determines the input energy of the switched out clock pulses as they re-enter the loop mirror as control pulses. If the losses in the feedback loop are too high then the energy of the control pulses, as they enter the SOA, is too low to provide optimum switching. Therefore, there is a further reduction in the energy of the control pulses contained in the next circulation. This cycle will continue with the energy in the control data being reduced after every circulation until the data is totally lost.

Figure 3-10 shows the storage of data where the gain in the feedback is too low for the continuous storage of the data. After each circulation the power of the data stored is reduced every time and eventually results in the loss of the stored data.

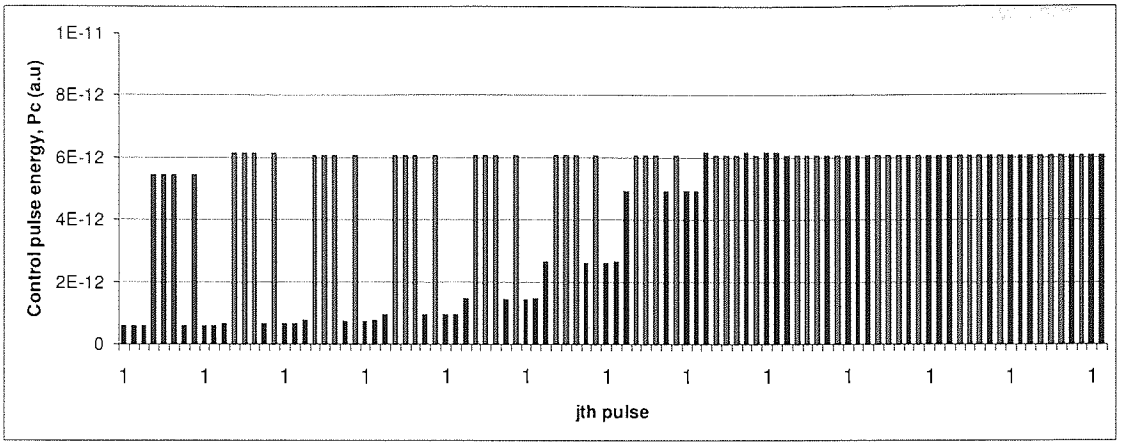


Figure 3-11 High gain in the feedback loop causes a build up of the zero level leading to errors.

Although having too little gain in the feedback can cause the data to be lost, having too much gain can also result in the loss of data. By increasing the gain in the system the overall power of the signal entering the loop mirror through the control port is increased, this applies to both signal and noise. In a perfect noiseless system the gain can be increased freely however, in a practical system there is always a noise floor and a non-zero level of zero. Figure 3-11 shows the result of the gain being increased to 1:1.1, when a poor extinction ratio is present. With the gain set correctly this level of extinction can be managed and even reduced see Figure 3-8. However, when the gain is set too high the regeneration process will insert errors thus, the data is ultimately lost. It is worth summarising at this point that reducing the signals extinction ratio results in an increase in sensitivity to the feedback gain, this will be discussed in more detail later in the thesis.

Previously in this chapter a "stable level" has been discussed. This is the natural energy level at which the device stores the data. Although this level is independent of the initial data power see Figure 3-5 and Figure 3-6, a change in the feedback gain has the direct effect of altering the stable energy level (providing the gain level is set to a

value that still allows for continuous storage of data.) If the feedback gain is low then the stabilisation level is low and if the gain is high then the stabilisation level is high. This is confirmed in Figure 3-12 which shows continuous storage for a reduced feedback gain value of 0:0.9. If we compare this result with the result in Figure 3-8, where the gain was 1:1 and Figure 3-11 where the feedback gain has a value of 1:1.1, we can see that the stabilisation level reduces as a result in the reduction of the gain in the feedback loop.

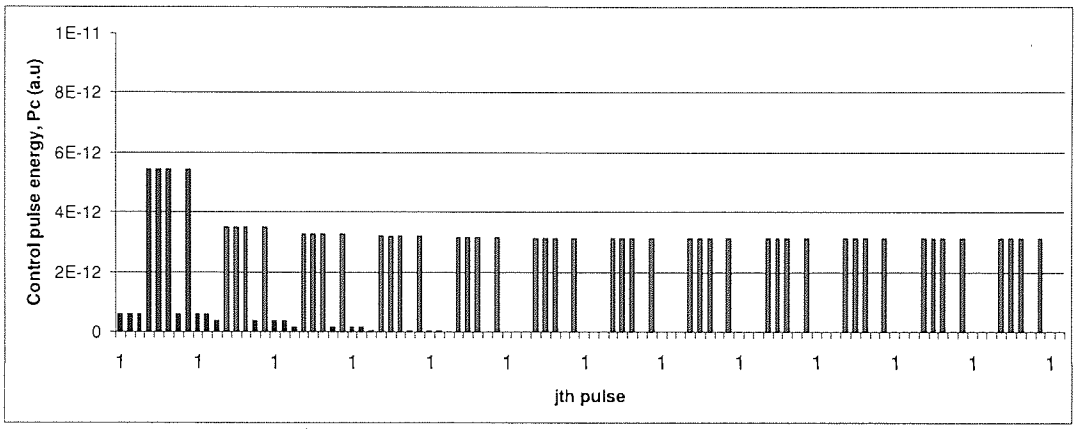


Figure 3-12 Continuous storage with reduced gain showing reduced stabilisation level.

3.5. Basic experimental proof of principle

After confirming the theoretical operation of the non-inverting memory we will now look at demonstrating the concept experimentally. As discussed previously there are two ways the device can be reset to be ready for storage: halting the clock pulses entering the device and blocking the feedback. The storage of data using both methods of reset will be experimentally demonstrated and conclusions will be made.

3.5.1. Experimental setup using the clock as reset

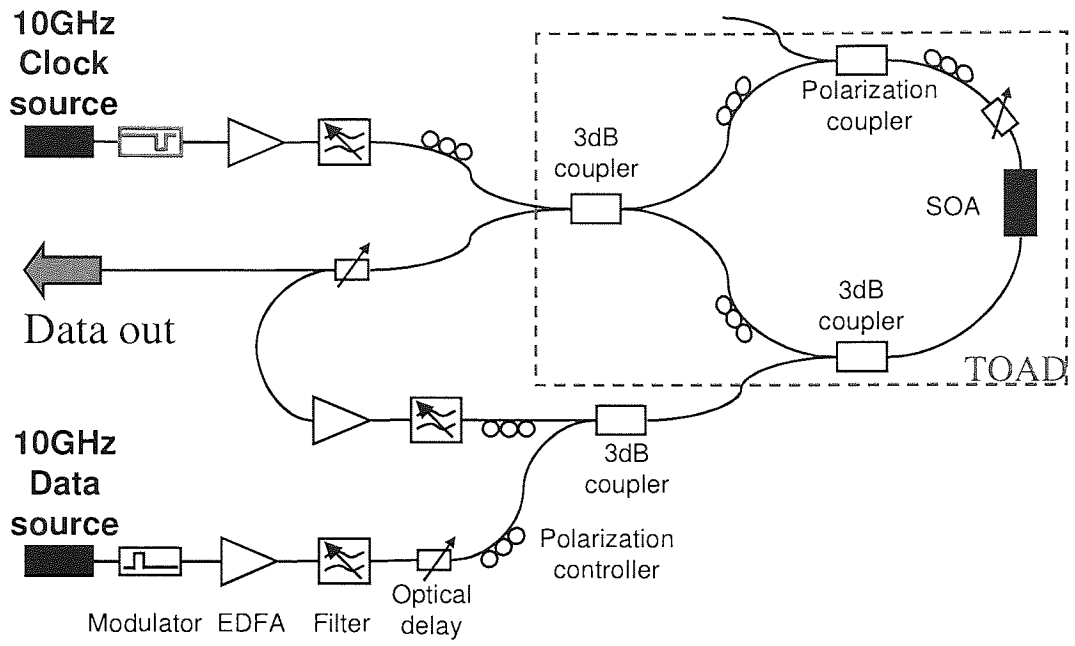


Figure 3-13 Experimental schematic of the memory where reset is achieved by halting the clock pulse supply

This experiment will demonstrate the operation of the non-inverting memory when reset is achieved by halting the clock supply. The experimental schematic can be seen in Figure 3-13 and is set up as follows: Two mode locked fibre lasers provide the clock and data sources operating at 1556nm and 1541nm respectively. In both cases the fibre lasers provide RZ pulses with a pulse width of approximately 12ps FWHM at a repetition rate of 10GHz. Two Lithium Niobate modulators are used, one will apply data to the data path providing a data packet and the second modulator will simply interrupt the clock when device reset is required. The outputs of both modulators are then amplified and filtered to remove excess ASE noise prior to injection into the device.

The loop consists of two 50:50 couplers and one polarization coupler. The single polarisation coupler is located on the opposite side to the loop of the control input, this is to allow for the disposal of the unwanted control pulses after they have been

used, see section 2.3. An SOA provides the non-linear element in the loop with the offset set to a quarter of the bit rate, which in this case is 25ps. The biasing of the loop mirror was set such that a control pulse must be present to generate the π phase shift in the SOA in order for transmission to occur.

To enable storage of the initial data transmitted pulses from the loop mirror are fed into a feedback loop where they are subsequently amplified. The amplified pulses are then filtered and polarization orientated ready for injection into the loop as new control pulses. The timing of the control pulses exiting the feedback loop is controlled through the use of an optical delay line. The control pulse arrival time at the SOA is always synchronous with the clock pulses and thus will always arrive at the same time dependent upon the length of the feedback loop. The length of the feedback loop used in this experiment is ~500ns which at 10GHz equates to ~5000 bits.

The following set of results will demonstrate three full cycles of data storage including: device reset and data write. In this experiment the patterns were set to repeat a pattern of length 24000 bits (240ns) and were stored for a total time of 1.5μs.

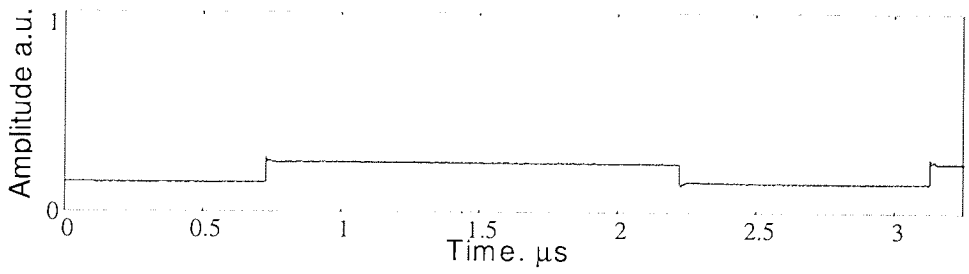


Figure 3-14 Input clock

The clock input to the loop can be seen in Figure 3-14, which consists of a resetting block of zeros 9000 bits long and 15000 bits of ones (enough for three complete 5000 bit cycles).

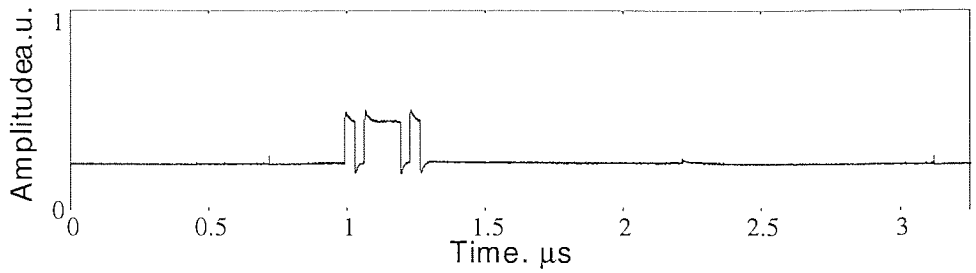


Figure 3-15 Initial data input

Figure 3-15 shows the data pattern injected into the loop. The timing of this data burst must be such that it lines up temporally with the start of the block of ones of the clock.

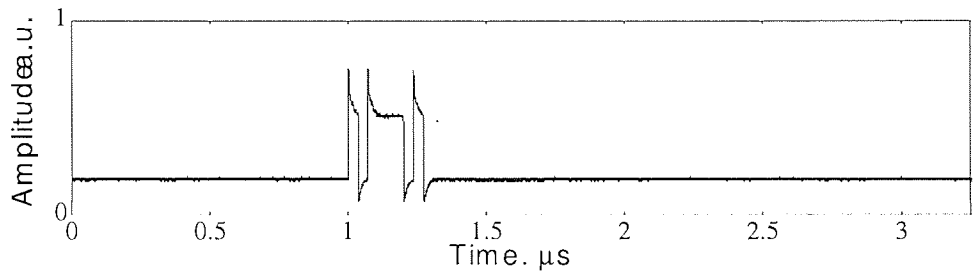


Figure 3-16 First TOAD output

Without the feedback connected, the loop mirror acts as a TOAD with the data switching the clock pulses out through transmission (Figure 3-16). This also shows that in the absence of ones in the data pattern no clock pulses are present at transmission. When the feedback loop is connected the switched clock pulses are used as control pulses creating the cyclic version of the memory.

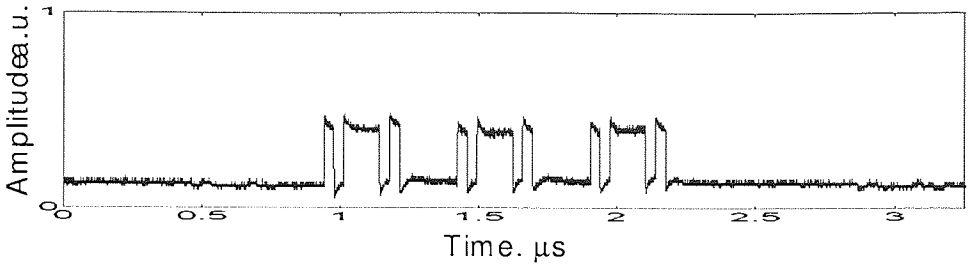


Figure 3-17 Three circulations of storage

In Figure 3-17 the first circulation of data shown contains the clock pulses switched by the original data pulses (as in Figure 3-16), the following circulations are data that have been switched by the circulating clock pulses demonstrating the non-inverting memory function. The reset function can be seen if we compare the output of the device Figure 3-17 with the clock input Figure 3-14. It can be seen that while the clock supply is present the continuous cycle of storage is preserved. However, once the clock is removed there are no pulses to be switched and the cycle is broken.

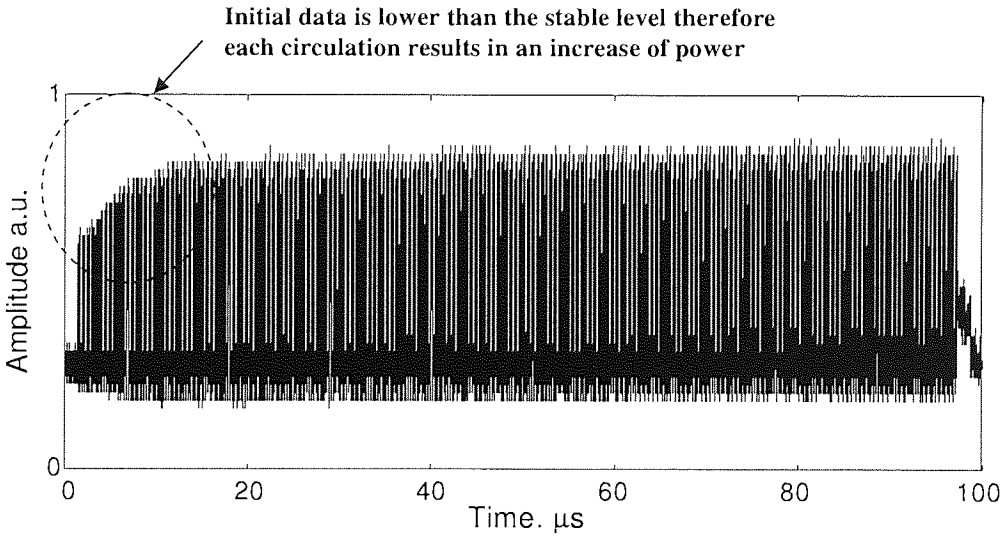


Figure 3-18 Storage over 100µs

After confirming the operation of the non-inverting memory the next step is to increase the storage period. In the next experiment the data was stored for approximately 100 µs as shown in Figure 3-18. It can be seen that after the initial

transient the amplitude of the data stored reaches the stable level, demonstrating the long-term storage potential of the device.

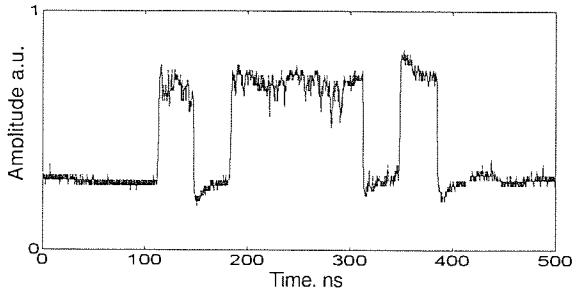


Figure 3-19 Data output after 100μs

Figure 3-19 shows the last cycle of the memory before reset, as can be visually confirmed the data pattern observed matches the original input data pattern in Figure 3-15. Although it has been demonstrated that the operation of such a device using the clock as a reset is possible it is worth noting that visually the device appeared to be very unstable and data was not always stored correctly.

There are two main issues which when combined together explain why using the clock as a reset is inherently unstable. Firstly, when the device is in reset there are no clock pulses entering the device thus leaving the SOA free of any incident light. Therefore the SOA will emit large amounts of ASE increasing the noise in the system (although most of the ASE can be removed using a tunable bandpass filter, the ASE at the signal wavelength will not be filtered out and will be free to propagate around the loop unhindered.) Secondly, during reset the feedback loop is never disconnected consequently any noise generated which cannot be removed will continuously propagate around the loop. This noise level will continue to grow with every circulation until the device is too dominated by noise to allow data to be stored.

3.5.2. Experimental Setup using the feedback as the reset

With both of the clock reset and the feedback reset schemes noise can prove to be a major issue. Both schemes contain a loop and two amplifiers, with the amplifiers providing gain not only to the signal but also to the unwanted ASE noise. The loop gain could easily exceed the loop losses resulting in the creation of a cavity laser and hence induce lasing. It is therefore essential to remove as much noise from the system as possible. The aim with noise management is to ensure that the total system loss for the noise is greater than the signal loss. If the loss for the noise is too low then the signal to noise ratio will decrease after every circulation, until the stored data can no longer be recovered.

One of the most important precautions is to add a bandpass filter after the feedback amplifier. Although this will remove some of the noise, the noise at the same wavelength as the signal will still remain. Additional filtering can be achieved through polarisation. By replacing the 50:50 coupler located at the control input with a polarization coupler the unwanted noise, which is orthogonally polarised to the signal, can be removed (noise which is not orthogonal will remain in the system).

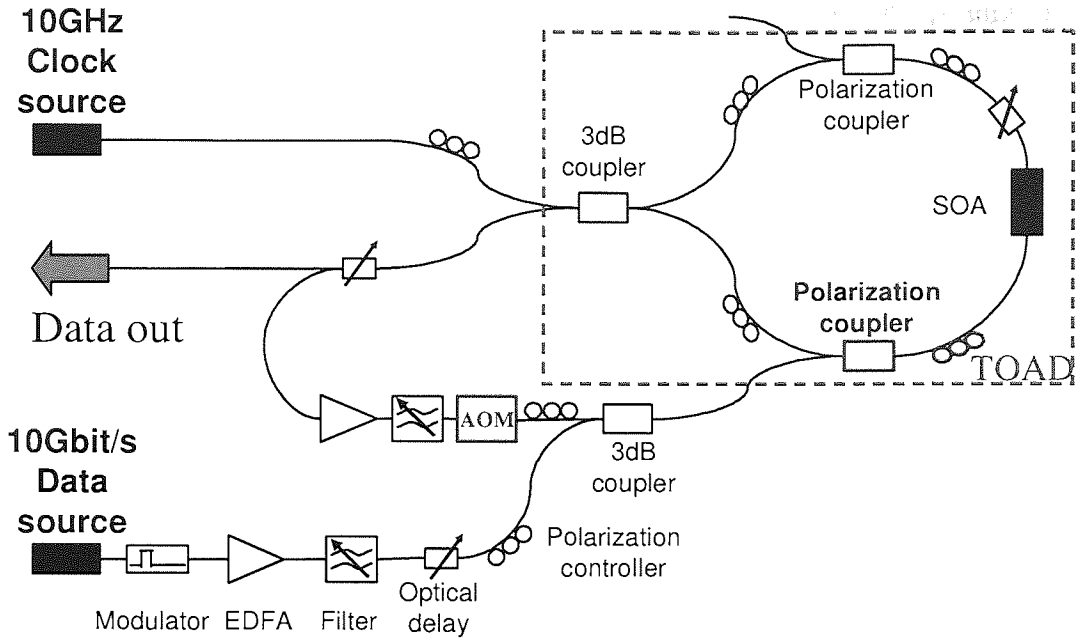


Figure 3-20 Experimental setup using an AOM in the feedback loop to clear the data

The second configuration shown in Figure 3-20 is different from the clock reset scheme in that the reset function is performed by blocking the feedback loop for a time period that is equal to or greater than the length of the feedback loop. In this configuration the need to suspend the supply of clock pulses to the SOA during reset is eliminated. This means that there is no additional ASE generated by an idle SOA, as found in the clock-reset configuration. In the feedback loop of the second configuration the disconnection of the feedback is achieved using an Acoustic Optical Modulator (AOM) see Figure 3-20. The AOM was chosen because of its excellent extinction ratio between the on and off transmission states. The second addition to the experiment is the polarisation coupler, shown in blue, replacing one of the 50:50 couplers. The new polarization coupler ensures that any noise propagating around the feedback loop, which is orthogonal to the signal, is removed again further reducing the noise in the system.

An AOM is introduced into the feedback loop to provide a means of opening or closing it. Opening the feedback loop acts as a reset on the device, this technique provides many advantages. Firstly, because the clock is continuous, there is always a signal propagating around the loop mirror. This ensures that there is less ASE produced from the SOA that would have been produced during the period of reset. Secondly, the AOM in the feedback loop means that it does not have to be connected until data is present in the loop. Hence, there is no loop for lasing to develop thereby increasing the stability of the system. Further noise reduction is achieved by ensuring the feedback amplifier is situated before the AOM, so that any ASE given off by the amplifier, during reset, does not enter the loop mirror.

3.6. Results

The length of the feedback loop (defined as the time taken for a switched out clock pulse to travel from the SOA, out of the transmitted ports, around the feedback loop and back to the SOA as a control pulse) determines the maximum size of the packet that can be stored. Normally the maximum size of the packet would be set slightly lower than this value to allow a guard band between packets (the device works on a bit by bit basis so a guard band is not necessary however one has been included in this experiment in order to clearly identify each circulation). The time taken for one circulation in the experiment described here was 5.5μs and so the size of the stored packet must be smaller than this.

To demonstrate the added stability generated by the addition of the improvements made to remove noise from the system the storage time is increased from 100μs to 1 second. With the length of the feedback loop at 5.5μs this means that for a storage

time of 1 second the data will have to be regenerated approximately 180,000 times. This figure would satisfy the required storage figure of 40 packet slots 4,500 times.

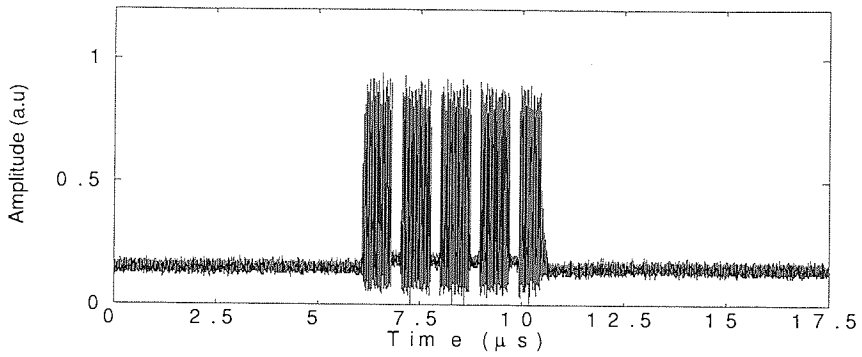


Figure 3-21 The initial data packet consisting of 44k bits of data (equivalent to 4.4μs)

Figure 3-21 shows the original 44kbits data packet or 4.4μs of data consisting of five blocks of ones and four blocks of zeros (this simple data pattern was chosen as this could visibly be seen on a real time oscilloscope). A space of 1μs was included to enhance visual identification of the individual circulations.

After the initial data packet enters the loop the data packet is then stored for one whole second. After one second the feedback loop is blocked which clears all data stored in the memory.

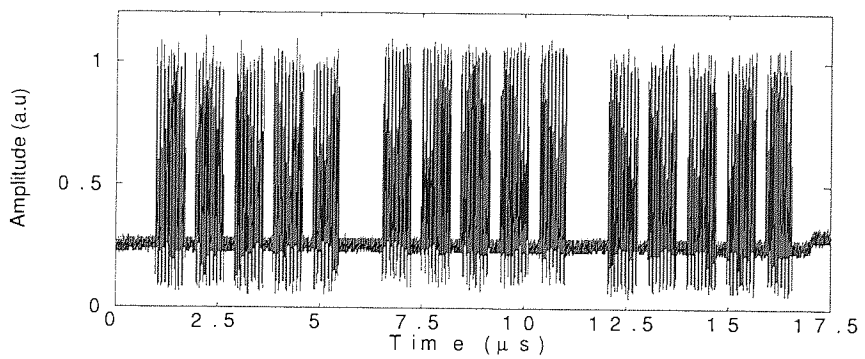


Figure 3-22 The final three circulations of stored data after one second of storage time

Confirmation of storage can be gained by comparing the last three circulations shown in Figure 3-22 and the initial input packet from Figure 3-21. We can see that the packet has been successfully stored for the one second period.

3.7. Discussion

In previous chapters we have introduced the TOAD and explored some of its capabilities. In this chapter we have demonstrated how the TOAD can be configured as an all-optical non-inverting memory. The acknowledgement has been made that a previous example of a TOAD based all-optical memory has already been demonstrated. However, in this solution the data packet is inverted during each circulation. The advantage of a non-inverting memory over the previously investigated inverting optical memory has been discussed.

A simple mathematical model of the non-inverting memory was used to demonstrate some of the basic attributes of the device. Initially the investigation focused on how the device reacts to a change in the initial data power. Here we have seen that within a certain range of initial data powers the data recovered to a stable level with each successive circulation. It was then confirmed that the stable level changed with a change in the feedback gain. By inducing noise (generated by reducing the extinction ratio) it was demonstrated how noise on the initial data was reduced through successive circulations providing the gain is kept low and the power of the noise is low enough. In the next two chapters some of the characteristics of the model will be tested and investigated experimentally.

In the later part of the chapter the simple operation of the device was experimentally demonstrated. The proposed solution consisted of two optical inputs, a clock port and an initial data port (used for loading the memory.) This solution has been confirmed

to be non-inverting and capable of storing a 4.4kbit data packet for a period of 1 second or 180,000 circulations of the loop. We have shown that by using the feedback reset configuration long-term storage of the data can be achieved. Whereas, when using the clock reset technique the system was noise dominated, reducing the potential storage time. Therefore, for the rest of this thesis the feedback reset function will be used.

4. Simple pattern operation

4.1. Introduction

This chapter studies the performance of the experimental device when a selection of the primary operating parameters, such as signal input power, are changed. This is done with the aim of generating an understanding of the operation of the device. The results described here represent the most complete characterisation of an optical memory, which has been achieved. The experiment was set to an optimum working point, where the individual circulations can be clearly identified using a real time oscilloscope, and the selected operating parameters were changed accordingly. A real time image was then recorded for each parameter value with each 2D image consisting of amplitude against time over a 50μs time period. The results were then used to build up a 3D intensity plot. For visual identification a simple data packet was used, consisting of 2 blocks of "1"s separated by one block of "0"s, see Figure 4-1. The 50μs of storage time for each measurement was enough for nine complete circulations of the data.

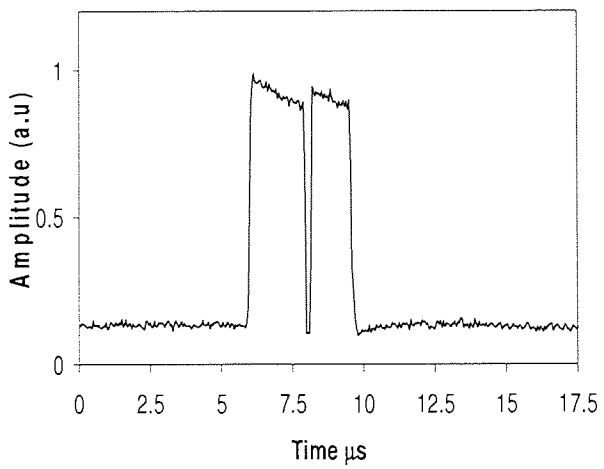


Figure 4-1 Original data packet entering the device

4.2. *Initial data power characterisation*

In this section we study the performance of the memory as a function of the initially injected data packet power. Figure 4-2 shows nine consecutive circulations stored in the memory at four different power levels. A more complete characterisation as a function of input power is shown in the intensity plot of Figure 4-3. Block 1 in Figure 4-2 is the first circulation, switched out by the original data packet, followed by the circulations 2 to 9.

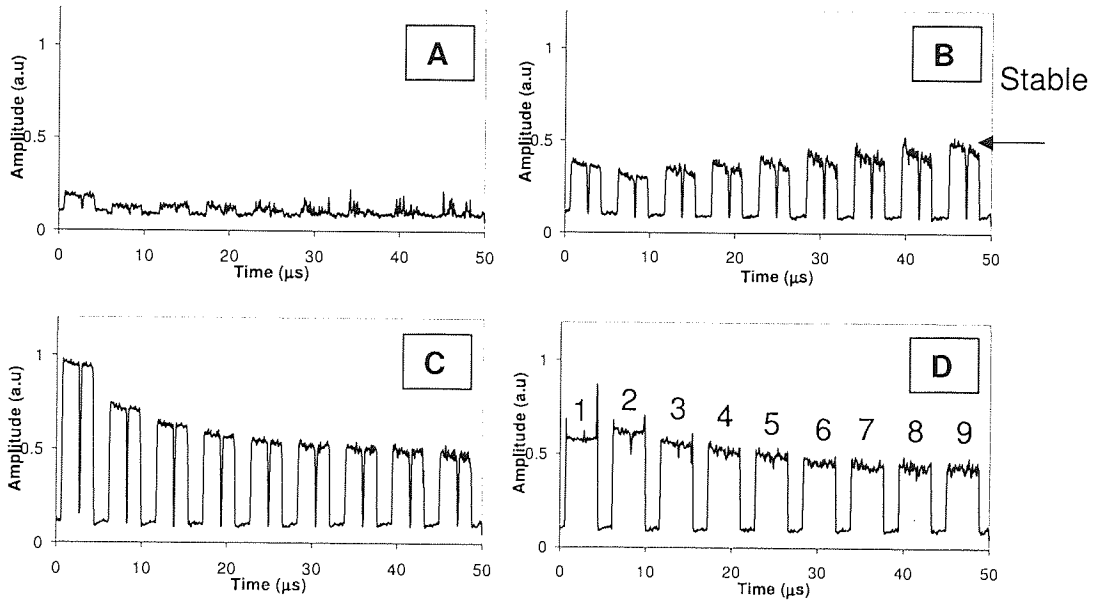


Figure 4-2 2D diagrams showing data stored for varying initial data input powers

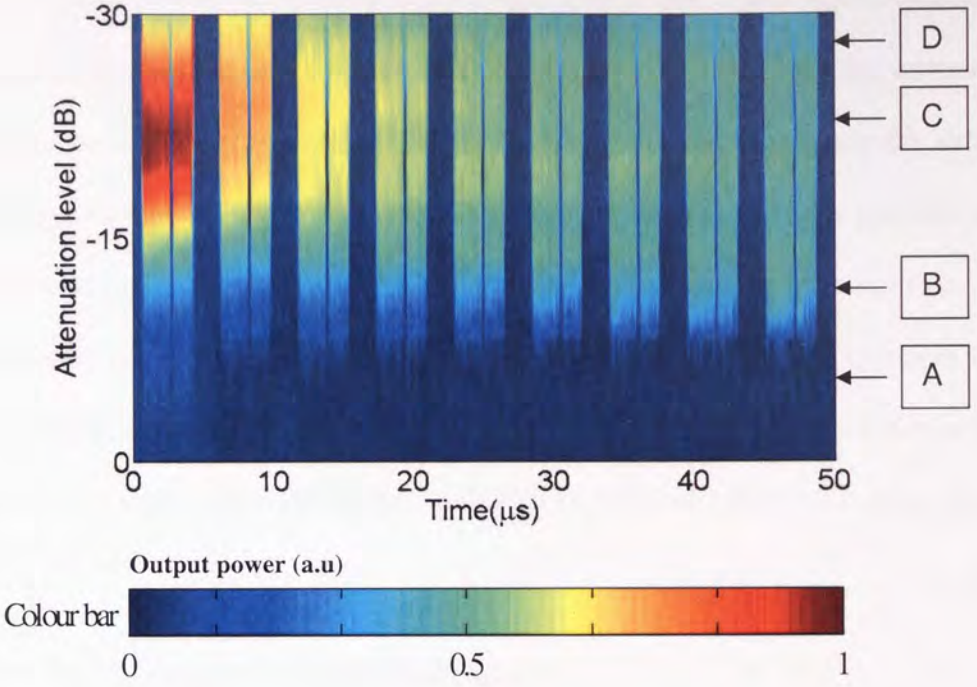


Figure 4-3 3D chart showing change in original data input power

When the power of the initial data packet is too low for storage, Figure 4-2 A, the initial switched out clock pulses, circulation 1, are not high enough in intensity for the device to recover the data to a stabilised level and so the data is lost. This result can be compared to the results in Figure 3-7, generated using the numerical simulation, where it has been shown that a data packet can not be stored when the initial data signal is too low. When the data increases in power, Figure 4-2 B, although the initial data is lower than the stabilised level there is enough power for the data to be stored and after each circulation the level of the ones continues to increase until the stabilised level is reached. This can also be compared with the results generated using the numerical model in Figure 3-5, where the data is stored using an initial data input power lower than the stabilized level. When the initial data power is high enough to cause a full π phase shift, required to provide complete switching, the initial level is higher than the stabilised level, Figure 4-2 C. Therefore, the intensity of the preceding levels reduces after every circulation until the stabilised level is reached. Any further

increase of input power will generate a phase shift greater than π and so the intensity of the initial switched out circulation is reduced Figure 4-2 D. In addition, the increase in the zero noise floor will causes the zeros to turn into ones, corrupting the data. Figure 4-3 shows the full sweep from A to D, in Figure 4-2, in an intensity graph from the point where no data is stored at the lower levels (A) up to where the amplitude of the initial data is too high and definition of the zeros is lost (D). Further increases in input power were limited by the risk of damage to the SOA. However, it has been shown that the device will store the data through a variation of 15dB in the initial data power.

4.3. Initial data timing characterisation

As investigated in section 2.5.1, the arrival time of the control pulses at the SOA, with respect to the clock pulses, defines the switching efficiency of the TOAD. The timing of the initial data determines the output power at the transmission port. Variations of initial data pulse timing, with respect to the clock pulses, are demonstrated in Figure 4-4 and Figure 4-5. By changing the initial data timing, only, it is demonstrated how tolerant the device is to phase wander (defined as the movement of the pulse from the nominal centre of the bit slot) at the initial data input. We have already seen how the device reacts to a change in initial data powers. By adjusting the timing of the initial data similar results should be obtained such that, when the timing is in a poor position then there is not enough switched power for the device to store the data.

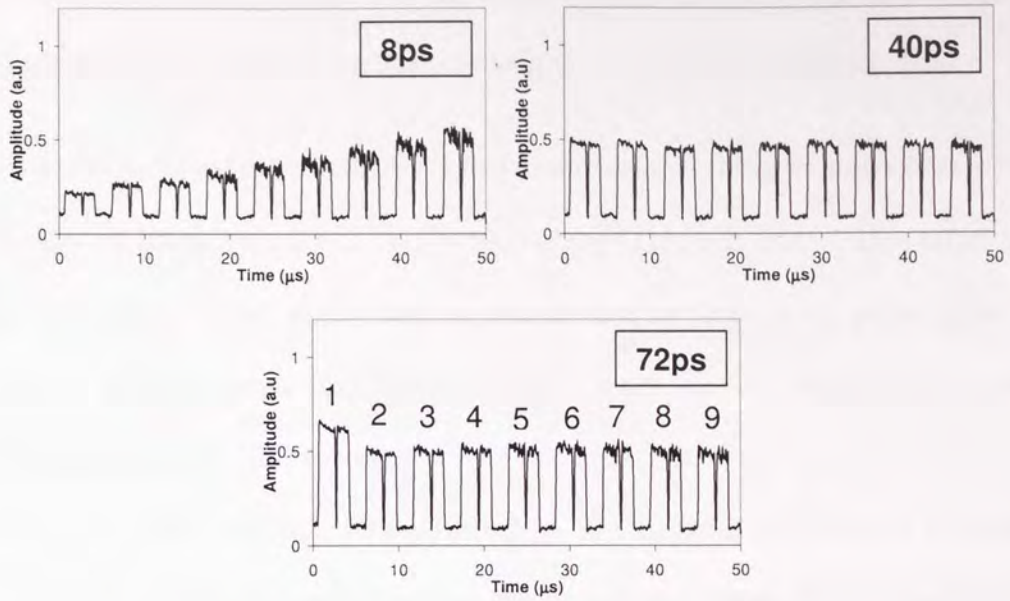


Figure 4-4 2D results showing storage for various data input timings

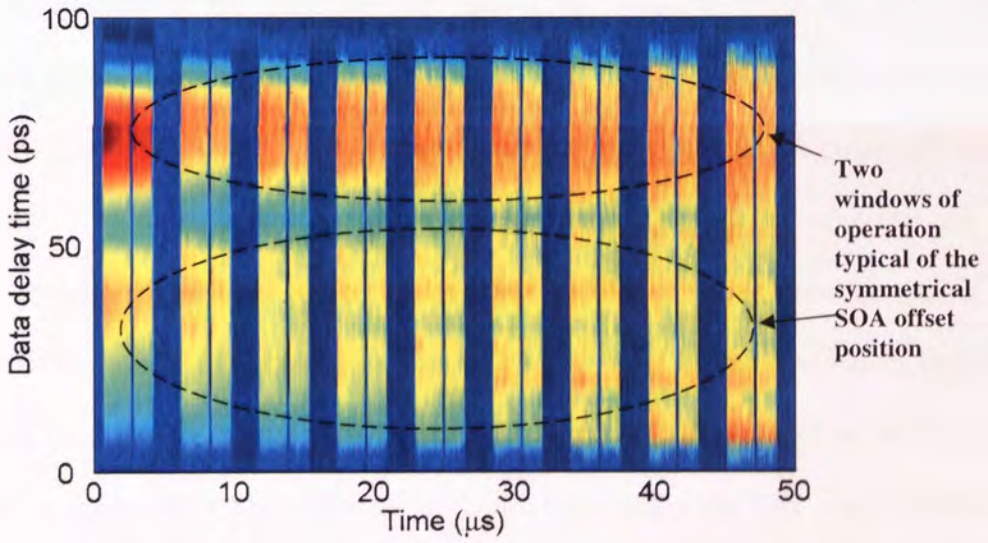


Figure 4-5 3D chart showing data storage with 100ps variation of the initial data input timing

In Figure 4-5 0ps is defined as the position where the initial data timing is such that no pulses are switched out hence the data cannot be recovered and therefore no data is stored. As the timing changes to 8ps, Figure 4-4, the amount of differential phase shift generated in the clock pulses increase, as a consequence the intensity of the switched

out clock pulses also increase. This allows for the consecutive circulations to store the data and recover to the stabilised level, therefore successfully storing the data.

It is at this point to note that there are two prominent switching windows over a delay variation of 100ps, Figure 4-5. The location of the SOA, τ, is set to a 25ps offset from the loop centre, which means that the counter and co-propagating pulses enter the SOA at equally spaced time intervals. As a result, in one window the counter propagating pulses will experience a saturated SOA and in the other window the co-propagating pulse will pass through the SOA in a depleted condition. It is seen by comparing the two optimised operating points from the two windows 40ps and 72ps that one window is better than the other. This phenomenon is due to a combination of the natural balance of the loop and the side of the loop on which the SOA is positioned (this is discussed in more detail in the next chapter), yet in both windows the data is successfully stored. With the initial data timing at its optimum point, which in this case is 72ps, a maximum phase shift will be achieved and therefore the intensity of the output will be higher than the stabilised level. As we have seen in the previous section when the initial data power was higher than the stabilised level, each circulation results in a reduction of power until the stabilised level is reached. However, in Figure 4-4 the output at the optimum switching point 72ps is not greatly above the stabilised level, hence stabilisation is quickly reached. It has been shown that the TOAD's regenerative nature and its self-levelling ability provides for a large tolerance to input phase wander which in this case can be 40ps in the initial data.

4.4. Feedback gain characterisation

This section studies how the gain in the feedback arm of the memory affects the stored data. We have already discussed that the clock pulses, which are transmitted

(switched out), are fed back into the TOAD as control pulses. Therefore, the power of these pulses is dependent upon the gain in the feedback loop and the initial power of the pulses exiting the transmitted port. If the gain in the feedback loop is too low then the intensity of the clock pulses as they re-enter the loop through the control port will be reduced. This will result in the intensity of the next set of clock pulses entering the transmitted port being further reduced. Continuing circulations will result in the cumulative deterioration of the pulses continuing with every circulation until the data is lost. However, if the feedback gain is too high then the overall gain in the device will be greater than the losses. This allows for noise to build up through every circulation thereby corrupting the data. If the feedback gain is set correctly, then the pulses can regenerate correctly, whilst simultaneously suppressing the noise, as demonstrated in Figure 3-8.

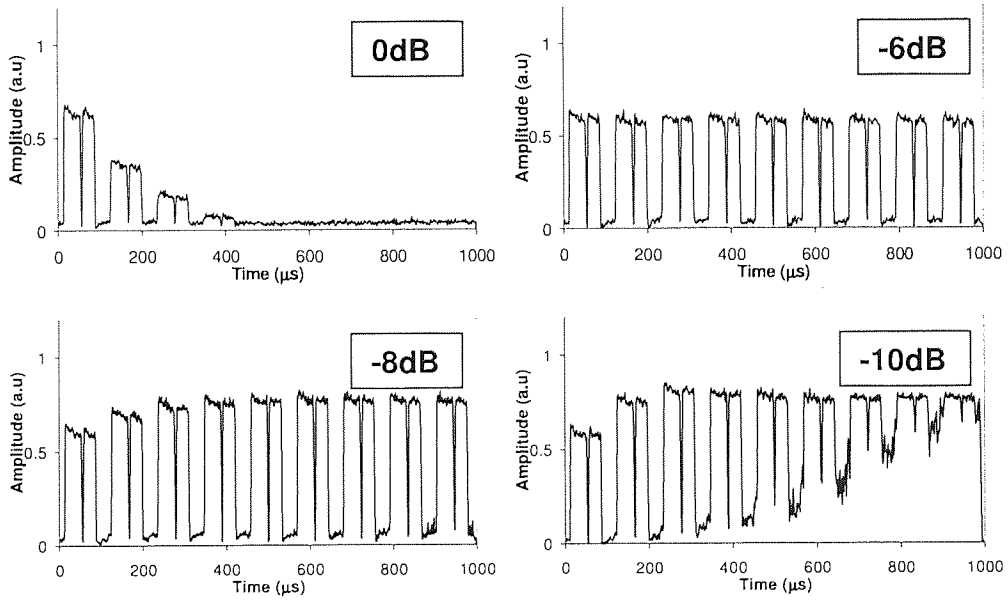


Figure 4-6 2D diagrams for 0,-6,-8 and -10dB of attenuation

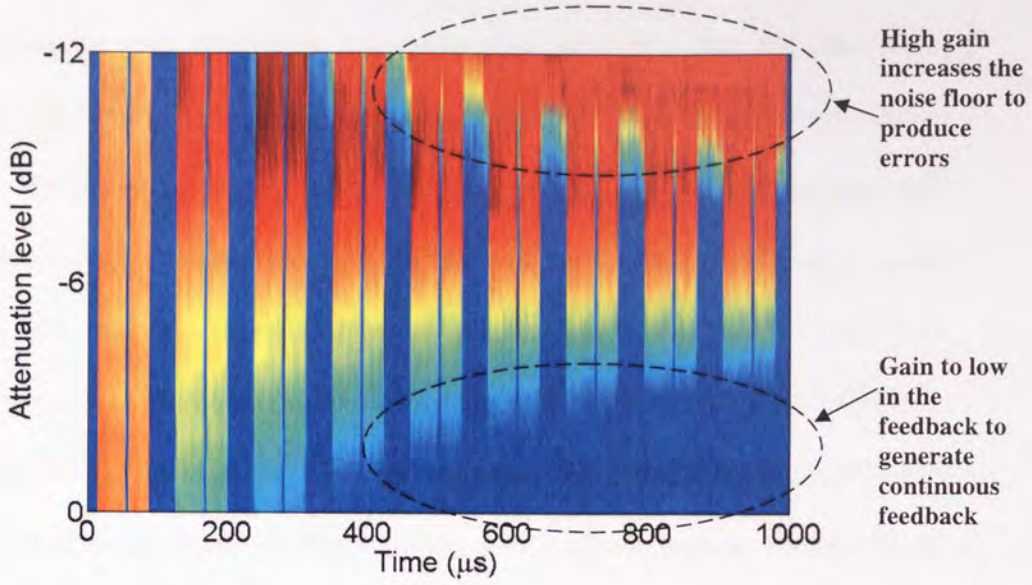


Figure 4-7 Variation in the feedback gain

Figure 4-6 shows the 2D results for feedback attenuation levels of 0, -6, -8 and –10dB of attenuation with a 3D plot shown in Figure 4-7. For this result only, the loop was extended in length and thus a longer packet was used and 9 circulations required 1000μs of time. In the experimental setup the attenuation was applied to the feedback through the use of a Variable Optical Attenuator (VOA). The gain in the feedback is defined as the overall gain in the feedback where all losses are included, not just the gain through the amplifier. Hence, the feedback gain is varied using a VOA located after the amplifier. In this experiment, when the VOA was set to an attenuation level of 6dB, the gain in the feedback loop for the signal will be ~1dB. With the addition of the band pass filters and the polarisation couplers the loss through the feedback loop for the noise is higher by approximately 6dB.

In the numerical simulations Figure 3-10 we demonstrated that even when there is sufficient initial data input power, if there is not enough gain in the feedback arm then the data will not be stored. This is supported in the experimental results where at an attenuation level of 0dB the data is quickly lost after a few circulations. If we decrease

the attenuation levels, effectively increasing the gain, we can see that more circulations are required before the data is lost, Figure 4-7. Decreasing the attenuation further to –6dB results in the successful storage of the data and this will continue until approximately –8dB, see Figure 4-6. In Figure 3-11 the numerical simulation shows that in a system where the noise floor on the zero was significant then too much gain will result in the zeros turning into ones causing errors. We can see the start of this on the experimental device at –8dB of attenuation. However, this becomes prominent at an attenuation level of –10dB. At this point the device successfully stores the data for a short period of time. Subsequently, after each circulation the zero level increases and eventually the noise is at the same level as the ones resulting in errors.

In the previous paragraph a window has been defined in which the gain can be altered whilst the data is successfully stored (that is the window of attenuation between not enough gain to store the data and too much gain so that the data is lost through noise.) Within this window we can see than the gain in the feedback changes the stabilised level, see Figure 4-6. Where we can see that with an attenuation level of –8dB the stabilisation level is higher than with an attenuation level of –6dB. This was first noted in Section 3.4 where the numerical simulation showed that changing the feedback gain alters the stabilisation level.

4.5. Feedback timing characterisation

The ability of the all-optical memory device to store data is dependant upon the condition of the control pulses exiting the feedback loop. Effective switching relies upon two major factors, pulse energy and pulse timing. We have already looked at the impact of feedback gain in the previous section. Here we will look at the effect the timing of the feedback pulse has upon the storage of the data.

With a variable delay line located in the feedback arm we can alter the length of the feedback loop, defining the arrival time of the control pulse at the SOA. As we know from section 2.5, the switching efficiency of the TOAD is dependant upon the arrival time of the control pulse. If the timing is in the optimum position then maximum switching will be achieved and the resulting copy will be of sufficiently high power and the cycle will be able to continue. However, with the wrong timing switching will be inefficient and the switched out transmitted pulses will be lower in power. This means that the gain in the feedback loop will have to be increased to allow for the cycle to continue which will ultimately cause the data to be dominated with noise, as discussed in the previous section.

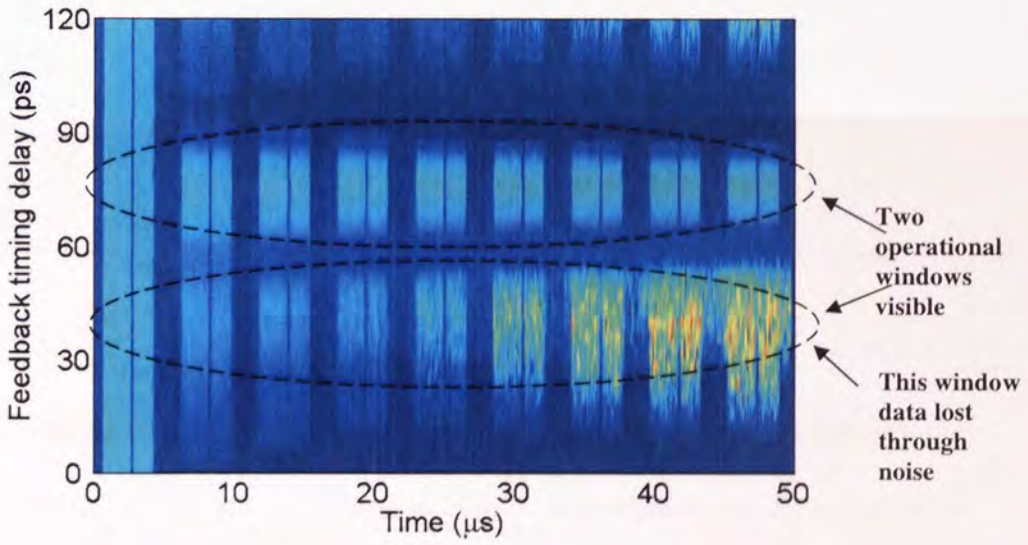


Figure 4-8 Change in the feedback timing

Figure 4-8 shows a 3D plot of the complete results taken for the change in feedback timing. With a total sweep of 120ps, in the control pulse arrival time, we can see a complete window for a bit interval of 100ps (it is worth noting that changing the pulse arrival time by more than 100ps will change the length of the feedback loop by 1 bit, therefore beyond 100ps the results are just repeated.) As found with the initial data

timing sweeps, section 4.3, there are two timing windows. This is because, as discussed in chapter 2, switching is achieved by letting either the clockwise or anticlockwise pulse experience a saturated SOA. If we compare these results to the initial data timing sweep, section 4.3, we can see that the width of the window in which data is stored is smaller than measured for the initial data sweep, Figure 4-5. The cause of this is due to the continuous circulation of the data. With the initial data timing the device can recover a poor switching of the first circulation by having good successive regenerations of the data. If the feedback timing is poor then although the initial circulation of the data is good the successive circulations will all be poor, thus cumulatively degrading the data stored resulting in the loss of the data.

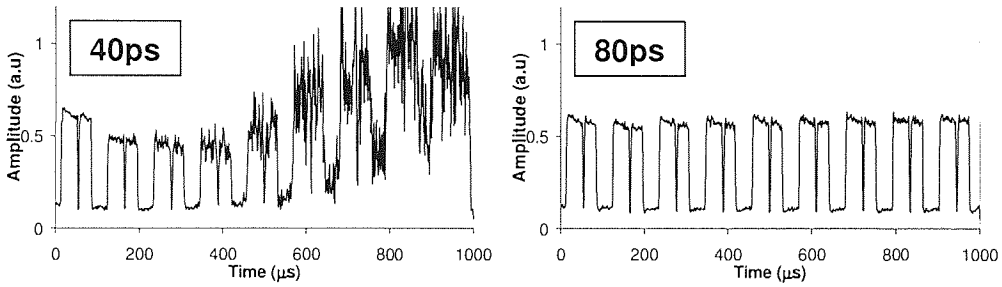


Figure 4-9 2D results for 40ps and 80ps feedback timing

Figure 4-9 shows the data storage results for 40ps and 80ps of control pulse timing offset. As we can clearly see the window at 80ps is better than the window at 40ps. At 80ps the switching is at its optimum point, suppressing the noise and allowing the data to be stored. At 40ps we can see that the second window is not so efficient, therefore, the data is quickly lost allowing the noise to become prominent. Under initial inspection it could be expected that the two windows will be 50ps apart as the SOA is in the symmetrical position. However, due to the finite length of the SOA this is not the case as will be discussed in the next chapter.

4.6. SOA current characterisation

Changing the current of the SOA has two prominent effects. Firstly we have already seen, from the results in section 2.8, that a higher bias current results in a higher SOA initial recovery rate. The second effect is associated with the amplification component of the SOA. By increasing the current in the SOA the gain that is seen by the clock is increased. Although the SOA is not directly located in the feedback loop, the gain provided by the SOA is one of the factors that must be taken into consideration when determining the output of the TOAD and the gain in the feedback loop (the higher the SOA current, the greater the switched clock pulse exiting the loop.) Therefore, by changing the SOA current we should witness similar results to changing the gain in the feedback loop, see section 4.4.

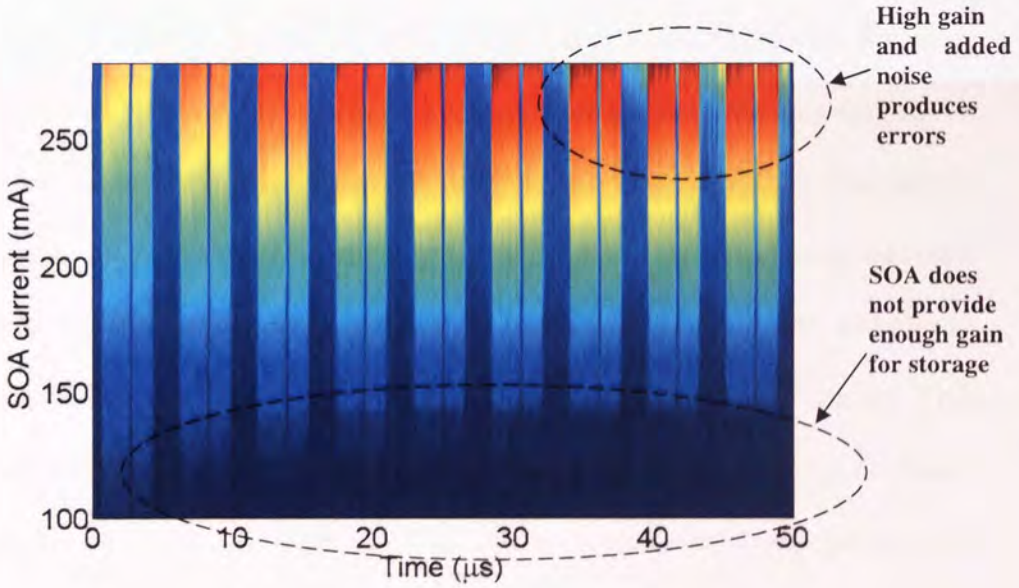


Figure 4-10 Change in the SOA current

Figure 4-10 shows the results when the SOA bias current changes from 100mA to 270mA (or a measured 10dB of Gain variation through the SOA). As we can see at low currents the data is not stored. We now compare the results for the change in the SOA current and the change in the feedback gain, Figure 4-7. We see an extremely

rapid transition from the low gain area, <150mA, where the data is not stored, to the high gain area >150mA, where the data is stored. This is evidence that changing the SOA current has a much greater affect than solely changing the gain in the feedback arm. There is many reasons for this such as: the recovery rate of the SOA may be too slow at low current levels or the control power required to generate switching may have changed. As with the higher gain levels in the feedback, high values of SOA current will cause the extra gain to generate more noise causing errors in the stored data.

4.7. Clock power characterisation

This section investigates how the power of the clock affects the storage of the data. The clock consists of a constant feed of pulses, which enter the device through a 50:50 coupler located at the bottom of the loop and provides the source for fresh pulses, onto which the data is copied. Without the clock source the data can not be stored as there is no clock pulses to which the data can be mapped. If the clock power is too low then the power of the signal entering the feedback arm will be too low. As a result there will not be enough power in the resulting control pulses to completely switch out the next circulation of clock pulses, preventing continuous storage. This can be compensated for by increasing the gain in the feedback arm (although increasing the gain in the feedback also increases noise as we have seen previously.) In addition a low clock power means that the incident light upon the SOA is reduced, thus more noise will be produced from the SOA. The combined result of this effect and an increase in the feedback gain will ultimately produce a noisy system, which will provide a greater chance for data loss.

It has already been shown in section 2.6 that by increasing the clock power the extinction ratio on the transmitted port will improve. Therefore, by increasing the clock power not only will the power of the signal entering the feedback loop be higher (reducing the gain required in the feedback loop) but the quality of the control pulses will improved through an increase in extinction ratio.

We have seen from section 2.7 that as we increase the clock power more control pulse energy is required to provide a full π phase shift. This is because high power clock pulses proportionally remove more gain and therefore reduce the carrier density, clearly requiring the control pulse powers to increase. Ultimately as the clock power increases, too much gain will be removed and the control pulses will not be able to perform the switching so the data is lost (however this level was not tested experimentally due to the risk of damaging the SOA.)

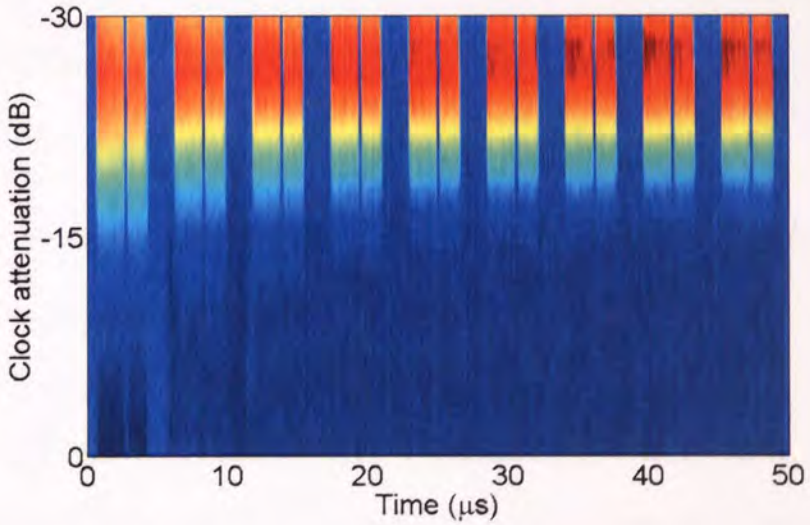


Figure 4-11 Variation in the clock power

The results for the variation in clock power are shown in Figure 4-11. A VOA was used to change the power of the clock signal supplied to the device. As is seen, at lower clock levels there is no evidence of stored data. It is only at attenuation levels

less than approximately -16dB that any storage is evident. But, even at this point the signal entering the feedback loop is too low to sustain data storage and the data is quickly lost. Successful storage can only be achieved when there is sufficient power entering the feedback arm to continue the cycle. This is only achieved once the attenuation is reduced to a value lower than -20dB, which equals a clock power of 15dBm at the SOA.

4.8. Discussion

Although the measurements in this chapter do not supply a detailed analysis confirming the quality of the data stored, they do provide a good initial investigation into the operation of the non-inverting memory allowing comparison with the numerical model.

Varying the initial data power and timing has given an indication as to the memory device's regenerative capabilities and the tolerance to noise. From the results it has been demonstrated that the device is capable of storing data when there is a maximum of 40ps of phase wander and a 15dB variation in the optical peak power.

We have seen how the feedback timing and feedback gain needs to be balanced so that the control pulses exiting the feedback loop enter the SOA at the correct time and pulse energy. We have seen how the SOA current contributes to the gain in the feedback and this will be investigated further in the next chapter. It has also been demonstrated that the correct clock power is essential. When the clock power is too low the power of the signal exiting the transmitted port is too low and hence the device is dominated by noise and the data is lost.

In this chapter we have demonstrated how changing a single parameter can affect the storage of the device. In the next chapter we will look at the relationship between two pairs of parameters, such as both the initial data timing and initial power. We will investigate that within certain windows one parameter can compensate for the other. Also in the next chapter the quality of the data stored will be measured using a bit error rate detector. This will confirm that the degradation of the stored data is independent of the storage time.

5. Bit error rate characterisation of the memory

5.1. Introduction

In the previous section we demonstrated the operation of the memory using a real time oscilloscope to capture packet traces on a slow time scale. Although we can confirm the storage of basic patterns using this method, we cannot identify the individual bits stored within a pattern. In this chapter we test the non-inverting memory device by measuring the Bit Error Rate (BER) of the stored data. Along with confirming that the data has been successfully stored, the quality of the stored data after a selected number of circulations will be measured. This will confirm the non-degenerative nature of the device. As included in the previous chapter the characterisation of a selected number of operating parameters will be measured and investigated.

The BER measurement allows for the performance of a digital system to be evaluated and is performed using a Bit Error Rate Test device (BERT). After the received optical signal has been transferred into the electrical domain (normally using a photodiode), the BERT reads the received data and compares it to a stored data word. The stored data word is a pre-programmed pattern containing the correct data that should be received.

The BERT decides whether the received data bit is a zero or a one in the same way a receiver would as described in section 1.3. At a specific point of time, set by the delay offset, a sample of the amplitude is taken. The sampled amplitude is then compared against the preset amplitude decision threshold. Samples with a value above this level are recorded as a one and samples below this level are recorded as a zero. If the

received bit value does not match the value contained in the stored data word, then the BERT will record an error. It is worth noting that a BER value of $1x10^{-12}$ would mean that one error on average is received in every $1x10^{12}$ bits.

5.2. Bit error rate measurement considerations

5.2.1. Temperature

When measuring the BER it is important to have the memory operating at its optimum position for the entire period of the measurement. All the individual BER measurements taken in this chapter are of data stored after a number of circulations. Hence a burst measurement technique will be used and therefore the number of measured bits per unit time is greatly reduced when compared to a continuous measurement. For example if the total time from the data being stored to being erased is 500 circulations the total packet size would be 1/500 of the total cycle length therefore the total measured time taking into account guard bands either side of the measurement period, plus pattern synchronisation time, could be 1/1000 of the cycle time. In comparison to a continuous measurement this would mean that it would take a thousand times longer to measure the same number of bits. Therefore to allow small values of BER to be measured the operational stability of the memory over time is essential. However, in the experiments, it quickly became apparent that this was not easy to achieve.

The size of the burst measurement window has a minimum value limited by the BERT. For values less than the minimum value the BERT would not be able to synchronise with the data pattern. Therefore, to enable measurements to be taken the length of the feedback was increased by including 1km of SMF. This meant that the

overall length of the stored packet would allow for a bigger burst window and thus provide enough data to allow the BERT to synchronise.

Although the extra 1km of SMF allowed for measurements to be taken, the extra length means an increased sensitivity to environmental changes. The laboratory where the experiment was located was not kept at a constant temperature and, as the length of the fibre changes with temperature so does the delay it provides. The extent of the change is seen in Figure 5-1 which shows a measure of the delay against the room temperature over an overnight period of 17hrs. From the results we can see that for a change of one degree the delay would change by 60ps. It has previously been demonstrated in section 4.5 that the device is sensitive to the feedback timing, which will be further quantified later in this chapter. As a result minor changes in the ambient temperature can drastically change the performance of the device.

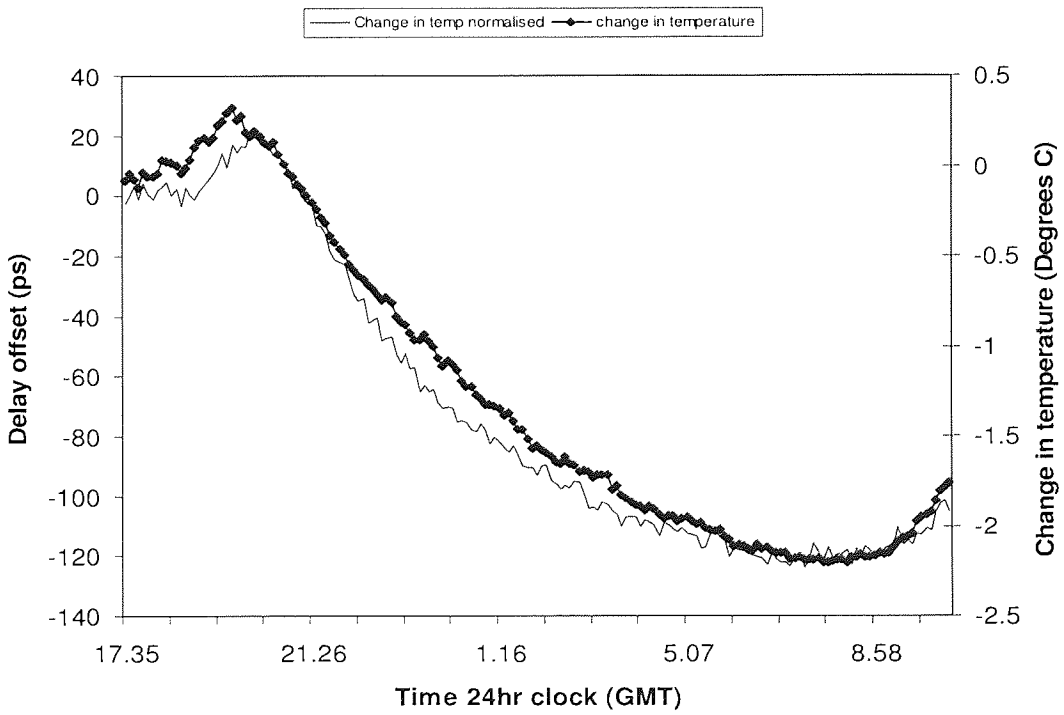


Figure 5-1 Pulse delay through 1km of SMF fibre as a function of ambient air temperature over 12hrs

The combination of the added susceptibility to ambient temperature and the increase in measurement time generated by using burst measurements, make measurements over large samples difficult. For that reason the BER will be measured down to a level of $1x10^{-7}$, unless otherwise stated.

5.2.2. Operational bit rate

In section 2.8 we discussed how a slow SOA affects the operation of a TOAD. For basic patterns, as used in chapter 4 (where the 10Gbit/s data consisted of large blocks of ones and zeros and storage was identified using a real time oscilloscope) this effect was negligible and consequently was not a problem. However, in this chapter measurements will be taken using a BERT which is a more sensitive method of measuring the quality of the signal. Consequently, the errors generated by using a slow SOA as the non-linear element will become apparent after a few circulations. To ensure that there is no degradation of the data stored after each circulation the transmitted output of the TOAD has to be of sufficient quality. When the TOAD is set up to provide maximum extinction (which is required for successful storage see section 2.8), on the transmitted port, the first bit of value "1" following a "0" is of higher power than a bit value "1" which immediately follows another bit value "1" see Figure 2-22. The effect this has on the memory is seen in Appendix D where the evolution of a 10Gb/s data pattern was measured using a sampling oscilloscope. When the bit rate of the data is too high then the amplitude of the second pulse in a pair reduces after each circulation. Therefore when a 10GHz data signal is used, after as little as 5 circulations an error has appeared and the data is lost.

One way to remove the modulation effects would be to use a faster SOA. Unfortunately, this option was not available. As a result, the effective bit rate of the

data was reduced from 10Gb/s (where the bit period was 100ps) to 3.3Gb/s allowing 300ps of recovery time between the data bits (5Gb/s was also tried however the 200ps between each pulse still did not completely remove the modulation effects - the result of which will be demonstrated later in the chapter). For all the following experiments the 3.3GHz initial data pattern was constructed using a 10Gb/s 16-bit data word of 1001,0001,1001,1001. Although the initial data bit rate was reduced, the clock supply remained at 10Gb/s.

5.3. BER curves measuring the quality of the stored data

For long storage times to be possible it is imperative that after each regeneration process (circulation), the quality of the data does not deteriorate. One of the best ways to measure the quality of a signal is to generate a BER curve showing how the bit error rate varies with the receiver input power. As a general rule, the lower the power required at the receiver for a given BER the lower the signal noise. As we have mentioned in section 1.3, if no noise is present then the data could be recoverable from an infinitely small signal. However, in any practical system noise is always present therefore; there is always a non-zero value for the minimum signal power required for complete recovery of the data. Normally when a system is tested it is made as a comparison with a back to back measurement. The power difference between the back to back measurement and the system measurement gives the power penalty. In this experiment the aim is to assess the deterioration of the data after each circulation. Therefore, we will only compare the BER curves of each circulation.

A complete BER curve was generated for a selected number of circulations ranging from 5 to 500. During the recording of the BER curves, the optimum delay and

amplitude thresholds were monitored and BER measurements taken as a function of the received (RX) power.

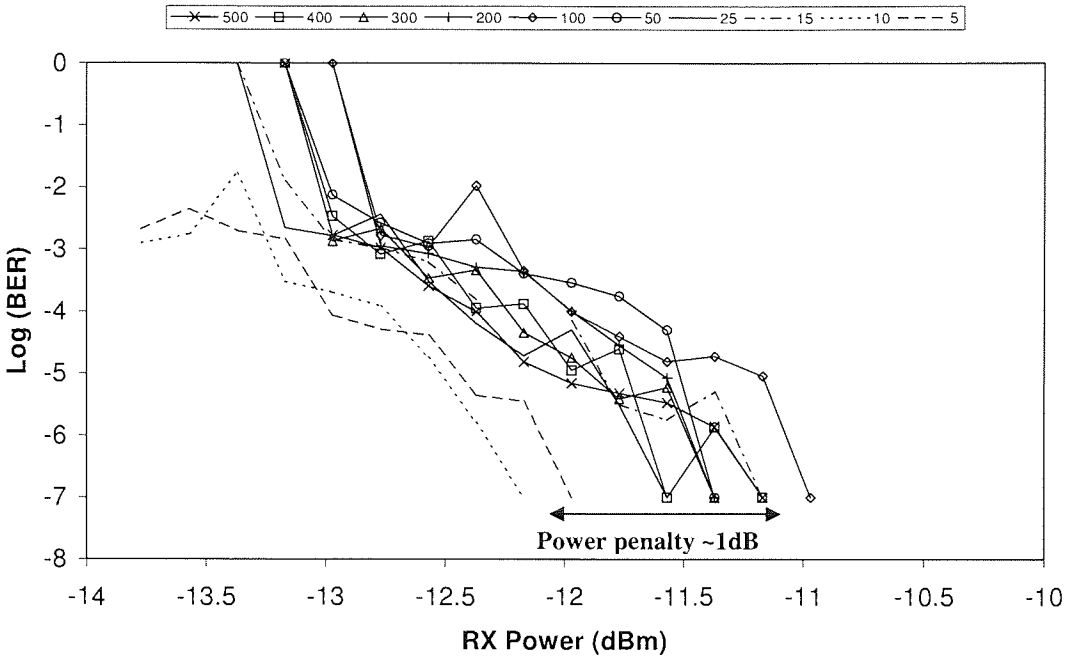


Figure 5-2 BER curves for varying circulations

If we examine the BER curves generated for the memory, Figure 5-2, we can see that circulations 5 and 10 are to the left of the graph compared to the remaining circulations. This means that there is less noise on circulations 5 and 10 hence less power is needed for full data recovery. The initial data to be stored is provided directly by a modulator, thus the initial signal is of high quality. For the initial circulations the quality of the data is continuously reduced until at 15 circulations it reaches a stable point from which the data will not deteriorate further. Therefore, we can see that it is possible to store data for long periods of time. In later sections we will be able to see that the device cannot improve an already high quality pulse.

However, because the device is regenerative we will see that it can improve on an initially poor quality signal.

5.4. Q Values of the stored data

Previously by generating BER curves we have demonstrated how the quality of the signal does not continuously deteriorate for each of the circulations. Another way that this can be shown is to use Q factor values. The Q factor is widely used to specify the quality of the received signal in an optical system, since it is associated with the signal-to-noise ratio required to provide a specific BER. The Q value can be expressed as

$$Q = \frac{\mu_1 - \mu_0}{\sigma_1 + \sigma_0}$$

Where $\mu_{1,0}$ represents the mean value of the marks / spaces rail and $\sigma_{1,0}$ is the standard deviation see Figure 5-3.

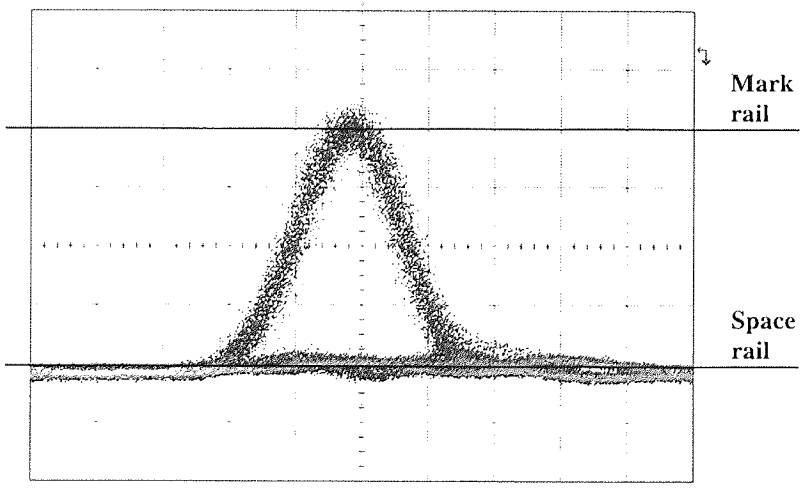


Figure 5-3 Example eye diagram showing mark and space rail

The simple way to obtain the Q factor is to use a sampling oscilloscope to generate a histogram vertically across the widest part of the eye. From this the average voltages and standard deviation values for the marks and spaces can be calculated.

Care has to be taken when measuring the Q values of the memory using a sampling oscilloscope, as this method could produce erroneous results. When using the sampling oscilloscope we are relying on a digital to analogue converter operating on a much lower sampling rate than the speed of the sampled signal. There is also additional noise generated in the receiver itself, which when combined with the slow sampling rate results in distortion of the rails.

The particular issue outlined below (associated with the memory) can occur when measuring individual circulations. Each circulation is a regenerated copy of the previous circulation. This means that it would be possible for an error occurring in a previous circulation to be stored in successive circulations. Although the error may not be at the same level as the other bits initially, successive circulations will ensure that the amplitude level of the error aligns with the rails. This means that when using the sampling oscilloscope to measure the Q factor it would be possible for an error to be hidden in the opposing rail where it cannot to be recognised, thus providing erroneous results.

A method to calculate the Q factor whilst minimising the problems highlighted in previous paragraphs has been developed [90]. Instead of using a sampling oscilloscope to develop a histogram of the two rails, the rails are probed using a BERT, where the decision threshold is varied and the BER is recorded. The results for both the marks and the spaces are then fitted to an ideal Gaussian curve from which the values of $\mu_{1,0}$ and $\sigma_{1,0,}$ can be obtained and from these the Q value can then be

calculated. The problems referred to are either reduced or eliminated by using a BERT, which actually checks the data contained in the signal.

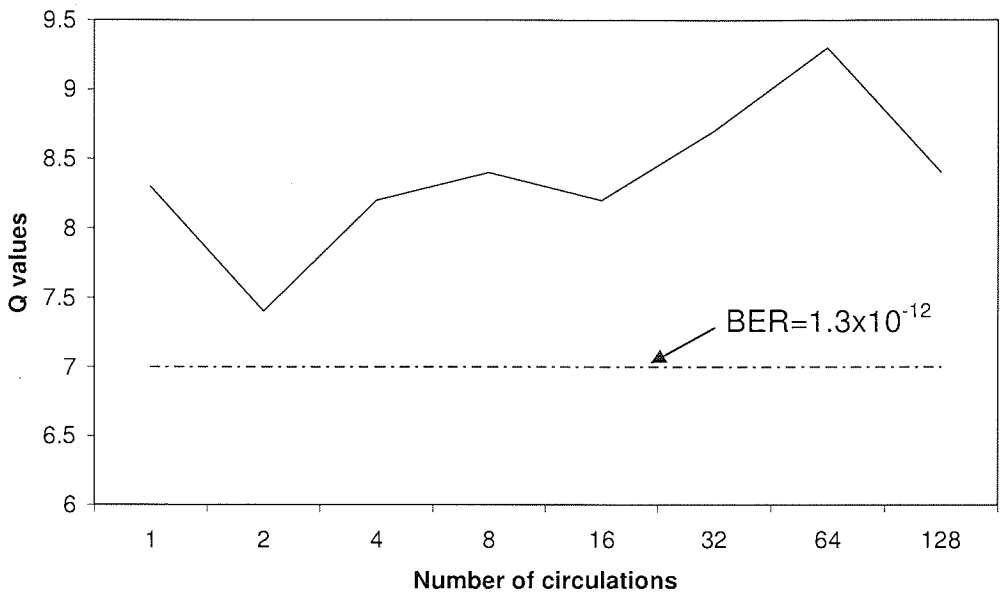


Figure 5-4 Calculated Q values for varying circulations showing no deterioration of the data

The results shown in Figure 5-4 are the measured Q factor values for varying circulations, where the Q factor was measured using the method described above. The Q factor value can be used to estimate the BER using the following equation [91]

$$BER = \frac{\frac{1}{\sqrt{2\pi}} e^{\frac{-Q^2}{2}}}{Q}$$

From this equation it can be seen that a Q factor of 7 represents a BER of 1.3×10^{-12}.As we can see from the results, for each Q factor measurement a value over 7 is achieved indicating a BER value lower than 10^{-12}. It can also be seen that the quality of the signal contained in each circulation has changed very little; therefore, there is no evidence of continuous signal degradation after each circulation. This once again confirms the capability of long term data storage.

5.5. *Intensity graphs up to 1000 circulations*

Previously we have looked at using both BER curves and Q values to confirm the quality of the data after every circulation and the possibility of the long-term storage capabilities of the device. These are standard measurements and are widely used. In this section we will measure the quality of the pulses for multiple circulations by using a less well-used method. However, this measurement will provide a basis for the remaining measurements in this chapter and enable a vital insight into the operation and characteristics of the memory.

As with the previous measurements in this chapter this method is based around the BERT, but this time the timing and amplitude decision thresholds were varied and in each case the BER was recorded resulting in a BER contour map. The main advantage of this method is that the quality of the data for each measured circulation can be quickly compared: i.e. the signal to noise ratio and the shape of the pulses can be confirmed.

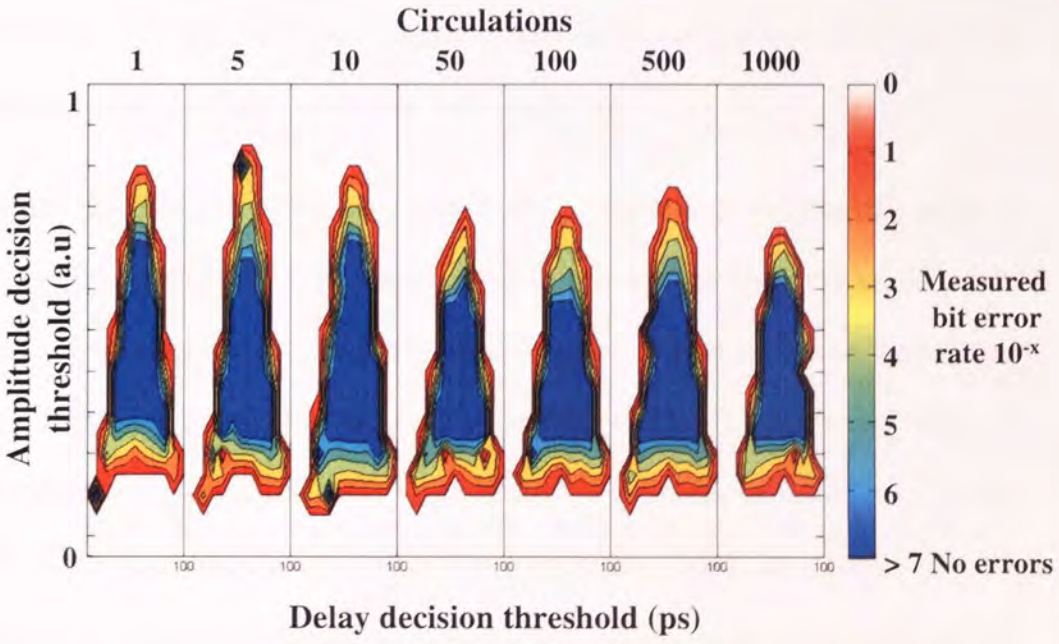


Figure 5-5 3D bit error rate maps for different circulations

The results in Figure 5-5 are the BER maps acquired from the memory for selected circulations from 1 to 1000. The clock was operating at 10GHz therefore the total range of the decision delay threshold was set to 100ps using a 10GHz sampling oscilloscope and a 7GHz narrow band electrical filter. This combination broadened the pulses sufficiently to enlarge the eye to fill the 100ps window without generating intersymbol interference. As mentioned previously, because of the environmental instability and the measurement timescales required, the measured bit error rate was limited to 10^{-7}.

As can be seen from the results in Figure 5-5 the first three eyes are evidently open and the pulse shape can be clearly identified. It is also clear that there is no build up of noise on the zeros and there is minimal noise on the ones. If we look after the initial 10 circulations we can see that the overall amplitude has reduced. As described earlier the amplitude of successive circulations recovers to a stable level. The change in amplitude levels identified in Figure 5-5 is a result of the device finding the stable amplitude. As we can see the shape has not greatly changed for the final 950 circulations. The free of error window (which is the area where no errors were recorded) has not reduced in size over the storage time.

In all the previous results we have looked at the response of the memory using an initially high quality data signal direct from the modulator. The next set of results demonstrates the response of the device to a signal of poor extinction and of low power. The memory device contains the properties of a 3R regenerator which is performed once every circulation. Consequently, this allows an initial poor quality signal to be improved during storage. One of the associated components of a 3R regenerator is the ability to rectify amplitude jitter or improve the extinction ratio of a

signal. The device works by having an input threshold where everything above the threshold is recorded as a one and everything below the threshold is registered as a zero.

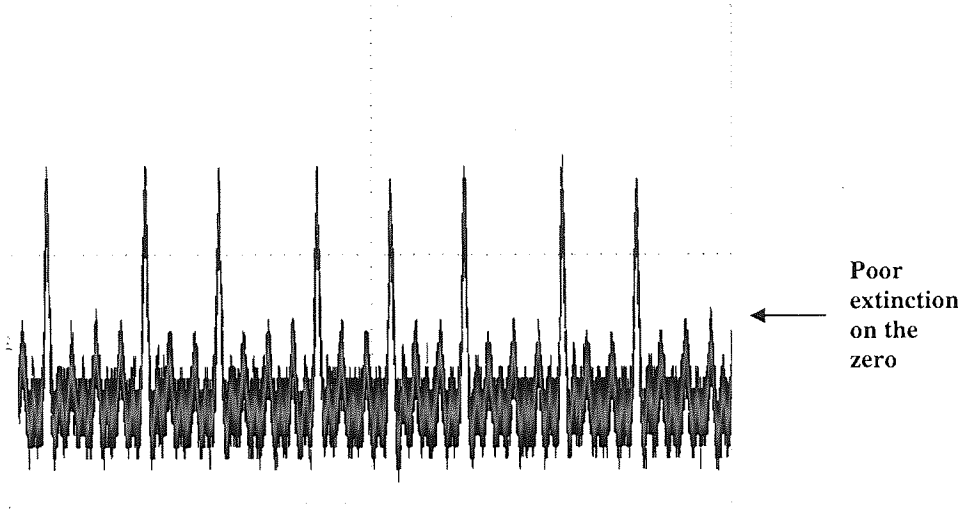


Figure 5-6 Initial data to be stored at the reduced power and extinction ratio

Figure 5-6 is the trace of the initial data, which is to be injected into the device. As can be seen the data is at the 10Gb/s rate with the usual data pattern defined in section 5.2.2.

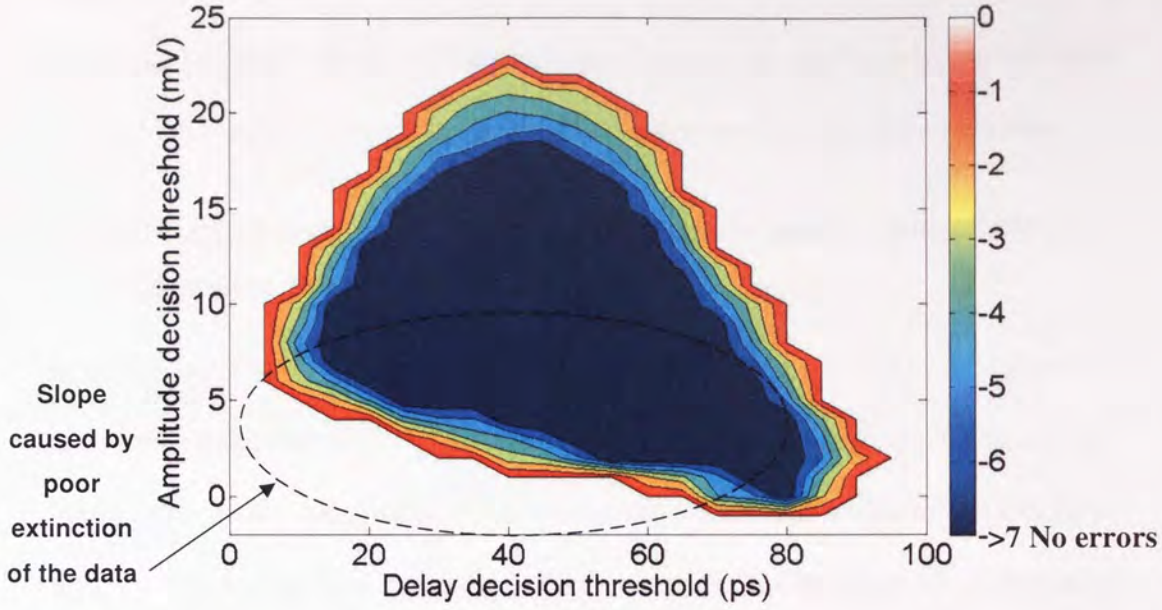


Figure 5-7 3D bit error rate map of the initial data packet pulses before entering the device

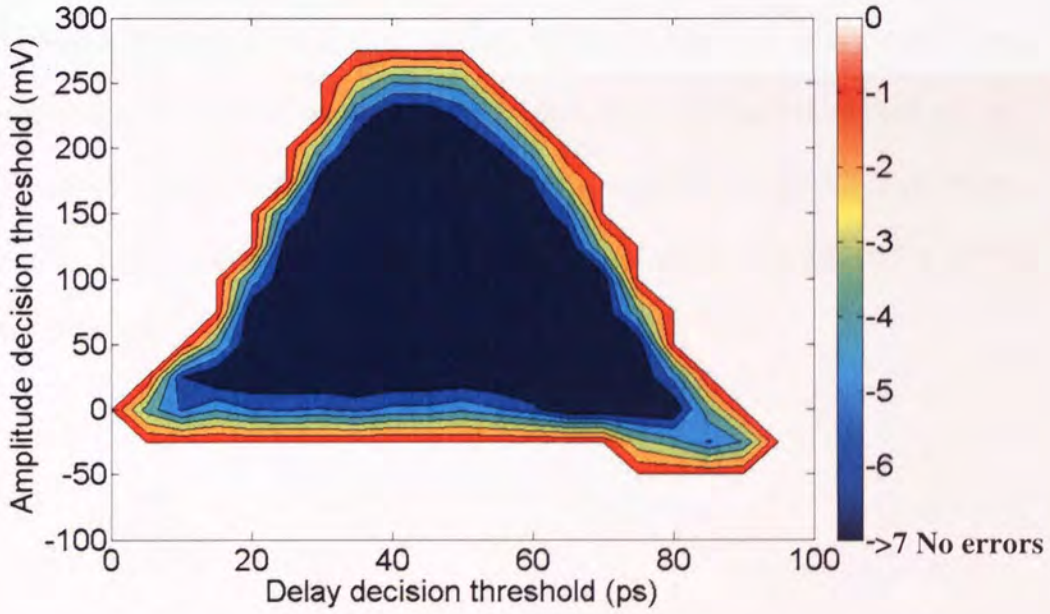


Figure 5-8 3D BER map of the pulses contained in the packet after 250 circulations

Figure 5-7 and Figure 5-8 show the BER maps for the initial input and the output after 250 circulations respectfully. If we compare the two charts we can see that the initial data is of much smaller amplitude than the resultant output from the memory. In addition we can see that the zero line of the BER amplitude decision threshold is

higher in the original data than the output. This indicates how the extinction ratio of the device has been improved. The map also illustrates the trailing edge on the initial data has been reduced as well, confirming the improvement in the extinction ratio.

5.6. *Initial data power attenuation characterisation using BER measurements*

In section 4.2 a basic pattern was used to investigate how the power of the initial data affects the storage capability of the memory device. It has already been discussed how through successive circulations the power of the stored data settles to a stable level, which is independent of the initial data power (section 3.4.) For example a high initial data power will be reduced to the stable level and a low initial data power will be increased to the stable level.

For the first half of this section three separate 3D BER maps will be generated. The first map will be the measurement of the initial data; the second and third map will be the 1^{st} data circulation and the 250^{th} circulation respectively. All the 3D maps in the initial part of this section will demonstrate the BER results for changes in the initial data power as a function of the amplitude decision threshold level.

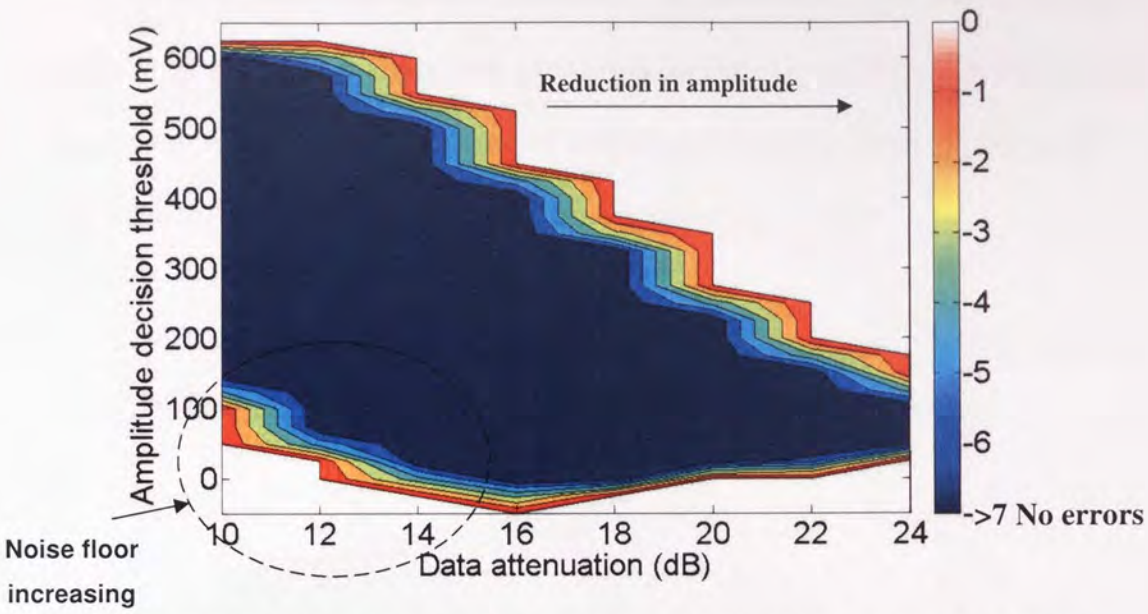


Figure 5-9 BER Amplitude threshold of the initial data before entering the loop

Figure 5-9 shows the BER map for the initial data: the horizontal axis represents the attenuation applied to the data while the vertical axis represents the amplitude decision threshold on the BERT. Here we can see the results for a range of attenuation levels from 10dB to 24dB on the initial data path (further reduction in the attenuation would result in damage to the receiver) Figure 5-9. At attenuation levels of less than16dB we can see evidence of a noise floor on the zero level, which increases as a result of the reduction in the attenuation. As the attenuation is increased beyond 16dB the window decreases in size as the one level is reduced.

The initial data is used to switch out the first copy of the packet providing the first circulation. As this first circulation is directly switched out by the initial data it is this circulation that is mostly affected by the change in the initial data power. When the attenuation level is high the control pulses from the initial data packet do not have sufficient energy to allow the data to be recovered. As the attenuation of the initial data packet is reduced there is more energy in the control pulses and successful recovery of the data from the initial data packet is possible. The power of the data

switched out is raised with further decreases in data attenuation until there is enough power to generate full π phase shift (maximum output power.) Further decreases in attenuation, resulting in increases to the control pulse power, forces the phase shift past π and therefore the output signal of the 1st circulation is reduce.

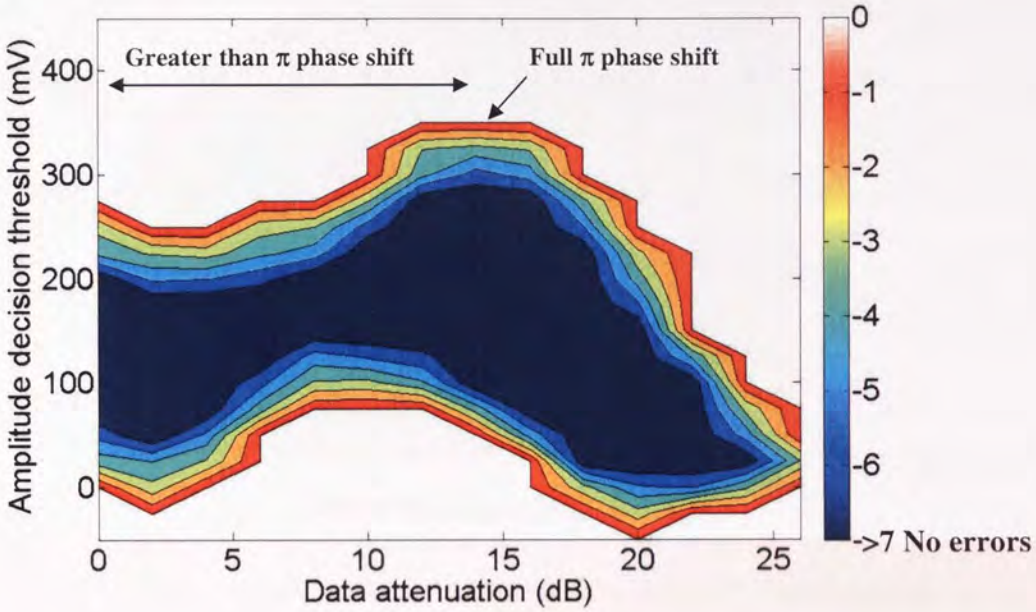


Figure 5-10 BER amplitude threshold sweep for varying attenuation levels after the first circulation

Figure 5-10 shows the resultant BER map of the 1st circulation for varying initial data attenuation ranging from 0dB to 26dB. Here we can see that at data attenuation levels greater than 24dB the data cannot be recovered. Between 24dB and 14dB of attenuation the data can be recovered and the optimum π phase shift is reached at 14dB. Further reductions (that is data attenuation less than 14dB) push the switching past π and therefore the power of the pulses exiting the transmitted port is reduced.

We now turn our attention to what happens to the stored data after the 1st circulation. We have already discussed how the memory will regenerate the data to a stable level, provided the initial data power is suitable for storage. Although the power of the 1st

circulation varied greatly with the initial data input power, the regenerative nature of the device should reduce these variations through successive circulations. Consequently, later circulations should not see the same magnitude of variation.

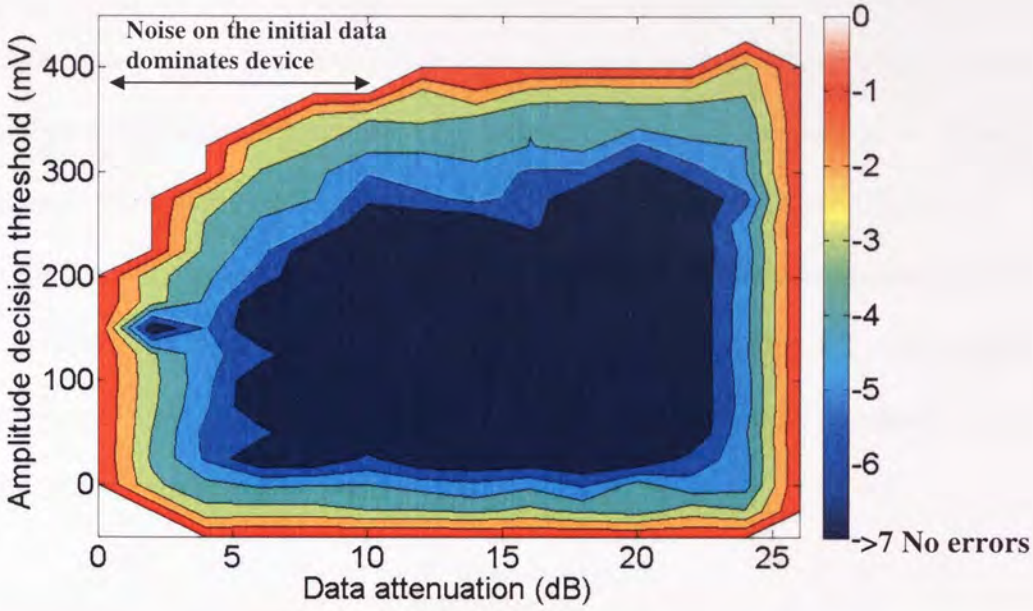


Figure 5-11 BER amplitude threshold after 250 circulations for changing data attenuation

Figure 5-11 shows the measured BER map for the 250th circulation. As can be seen from the map, for the lowest of the input powers (where the attenuation is greater than 23dB) the data has not been stored. If we look at the results for the first circulation Figure 5-10, 24dB of attenuation resulted in the minimum power from which the initial data can be recovered. After 250 circulations the maximum data attenuation level has been reduced to 23dB of attenuation, a 1dB difference. Initially once the attenuation level is lower than 23dB the size of the window where a BER of 10^{-7} can be achieved does not change. However, a point is reached at approximately 8dB of attenuation where the amplitude of the ones decreases. This is because the noise floor of the initial data is not zero, after the initial packet has been provided. The poor noise floor is a result of both a poor extinction on the modulator and extra ASE generated

by the EDFA, located in the initial data supply. The unwanted noise entering the loop increases in power as the attenuation is reduced; therefore, removing gain available in both the feedback arm and the SOA. Ultimately the stable level mentioned previously is reduced.

We have discussed how the device stores the data at a stable level (section 3.4 and 4.4) and providing the initial data power is suitable the data will continue to be stored at this level. We can see evidence of this by comparing Figure 5-10 and Figure 5-11. Although there is considerable variation in the amplitude of the stored data after the first circulation, by 250 circulations this variation is greatly reduced. We can see the evolution of this by plotting the BER map for the amplitude decision threshold level as a function of the circulation number (storage time).

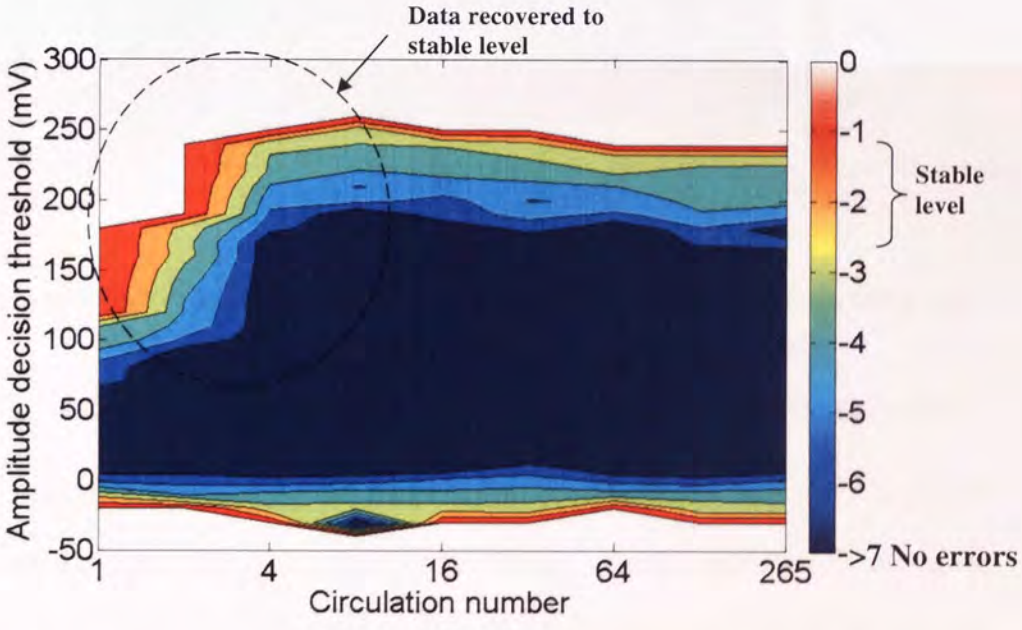


Figure 5-12 BER amplitude threshold sweep for varying circulations with a initial data input lower than stable level (data attenuation level of 23dB)

Figure 5-12 shows a BER map for a single initial data input power (data attenuation set to 23db) but this time the horizontal axis represents the number of circulations. This result demonstrates the process of how the device regenerates the stored data to a

stable level from a low power and Figure 5-13 shows the result for high power initial data. From Figure 5-12 we can see successive increases in power at small numbers of circulations and even evidence of an overshoot caused by the data finding its own level. Figure 5-13 shows the same measurement as the previous figure, however, this time the data is of a higher power than the stable level but we can still see the data recover to its stable level (data attenuation of 14dB.)

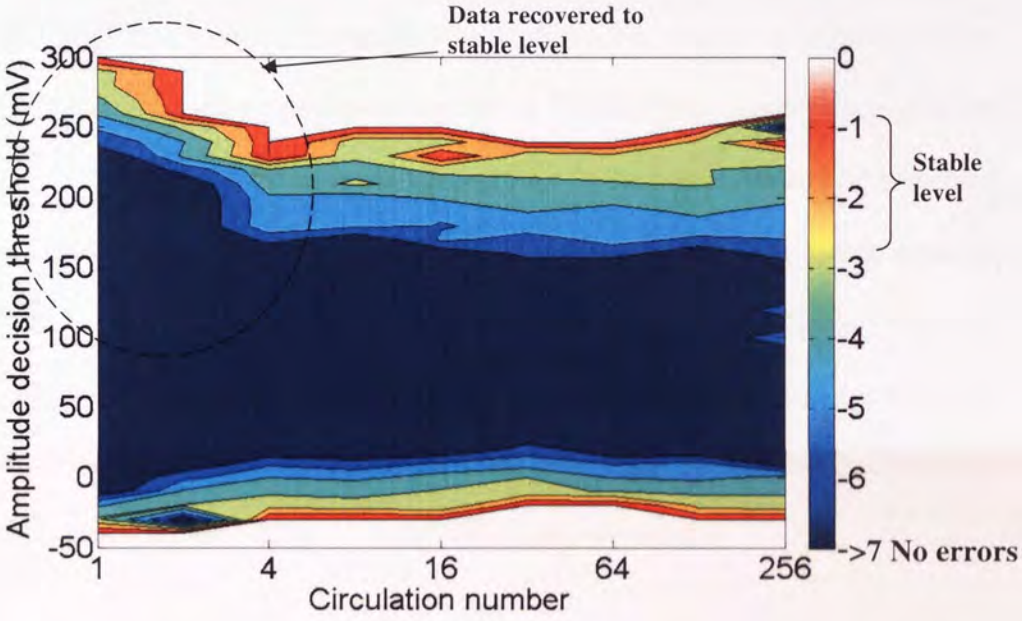


Figure 5-13 BER amplitude threshold sweep for varying circulations with a initial data input higher than the stable level (data attenuation =14dB)

5.7. Initial data timing characterisation using BER measurements

Along with pulse energy the other major property of the initial data is the timing of the pulses relative to the clock pulses. For optimum switching performance the pulses contained in the initial data packet must arrive immediately before one of the propagating clock pulses. Any variation from this point will result in poorer switching causing resultant output signal power from the 1st circulation to be reduced. As the timing of the control pulses moves further away from the optimum delay a point will

be reached where the switching will be so inefficient that the device will not be able to store the data.

In this section we look at how the timing of the initial data pulses affects the storage capability of the device. Figure 5-14 shows a 3D intensity BER map for the output of the 1st circulation with a range of 150ps delay on the initial data. The horizontal axis represents the relative timing for the control pulse and the vertical axis corresponds to the BERT amplitude decision threshold. Although the data is at an effectively reduced rate of 3.3Gb/s the clock pulse supply remains at 10GHz; consequently the results are repeated every 100ps. As we have seen in section 4.3, the two characteristic switching windows associated with the use of the symmetrical SOA operating position (described in section 2.6.) can be seen. It is also worth noting that the two windows are clearly of different sizes. In this instance we would expect that, because the clock pulses arrive at the SOA at equal time intervals, the switching window should be the same. This characteristic will be investigated later in this section.

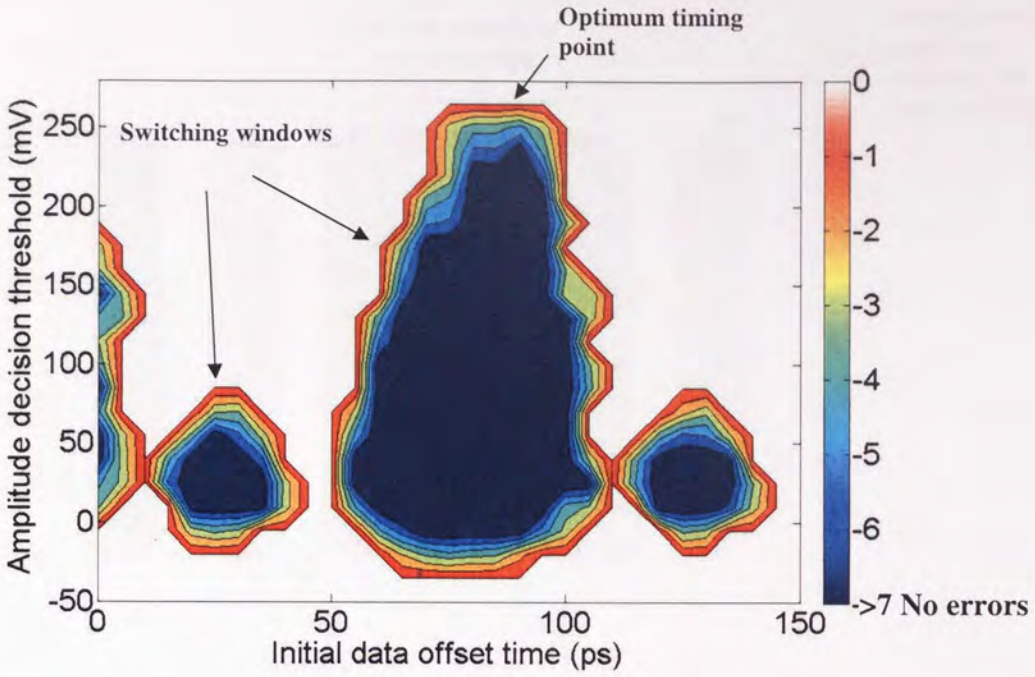


Figure 5-14 Variation in the initial data input timing against BER threshold after the first circulation of storage

For the 1st circulation the pulses contained in the initial data perform the task of the control pulse. Varying the initial data timing alters the arrival time of the control pulses at the SOA. For optimum switching the control pulse must arrive immediately before one of the clock pulses. In Figure 5-14 we can see that this occurs at a delay offset time of 90ps where the output power is at its maximum. Either side of this point the power switched out is reduced and ultimately data is lost.

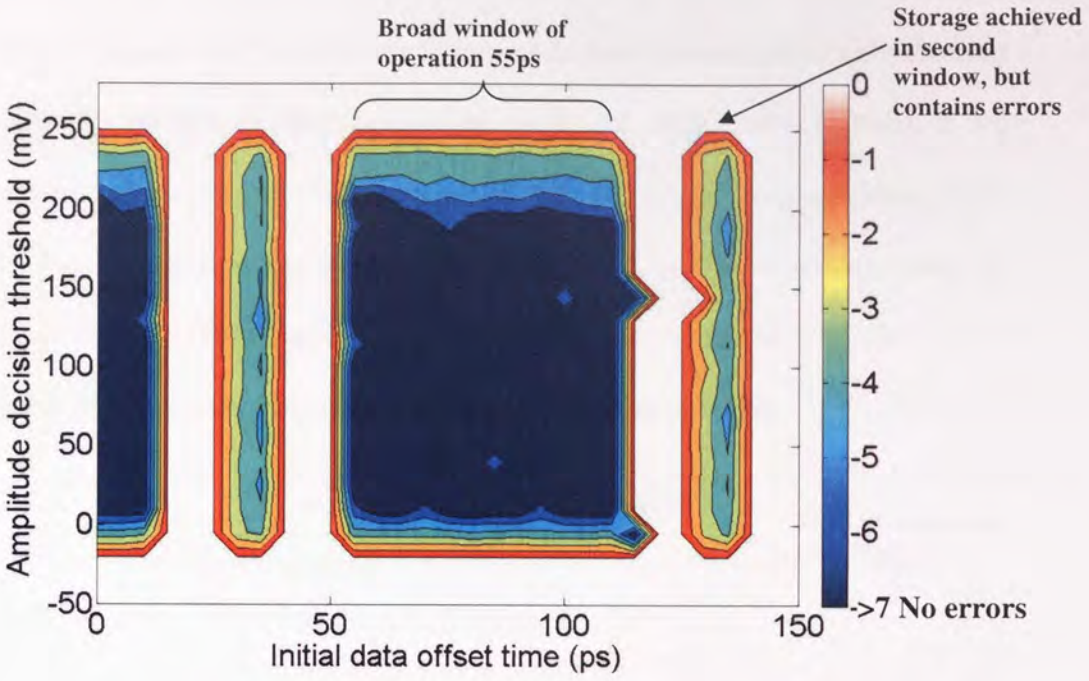


Figure 5-15 Variation in the initial data input timing against BER threshold after 250 circulations

The regenerative nature of the device will rectify the different levels seen after the first circulation through multiple circulations. This effect can be seen when the measurement was repeated after 250 circulations, Figure 5-15. Here we can see that the device has recovered the different amplitudes caused by the varying delay offsets to a standard level, thereby providing an operating range of 55ps. Outside this range the initial data switched out by the 1st circulation is not of sufficient power for the succeeding circulations to store the data successfully.

With the SOA in the symmetrical position it is expected that there should be two operating windows and one would expect these to be the same. However, as we have seen from section 4.3 (Figure 5-14 and Figure 5-15, where we measured the effects of changing the initial data timing) the windows are not symmetrical.

The main reason for the non-symmetry in the switching windows is a result of the finite length of the SOA. To understand this fully Figure 5-16 shows the results of the

transmitted output of the TOAD for varying initial data timings (effectively showing the output for the first circulation switched out by the initial data). Included in the diagram are representations of the position of the counter and co-propagating clock pulses. Also included is the SOA time of flight of 17ps (SOA width), which is calculated from a 1.6mm length of SOA and a refractive index of 3.2. The loop is configured so the counter propagating pulse arrives first at the SOA.

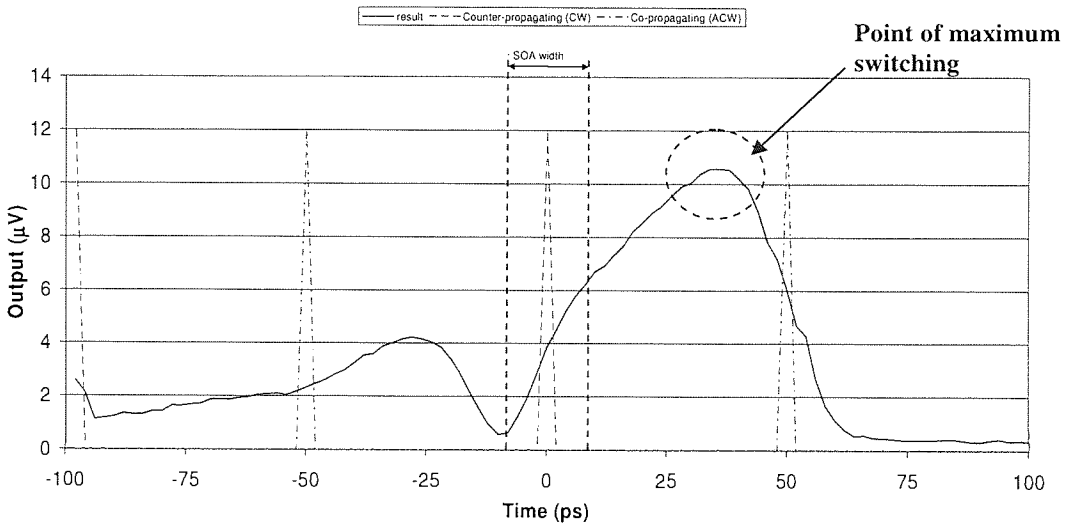


Figure 5-16 TOAD operating window for varying data input timing offset for 3.3GHz data pattern

Starting from –100ps the control pulse reaches the SOA 100ps before the two subject clock components. At this timing if we measure the transmitted output for the previous clock pulse then we would see it being affected and switched out. As we can see, because the SOA does not recover between each bit, even at 100ps before the counter propagating pulse the subject clock pulse is affected and so partial switching is achieved. When the delay between the control pulse and the counter propagating pulse is reduced, the impact upon the counter propagating pulses increases. The switching is therefore increased, which reaches a maximum at –28ps. It is worth noting that although it is mainly the counter propagating pulse that is affected, the

slow recovery of the SOA means that the co-propagating pulse is also affected. This effect on the co-propagating pulse opposes the phase shift generated on the counter propagating pulses. Hence, the switching in this window is never as high as its counter part, which is when the control pulse arrives after the counter propagating pulse. For timing offsets greater than –28ps the effect of the control pulse upon the co-propagating pulse increases and the differential phase shift reduces. This happens until a timing of –10ps where there is no differential phase shift and minimum switching is achieved. As the delay starts to increase further, the dominating effect swaps from the counter-propagating pulse to the co-propagating pulse. Further increases of delay result in an increase of switching efficiency until the maximum is reached at 34ps. At this point the counter-propagating pulse arrives at the SOA before the control pulse, so it is not affected. In addition maximum phase shift is applied to the co-propagating pulse; this is because the control pulse arrives immediately before the co-propagating pulse as it transits through the SOA. Once the maximum point is achieved at 34ps, further increases in the delay sees the control pulse start to overlap with the co-propagating pulses, this continues until the co-propagating pulse arrives at the SOA before the control pulse, preventing switching.

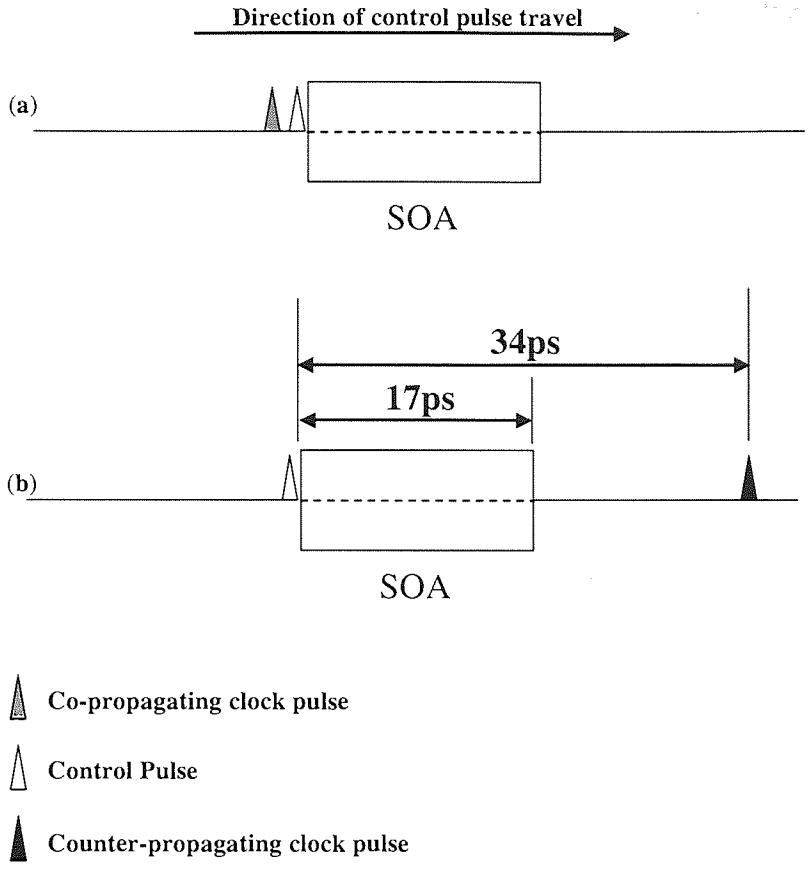


Figure 5-17 Transit of the control pulses through the SOA a) Co-propagating and b) Counter-propagating clock pulses

The effect caused by having a finite SOA shows itself when the control pulse switches out the counter-propagating pulse. The co-propagating clock pulse travels in the same direction and speed as the control pulse, so their relative positions stay the same. Therefore, when the control pulse transits through the SOA the co-propagating pulse immediately follows creating maximum impact see Figure 5-17(a). With the counter-propagating pulse this is not the case. This is because for the pulse to see the SOA in its maximum saturation state, the control pulse is required to fully pass through the SOA before the counter propagating pulse can enter, see Figure 5-17(b). This means that with an SOA which is 17ps in length, the time between the control pulse entering the SOA and the counter-propagating pulse exiting is 34ps, allowing the SOA time to

recover considerably before the entire counter propagating pulse exits the SOA. This reduces the total available phase shift, reducing the switching efficiency.

5.8. Relationship of the initial data timing and attenuation characterisation using initial data with good and poor extinctions

Previously we looked at how the device reacts exclusively to a change in the initial data timing and the initial data power. In this next section we will look at how the device reacts to a combined change both to the initial data power and initial data timing. Preliminary investigations will be made using initial data that has a high extinction ratio. This will then be repeated using an initial data signal with a reduced extinction ratio.

We have already seen how the power of the initial data affects the efficiency of the switching i.e. the higher the data power the higher the output power. When we vary the timing there is a position where the data could not be stored because the original output on the transmission was too low. It should be possible to compensate for this by increasing the power of the initial data thus allowing improved switching. However, a decrease in the initial data input power could result in a reduction of the window in which the timing can be changed.

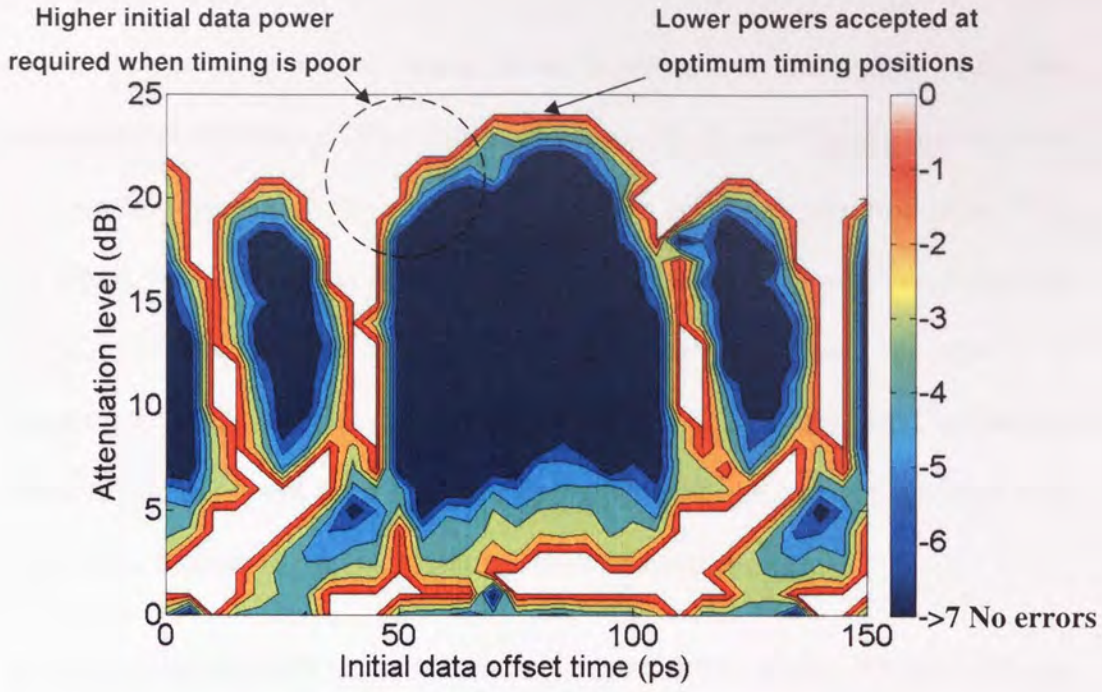


Figure 5-18 BER chart for initial timing against initial amplitude for an initial good extinction ratio on the data packet after 250 circulations

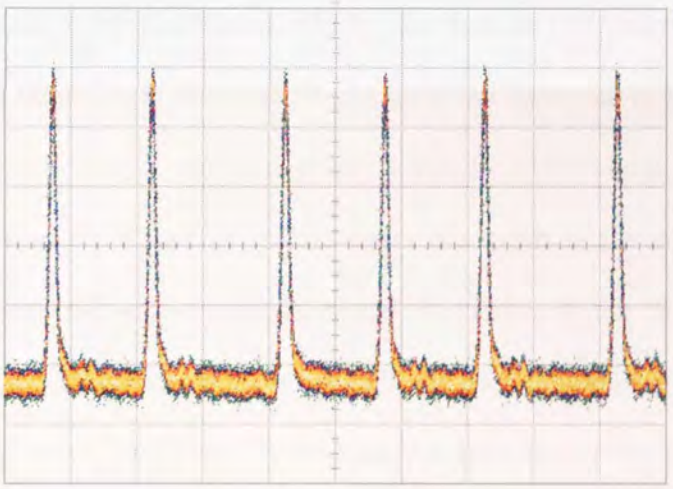


Figure 5-19 Initial data input with good extinction

Figure 5-18 shows a BER map after 250 circulations for varying initial data powers (regulated by an attenuator) and timings using the high quality signal shown in Figure 5-19. The two windows associated with the timing offset sweeps are clearly visible and as before the larger of the windows covers ~55ps. If we look at the range of input data powers where the device is error free, we can see the compensation of poor

switching, caused by a poor timing offset. If we look at the higher initial data attenuation levels between 18 and 24dB, we see that the level of input power required for error free operation is lower when the timing is in its optimum position of 85ps, see Figure 5-14. Either side of 85ps the control pulse timing moves away from the optimum position and therefore greater initial data input power is required to compensate. At higher input powers, between 9dB and 5dB of attenuation, we see that where the timing is not at its optimum operating point, the memory can cope with more power than when the timing is in the most efficient position.

The previous results were recorded using a high quality data source. We will now turn our attention to what happens when we repeat the experiment with a signal of poor quality. In this case, the extinction ratio (P_1/P_0) was considerably reduced. Considering all the other parameters, which contribute to the quality of a signal, the extinction ratio should have the most impact upon the operation of the memory. The memory stores data using a virtual decision threshold level; where pulses below the threshold are stored as "0" and any pulses above the threshold are stored as "1". With an infinitely large extinction ratio, provided the value of the "1"s is above the threshold level, the amplitude of the initial data can be continuously increased without errors occurring in the stored data. When there is a finite level of zero (as found in any practical system) continuously increasing the power of the initial data will result in the "0"s eventually reaching the decision threshold level of the memory. Once a "0" is above this decision level then it will be stored as "1" generating an error (see section 3.4). Therefore, the extinction ratio determines the maximum initial data power that the data can be stored error free. Similarly, the minimum initial data power required is determined by the "1" level. As error free data can only be stored when the "1" level is above the decision threshold.

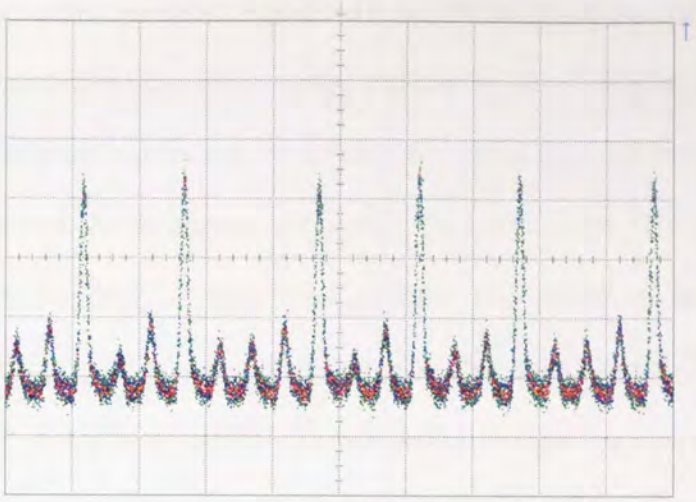


Figure 5-20 Initial data input with poor extinction of ~1:3

Figure 5-20 shows the trace of the initial data input, taken on the sampling oscilloscope. If we compare this trace with the trace of the input with good extinction, Figure 5-19, we can see that although the level of the "1"s remains the same, the level of the "0"s has increased to a ratio of approximately 1:3.

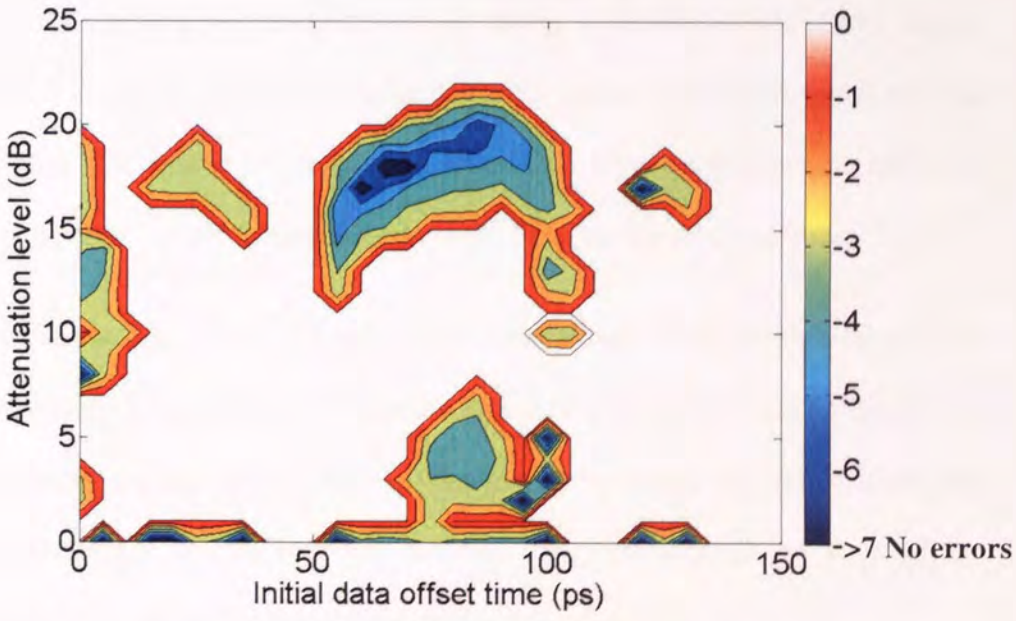


Figure 5-21 BER chart for initial timing against initial amplitude for an poor extinction ratio on the initial data packet after 250 circulations

As with the good extinction ratio, Figure 5-19, a BER sweep of the initial data power and the initial data offset time was recorded and can be seen in Figure 5-21. With the extinction ratio so poor we can see the window for which the amplitude can vary has been greatly reduced. As mentioned previously the levels of the "1"s determines the minimum power required for successful storage. The power of the "1"s hasn't changed from the results taken with the high quality input signal. Therefore, the minimum initial data power required for successful storage has changed very little between Figure 5-18 and Figure 5-21. Conversely, because the amplitude of the "0" has increased in relation to the "1" the maximum allowable power for error free storage has greatly reduced. Ultimately, a poor extinction ratio between "1"s and the "0"s results in a reduction in the window within which the initial data power can be varied whilst error free storage is achieved.

5.9. Feedback timing characterisation using BER measurements

In the previous section we looked at how the timing of the initial data pulses affects the stored data. It was shown that the timing of the initial data pulses could vary as much as 65ps before there are errors in the stored data. Here we will turn our attention to the timing of the control pulses arriving at the SOA via the feedback loop.

The length of the feedback loop determines the arrival time of the control pulses at the SOA whilst also determining the maximum length of a packet that can be stored. As in the previous results, section 4.5, the window is repeated every 100ps when the clock is operating at 10GHz. However, for every 100ps reduction in the length of the feedback loop the storage capacity of the device is reduced by 1 bit.

When investigating the initial data timing characteristics, the variation in switching efficiency was compensated for by the regenerative properties of successive

circulations. When the timing of the control pulse exiting the feedback results in poor switching, all the circulations will have a poor switching efficiency. Thus, unlike for poor initial data timing, the device cannot compensate so the data is lost. For the device to be self-sustaining, as required for successful long-term storage, the timing of the feedback is far more critical than the timing of the initial data. We expect evidence of this by having a smaller window of operation as we have already found in section 4.5.

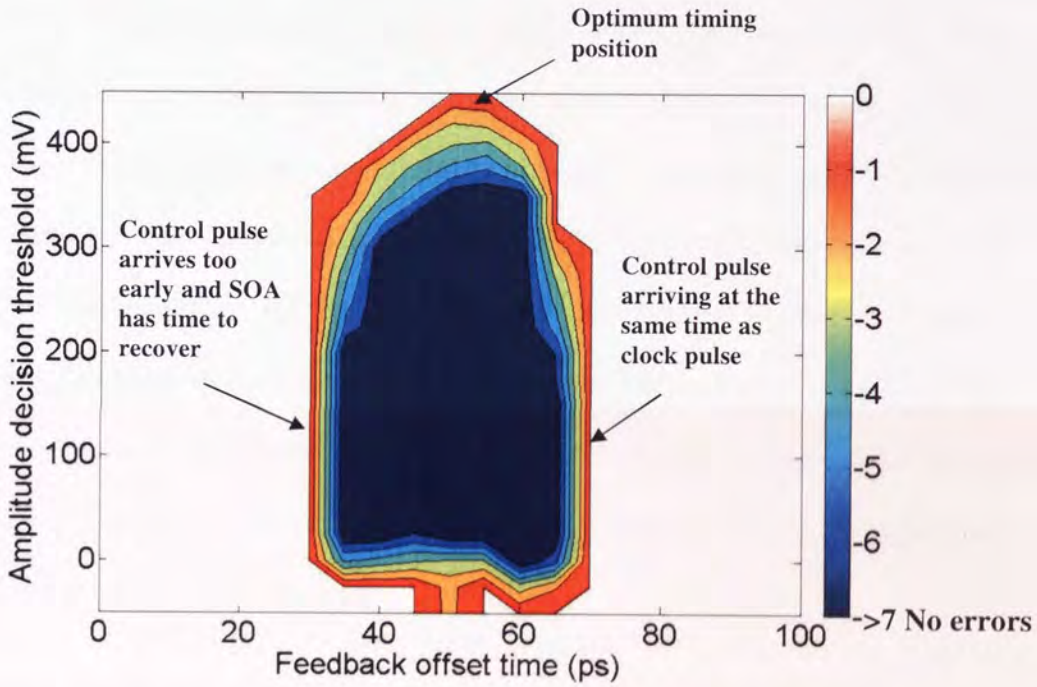


Figure 5-22 Variation in the initial feedback timing after 250 circulations

Figure 5-22 shows the BER map results for the feedback timing over 100ps against the BER threshold after 250 circulations. If we compare this result with the one taken for the initial data timing only, Figure 5-15, we can see that the feedback timing has a greater sensitivity, indicated by a smaller operating window. Where the operating range was a 65ps variation in the initial data timing, for the feedback timing this has now been reduced to 30ps. Outside of this operating range the switching efficiency is too low for the device to successfully store the data.

If we look at the amplitude decision threshold in Figure 5-22 we can see that the maximum amplitude is at a feedback timing of approximately 50ps. At this point the switching is at optimum efficiency and variations either side of this result in the reduction of the switching efficiency. What is noticeable from the results shown above is that the decrease in the efficiency on either side of the optimum operating point is not symmetrical. The steeper right hand side of the optimum point is where the control pulses are arriving at the SOA at the same time as the switched out clock component. Where the data is lost indicates that the control pulse actually arrives after the clock pulse preventing switching altogether. The left hand side of the optimum position is attributed to the control pulses arriving at the SOA before the clock component. Here, the difference in the arrival time of the control pulse and the clock component increases as the feedback loop is decreased in length. This allows increasing amounts of time for the SOA to recover before the propagating clock component arrives. Therefore, the gradient of the slope on the left hand side is consequently defined by the recovery of the SOA and the gradient on the right hand side is determined by the pulse width.

5.10. Feedback attenuation characterisation using BER measurements

Along with the feedback timing, the feedback attenuation or gain is arguably the most important and critical component of the feedback loop. The power of the control pulses which have transited the feedback loop is ultimately defined by the loss in the feedback loop. As demonstrated in section 4.6, when the loss in the feedback arm is too high then there is not enough power to keep the data stored. However, too much gain in the feedback arm will result in the data being lost due to the noise floor and the finite value of a "0" power increasing with every circulation.

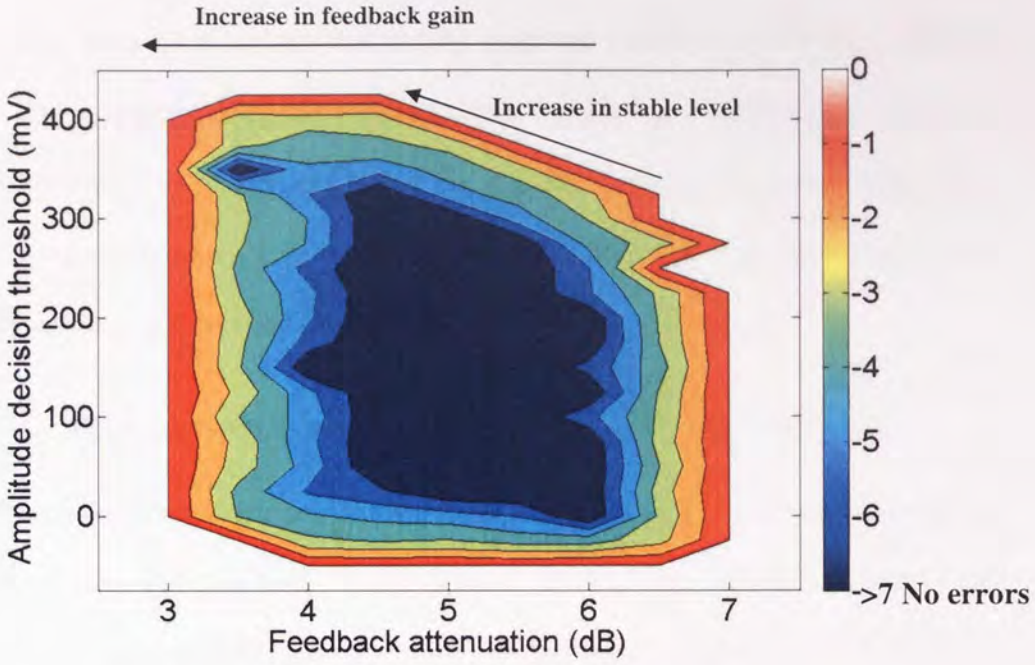


Figure 5-23 Variation in the feedback attenuation after 250 circulations

Figure 5-23 shows the BER map for a variation in feedback attenuation against the amplitude decision threshold level. If we compare this result with the initial data attenuation result, Figure 5-11, the ability of the memory to cope with a change in the feedback loss is less than for a change in the initial data power. In a similar way to the feedback timing experiments, this again is due to the regenerative cascade nature of the device.

As the loss in the feedback is reduced we can see an increase in the power of the clock pulses switched. However, this is limited by the increase in the noise level and the non-zero power in a bit value "0". When the feedback loss becomes too low for the device to suppress the noise, errors will occur (in this case ~4dB). This can be seen from the results in Figure 5-23, which confirms the numerical simulations in section 3.4 and experiments using basic patterns in section 4.4.

If the loss in the feedback arm is too high for storage then the power of the control pulses entering the SOA is reduced. Hence, the next group of clock pulses, in the

subsequent circulation, is not completely switched and this results in a reduced control pulse power exiting the feedback loop. Further circulations result in greater power reductions until the data is lost (in this case ~7dB). The other component, defining the power of the control pulses exiting the feedback loop, is the SOA itself and we will look at this in the next section.

5.11. SOA current characterisation using BER measurements

In the previous chapter, section 4.6, we looked at how the SOA current affected the storage of data using a basic block pattern. In this next section we repeat the experiment using the BER tester to provide a more detailed analysis.

Although the SOA is located in the loop mirror to provide the non-linear element required for switching, it is worth remembering that it is also an amplifier. If we look at the simplified path of the clock pulse we can see that the gain provided by the SOA defines the power of the switched out clock pulse as it exits the transmitted port. Therefore, the effect of changing the gain in the SOA, defined by the forward biasing current, is similar to the effect of changing the feedback gain provided by the EDFA. Consequently, when the SOA current is low then the gain seen by the clock pulses is low. As we have seen with a low feedback gain (previous section) when the clock pulses entering the feedback arm are too low the power of the control pulses exiting the feedback loop will not have enough power to provide continuous data storage. Similarly, when the SOA current is too high and providing too much gain the noise on the zero will be too high, this will result in the noise having enough power to switch out the next group of clock pulses producing errors.

We have already discussed the effect the SOA recovery rate has upon the device. By changing the SOA current we are changing the recovery rate and hence the dynamics

of the device. If the recovery rate is too slow then the data will not be stored. This is because the SOA cannot recover between individual bits and hence will cause interbit modulation, ultimately producing errors (as mentioned earlier in this chapter.)

It would therefore be reasonable to assume that the higher the SOA forward biasing current the better. However, because the recombination of the carriers is higher, the ASE noise produced from the SOA is increased raising the noise floor. This added noise will be fed back into the loop mirror affect the switching, hence causing errors.

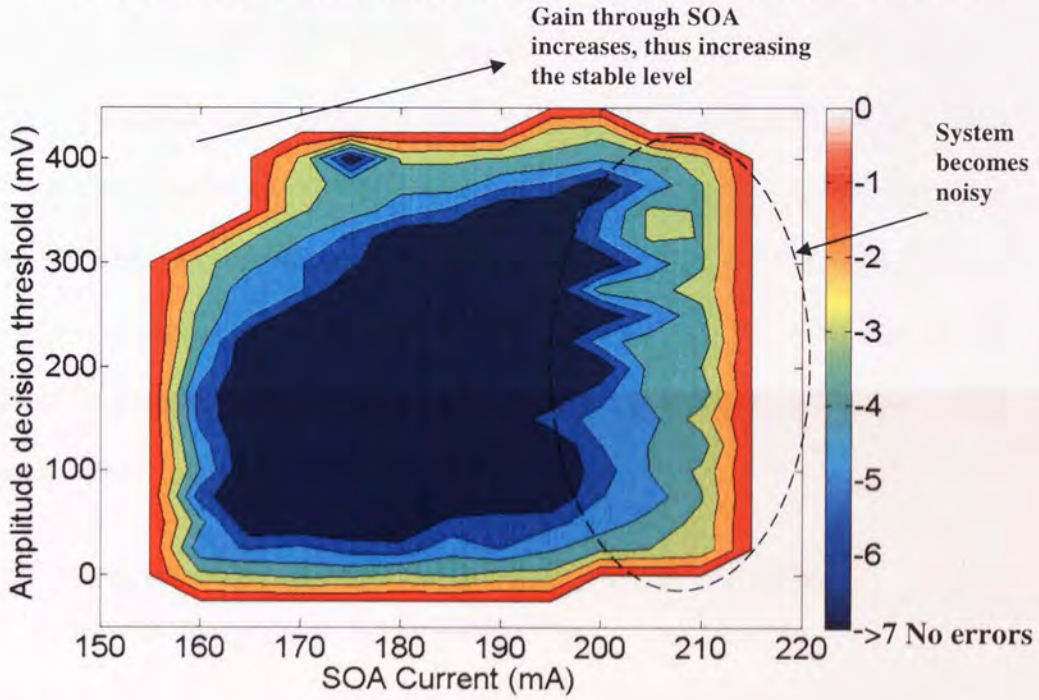


Figure 5-24 BER amplitude threshold sweep for varying SOA currents after 250 circulations

The results in Figure 5-24 show the BER map for the SOA current against the BER amplitude decision threshold after 250 circulations using a high quality input. As we can see, "error free" operation can be achieved for a SOA current ranging from a minimum value of 165mA to a maximum current of 195mA. Outside this window the device is unable to store the data. It is worth noting that around 165mA, the minimum operating point can be clearly identified. Whereas, on the higher operating point the

difference between working and not working is unclean and noisy. This is because at low currents there is not enough energy in the switched out pulses for the device to store the data. Whereas, in the higher operating point the SOA produces more noise, which when combined with the extra available gain results in a device dominated by noise.

In a previous section we have seen that the gain in the feedback arm changed the normalised stable position, therefore because the increase in the SOA current produces gain we would expect the normalised level to increase as the current increases. This can be seen in Figure 5-24 where the amplitude level of the "1"s after 250 circulations increased with SOA current. It is also worth noting at this point that the zero level has also increased proportionally with the SOA current. Although the zero level is increasing, it is not increasing at the same rate as the "1" amplitude level. This leads to the size of the window for the BER amplitude threshold level also increasing with the current.

5.12. Relationship between the SOA current and feedback attenuation using BER measurements

It has been demonstrated how the overall gain in the feedback affects the storage of the data. In this section the relationship between the SOA current and the feedback attenuation is investigated. If we reduce the SOA current then the power of the control pulse exiting the feedback arm is reduced. Therefore by reducing the loss in the feedback we can compensate for gain lost in the SOA. Alternatively, the feedback loss can be increased to compensate for a high signal gain through the SOA.

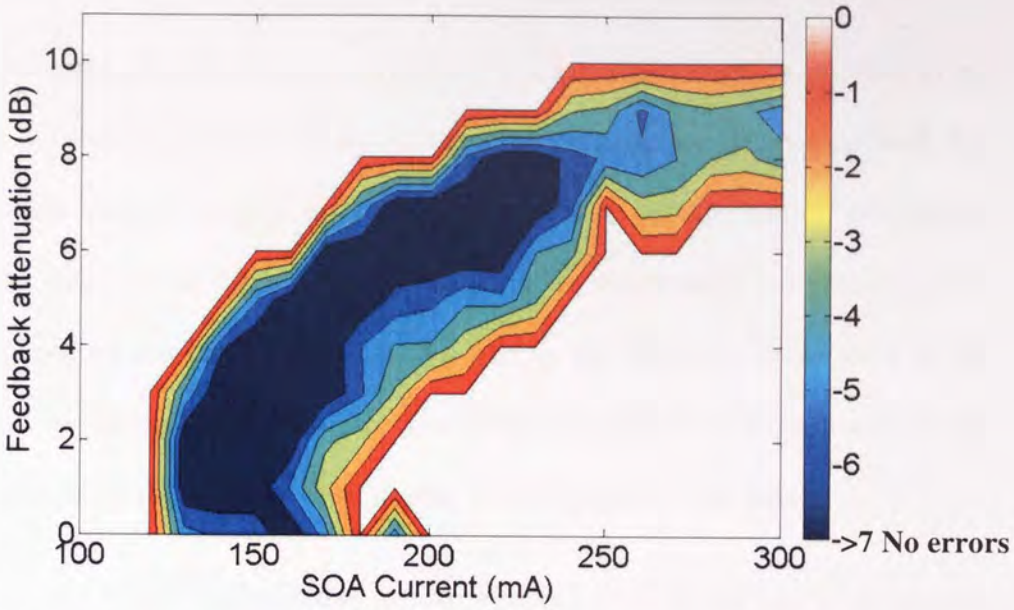


Figure 5-25 BER map for a change in SOA current and feedback attenuation after 250 circulations

Figure 5-25 is a BER map recorded for the feedback attenuation against the SOA current after 250 circulations. As we can see from the results, at low current the feedback loss needs to be reduced for the data to be stored. When the SOA current is high the feedback loss needs to be increased to compensate for the extra gain provided by the SOA. By changing the SOA current the variation in the range of the feedback loss is increased from 2dB (found in section 5.10) to 7dB. The current variation has also changed from 165–195mA to 130–230mA, by changing the feedback attenuation level.

The effect of the additional noise generated by a higher SOA current is also demonstrated in Figure 5-25. At SOA current levels above 240mA the SOA generates so much noise that no increase in the feedback loss can compensate and hence the stored data cannot be recovered.

5.13. Clock power characterisation using BER measurements

The clock consisting of a constant stream of "1"s provides pulses for the data to be mapped to. Without the clock the data cannot be stored. As previously described, the power of the clock is a significant parameter in defining the operation of the device. When the power of the clock is too low the power of the switched out pulses exiting the loop will be low. To compensate, the gain in the feedback would have to be increased. However, the penalty for increasing the gain in the feedback is the increased noise in the overall system leading to poor storage of the data.

When using a TOAD we normally assume that the clock power has no saturating effects upon the SOA. As described in section 2.7, this is not the case, since the clock pulses do remove gain from the SOA. If the clock powers are too high then the control powers used for switching may not be sufficient to generate the levels of transmitted output required for storage.

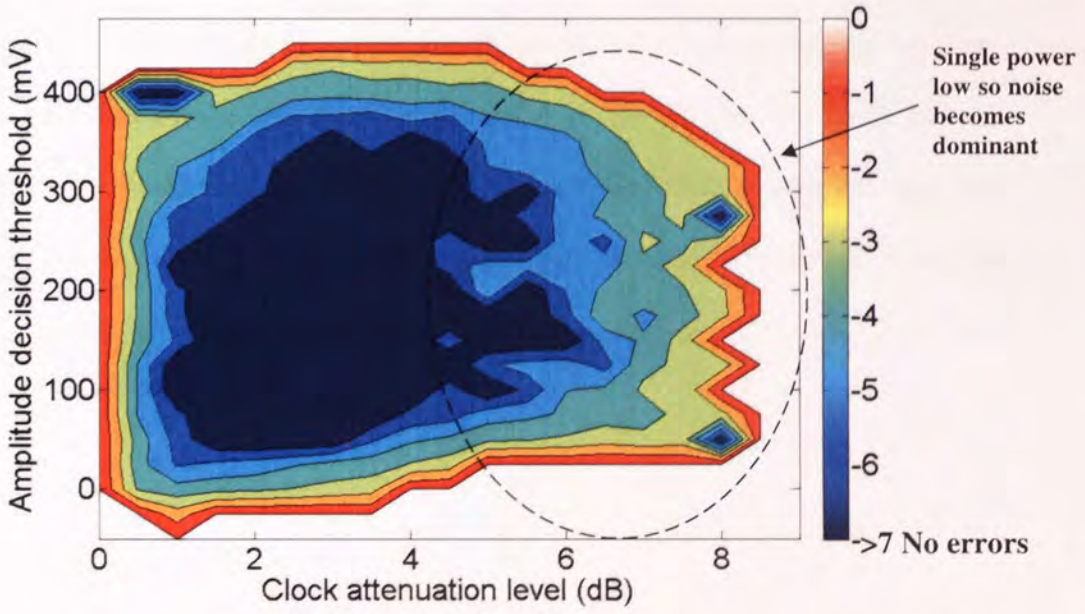


Figure 5-26 Characterisation sweep for varying clock attenuation levels after 250 circulations

The BER map in Figure 5-26 shows the experimental results for the change in clock power as a function of the Amplitude decision threshold level. As we can see the extra ASE (generated by an SOA with reduced incident light) and the reduced amplitude of the propagating signal causes the storage of the data to become unstable at an attenuation level of 5dB. If we compare the regions of low clock powers (attenuation>4dB) and high clock powers (attenuation<4dB) then we can see that the data stored has greater stability and less noise around the high clock power limit of 1dB of attenuation.

The lower the incident light upon the SAO the greater the level of ASE noise produced and we can see the result of this effect in Figure 5-26. This noise is a component of the "0" level and so is at its highest when the clock is at its lowest. As the clock power increases the gain available at the SOA reduces resulting in the reduction of generated ASE indicated by the reduction in the noise floor (as can be seen in Figure 5-26.)

The effect of high clock powers changing the switching efficiency can also be seen; this is indicated by the reduction in the power of the "1"s as the clock powers increased. As we have described previously when the clock powers are high the control power required to provide full π switching is increased. Therefore, it may be possible to reduce the loss in the feedback loop to compensate.

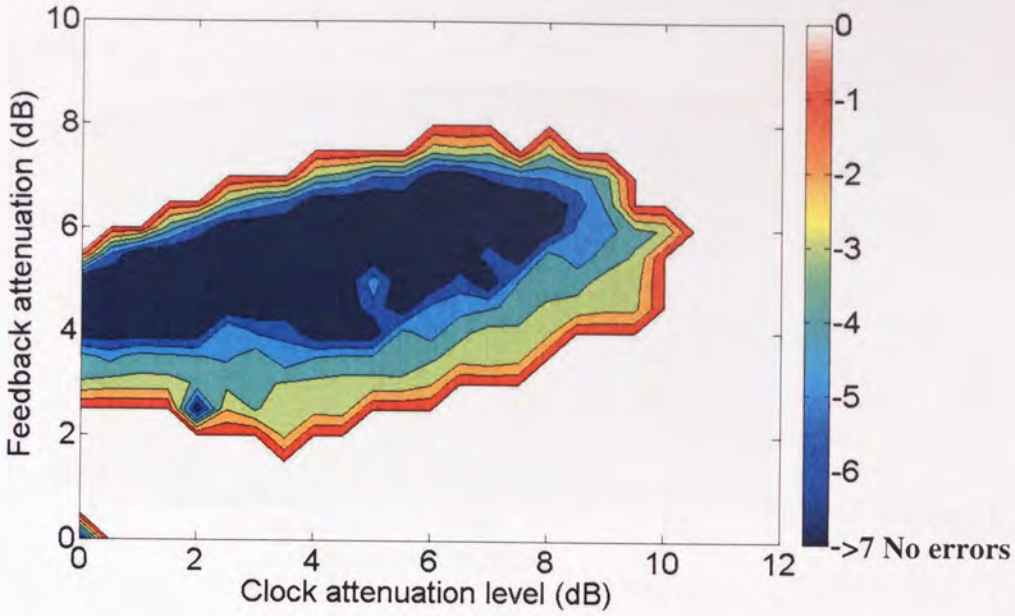


Figure 5-27 Characterisation sweep for clock attenuation against feedback attenuation levels

Figure 5-27 shows the BER map for feedback attenuation against clock power after 250 circulations. As we can see from the chart, by changing the feedback attenuation the dynamic range of the clock power, before the data is lost, is greatly increased.

5.14. 5Gb/s operation using BER measurements

It was discussed at the beginning of this chapter that the recovery of the SOA was too slow to completely switch out the clock pulses without applying modulation. Appendix D demonstrates using a sampling oscilloscope the process of deterioration of the data for a 10GHz signal. The speed of the deterioration of a stored 5GHz data packet is slower than for the 10GHz data and therefore will require more circulations for the data to be unrecoverable.

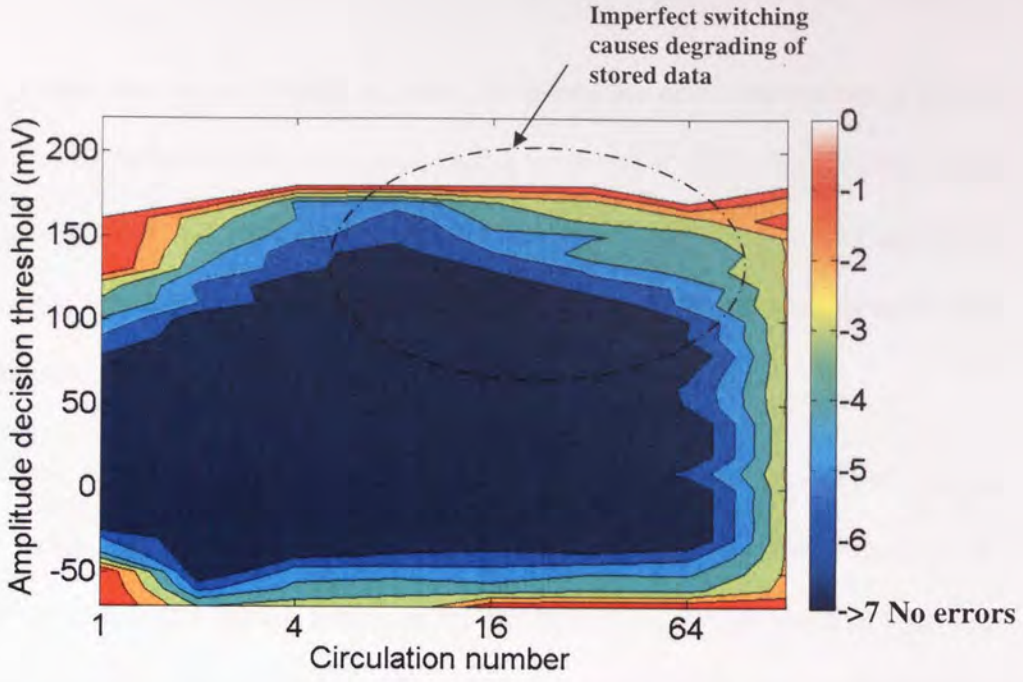


Figure 5-28 Deterioration of data quality for 5GHz operation

Figure 5-28 shows the deterioration of a 5GHz data packet over multiple circulations. The horizontal axis represents the number of circulations and the vertical axis represents the amplitude decision threshold. As can be seen the initial data power is lower than the stable level, as the memory initially starts to recover the data to the stable level. As with the 10GHz signal one of the data pulses start to reduce through the modulation effects of a slow SOA. We can see evidence of this from the results as the level of the ones starts to reduce through successive circulations. These results prove the incapability of the device, with its current setup, of storing 5GHz data.

5.15. Discussion

In this chapter we have investigated some of the main characteristics of the memory device using the TOAD as the regenerative component. We have measured the BER of the memory to show, because of the recovery rate of the SOA, the maximum operational speed of the data is 3.3GHz. Any data rate higher than this and continuous storage is not feasible.

With the data rate set to 3.3GHz we have confirmed the error free operation of the memory using both bit error rate curves and Q values up to 1000 circulations. It has been demonstrated that once the data has been stored no additional loss of quality is seen by the stored data through multiple circulations. This confirms the potential for extended storage times.

Some of the regenerative properties of the device have been proven by initially using a poor quality signal which, through successive circulations, has been improved. It has been demonstrated that the timing of the initial data can vary as much as 65ps and still the data will be stored. We have shown how the signal power can compensate for poor timing and visa versa. In addition, it has been demonstrated that the timing of the feedback pulses is more critical than the timing of the initial data pulses. Again poor timing can be compensated for by the gain in the feedback arm. Through experimental trials it has been shown that the main effect of changing the current in the SOA is that it alters the feedback gain required for switching. Thus, for successful storage a balance is required between the gain in the feedback loop and the gain generated by the SOA current.

Although we have demonstrated the operation of a non-inverting memory using a TOAD, the commercial viability of this type of product is weak. As well as suffering from a slow SOA, which limits the bandwidth, TOADs are generally used in research labs only because they can be simply made from discrete devices. However for a stronger commercially viable solution the integrated MZI could provide a better alternative. The proof of concept using the MZI will be made in the next chapter.

6. Hybrid integrated Mach-Zehnder interferometer (MZI)

6.1. Introduction

Previously we have concentrated upon a non-inverting optical memory buffer, which utilises a TOAD as its regenerator. The TOAD is a device that is suited for the laboratory as it can be simply made using discrete devices. However, the TOAD does not transfer easily from the laboratory to a commercially viable product. One method to improve the commercial viability of the non-inverting memory would be to replace the TOAD with a MZI.

The MZI is similar to the TOAD in that it can be used as a 3R regenerator as discussed in Chapter 1. When built using discrete devices, the susceptibility of the Mach-Zehnder to external environmental changes makes this type of device unsuitable for laboratory applications. However, with the advances of hybrid integrated technology it is now possible to obtain a commercial hybrid-integrated MZI 3R regenerator, which has the whole device packaged onto one chip [92]. By reducing the physical size of the device the environmental effects are minimised.

In this chapter we will look at the basic operation of the hybrid integrated MZI and experimentally demonstrate proof of concept for a MZI based non-inverting optical memory device.

6.2. *Introduction to the hybrid integrated Mach-Zehnder interferometer*

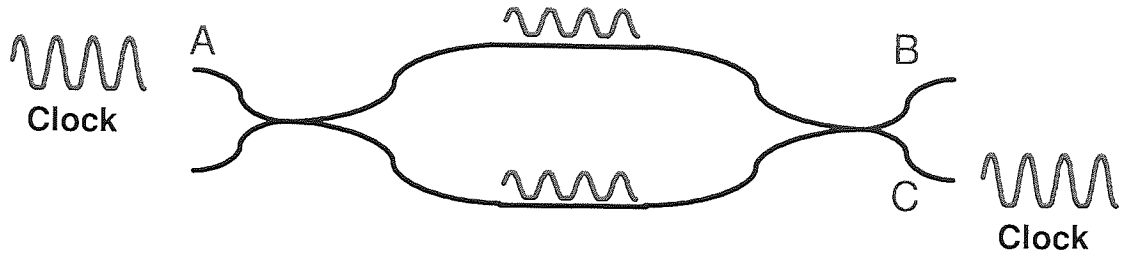


Figure 6-1 Light entering A will exit through port C when there is no differential phase shift.

We have already discussed the basic operating principles of the MZI in Chapter 1. Light entering port A, Figure 6-1, will split into two separate components as it passes through the first 50:50 coupler. After propagating along the upper and lower arms of the interferometer they will enter a second 50:50 coupler. Here they will recombine and because of constructive and destructive interference exit through port C only. As described in chapter 1, the differential phase shift between the two component signals determines what proportion of the incident light exits through each port. Zero differential phase shift will see all light exiting through port C, ("constructive port") and a π phase shift will result in the light exiting through port B ("destructive port").

As with the Sagnac loop mirror, the phase shift can be applied to one of the signals using a non-linear element. In the case of the hybrid integrated MZI an SOA is used as the non linear element. The SOA was chosen because it has many advantages over other potential non-linear elements. These include, ease of integration using hybrid technology, small physical footprint and low switching energies.

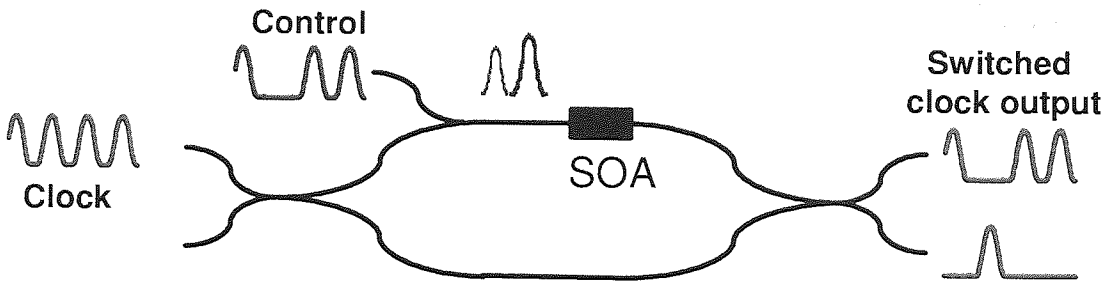


Figure 6-2 The addition of the SOA as the non-linear element enables switching using a control signal.

Figure 6-2 shows the interferometer using a single SOA located in one arm. In the same way as the TOAD, a control pulse is used to saturate the SOA switching a clock pulse from the constructive port to the destructive port. When the clock input consists of a train of ones, as shown in Figure 6-2, the data contained in the control input will be copied onto the clock pulses and thus regeneration will take place.

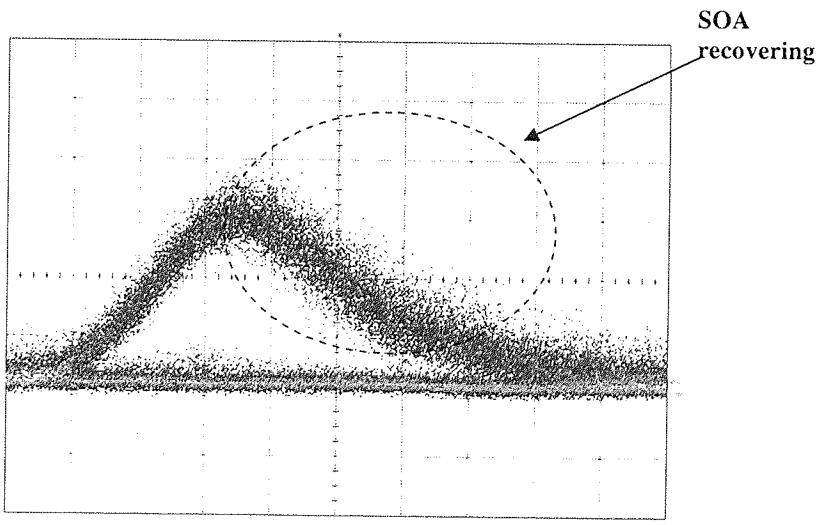


Figure 6-3 Mach-Zehnder interferometer output when CW clock is switched out using RZ data pulses

Previously in this chapter we have only talked about using an RZ pulse train as the clock input. However, these devices are also used with a clock consisting of a single wavelength CW source [93]. Figure 6-3 shows a typical output of a hybrid integrated MZI when a CW clock is used. Here we can see a typical eye produced from an RZ

Pseudo-Random Binary Sequence (PRBS) 2^7-1 input data signal, when only one SOA is used to generate the differential phase shift. Although we can clearly see the clock is being switched appropriately, it is worth noting the trailing edge. The initial edge is the result of the control pulse entering the SOA depleting the carrier density and thus generating a differential phase shift. The trailing edge is the result of the SOA recovering once the control pulse has fully transited the SOA. Consequently, although the initial gradient is quite steep and clearly defined the trailing edge can be quite shallow, resulting in a non-symmetrical switched output. This can be solved with the introduction of a second SOA arranged in a push-pull configuration.

6.3. *Push-pull configuration*

The push-pull configuration solves not only the issue of the trailing edge, as mentioned previously, but has the potential to increase the operating speed.

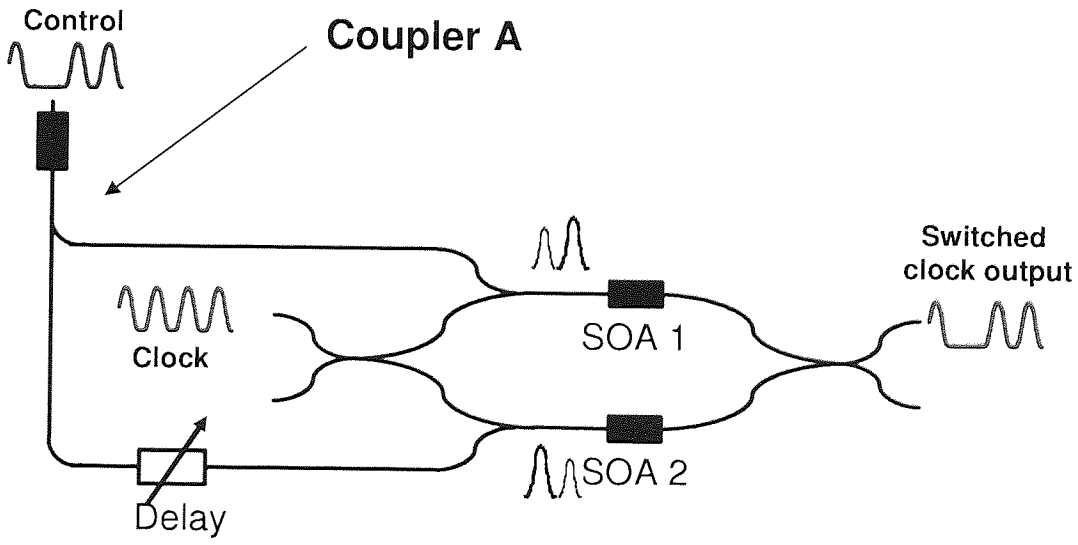


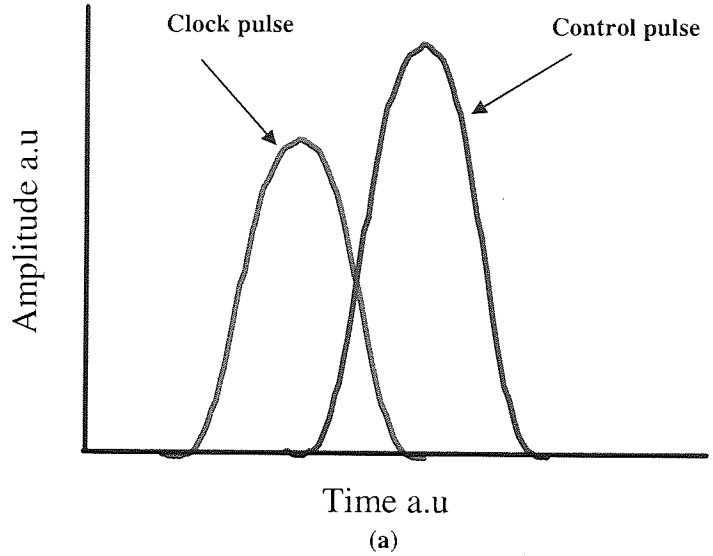
Figure 6-4 Mach-Zehnder interferometer with the combination of two SOA to form a push-pull configuration

Figure 6-4 shows the configuration for a push-pull device. Unlike the single SOA driven configuration, Figure 6-2, the push-pull driven MZI consists of two identical

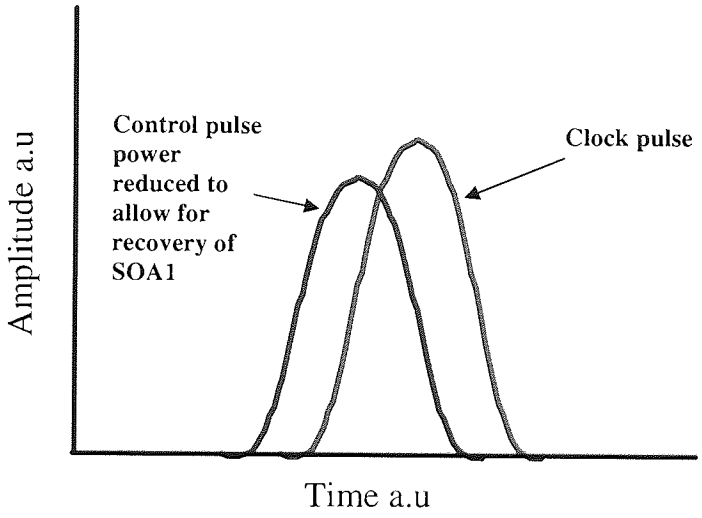
SOAs one located on each arm. Each SOA is supplied with an identical copy of the control data with the vital difference that one of the data signals is both delayed in time and is lower in energy.

The interferometer is "balanced" when the two SOAs both provide the same phase shift, that is the differential phase shift is zero (when the arms of the MZI are set to equal length.) When the two SOAs are providing an unequal phase shift (caused by different bias currents or saturation through a control pulse) the interferometer is referred to as "unbalanced".

When no control pulses are present, both of the SOAs are of equal gain and are therefore balanced thus, the clock will exit through the constructive port only. Switching is achieved through a control pulse. The control pulse will split into two separate pulses through a 50:50 coupler (coupler A) with one output pulse being delayed in relation to the other. The non-delayed control pulse will arrive at SOA1, which will cause the pair of SOAs to become unbalanced. This will cause a temporal differential phase shift causing switching. The delayed control pulse will enter SOA2 after a time set by the delay. The second control pulse will deplete SOA2, which will balance the two SOAs, thus preventing further switching. The time delay between the first pulse entering SOA1 and the second pulse entering SOA2 will enable SOA1 to recover a nominal amount. Therefore, to ensure that the second control pulse does not over deplete SOA2 (further unbalancing the SOAs), the second control pulse must be at a lower pulse energy than the first control pulse.



(a)



(b)

Figure 6-5 Picture showing the transit of the control and the clock pulse through a) SOA1 and b) SOA2

The push-pull configuration can reduce the slow trailing edge caused by the SOA recovery as mentioned previously, see Figure 6-3. By rebalancing the loop after a period of time (determined by the second control pulse delay) we can influence the pulse width of the output pulse and provide greater definition to the trailing edge. Figure 6-6 shows the output of a push-pull device. Here it can be seen that the trailing edge has a greater definition when compared to the results in Figure 6-3.

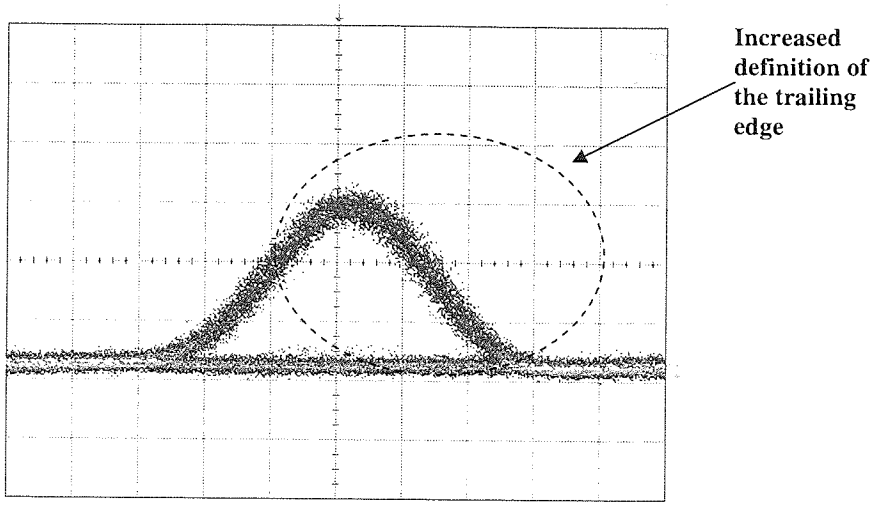


Figure 6-6 Output of a Mach-Zehnder interferometer using push-pull and CW clock input.

The second benefit of using a push-pull configuration is it allows for the use of higher bit rates, conventionally defined by the SOA recovery rate. With a non push-pull single SOA configuration perfect operation is highly reliant on the assurance that the SOA returns to the same carrier density levels between each bit. At high bit rates, which have a bit period shorter than the SOAs recovery rate, the SOA does not have enough time to recover between each bit. Therefore, the SOA is not in the same condition at the start of each bit period. This effect is most prominent when there is a long sequence of "1"s.

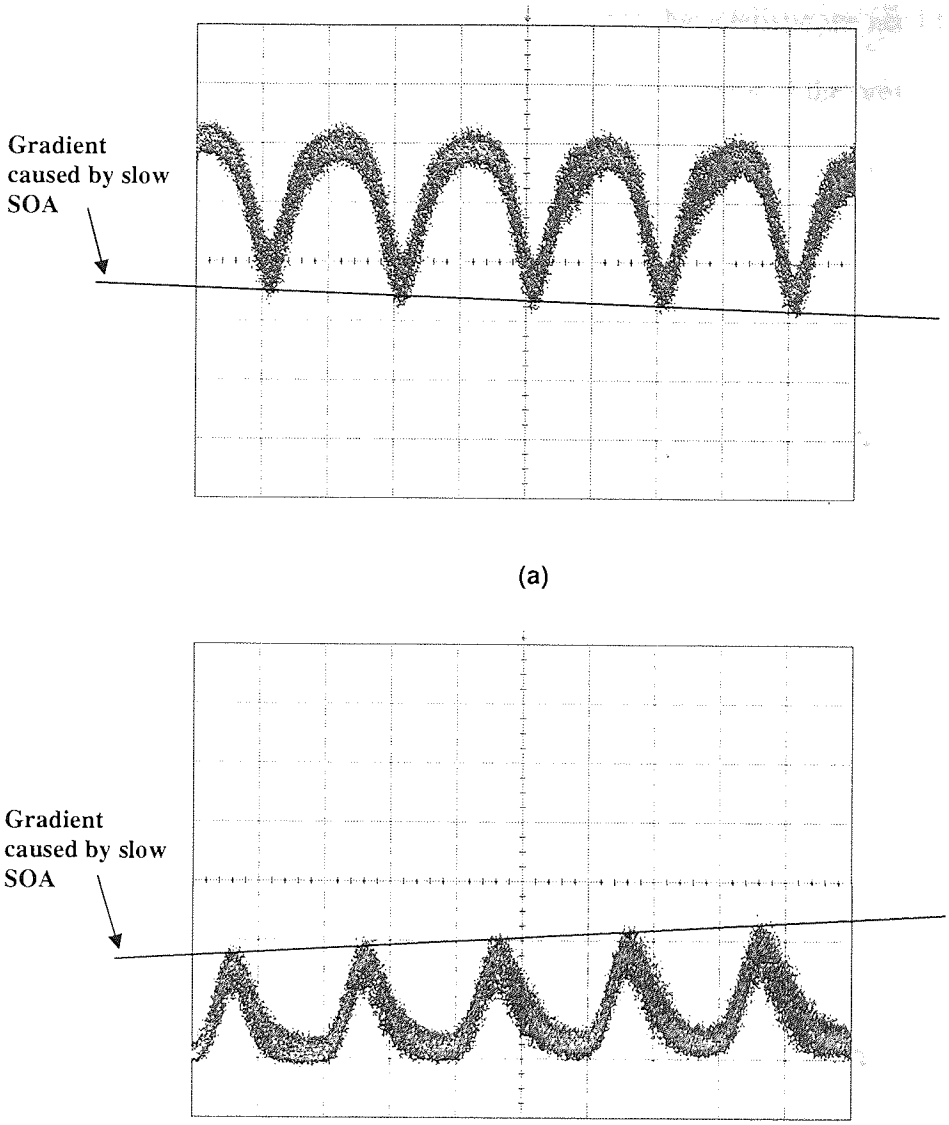
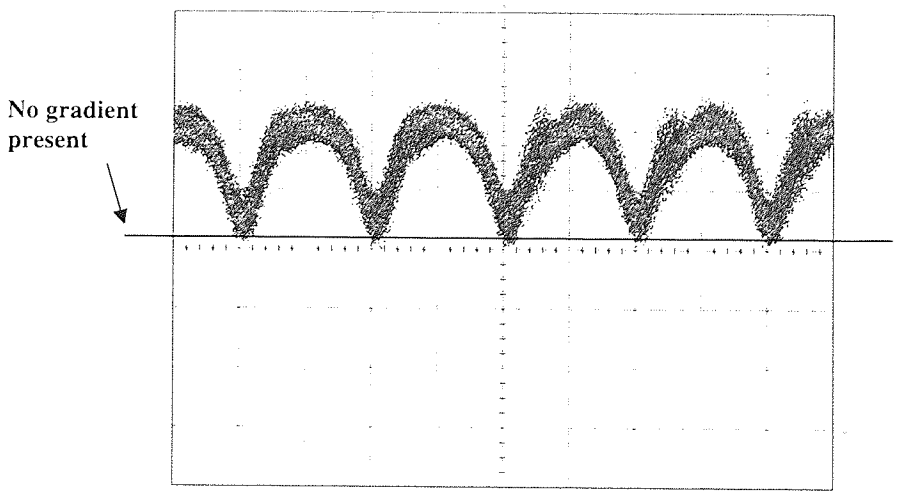


Figure 6-7 Output from the non push-pull Mach-Zehnder interferometer when five "1"s are switched out after a block of Zeros. (a) Is the normally constructive output (b) is the normally destructive output

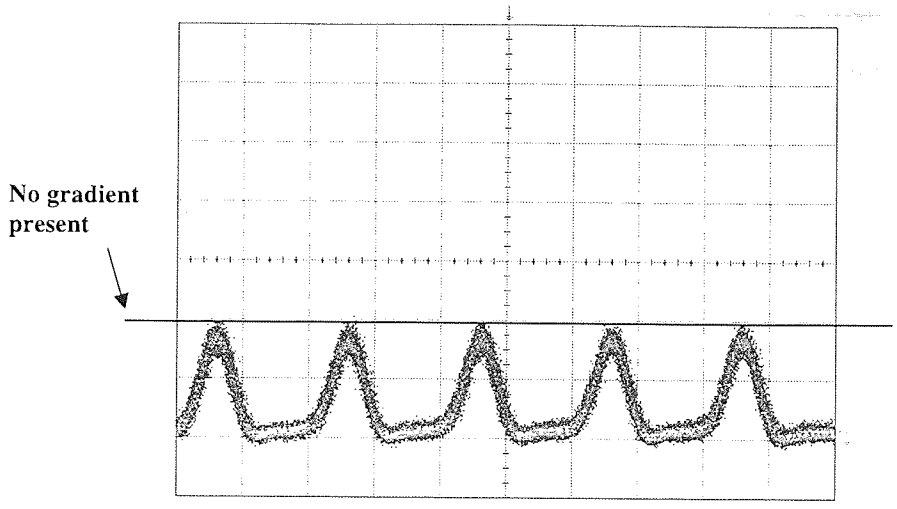
The effect of a long sequence of ones on a non push-pull device can be seen in Figure 6-7 where (a) represents the output for the normally constructive port and (b) is the output for the normally destructive port. After each control pulse the output of the destructive port does not return to the same level as before the control pulse. On the normally destructive port, the level of output continuously increases after each control pulse and as expected the opposite occurs on the normally constructive port, where

the output decreases. To explain the reason for this characteristic we need to consider the SOAs carrier density throughout this process. As a result of the previous block of zeros, the SOA has had time to fully recover before the first control pulse. However, after the first control pulse, the SOA does not have time to return to the fully recovered state. Therefore, when the second control pulse arrives at the SOA the carrier density is lower than when the first control pulse arrives. As a result the second control pulse reduces the carrier density to a lower level, than the first pulse. This lower level would take longer to recover and as a consequence for every subsequent "1" the carrier density level will be reduced further until a stable level is reached.

The push-pull configuration ensures that this does not happen. As with the non push-pull configuration, the non-delayed pulse saturates one of the SOAs first, causing switching. After a period of time, the delayed pulse enters the second SOA. This delayed pulse has sufficient power to saturate the second SOA to the same saturation level as the recovering first SOA, thus bringing to a halt switching. After every bit the two SOAs are balanced to the same carrier density level, consequently the impact of the recovery rate of the SOA is reduced (at high bit rates the patterning effect is still evident).



(a)



(b)

Figure 6-8 The output from the Mach-Zehnder using two SOAs in push-pull configuration when five "1"s are switched out after a block of Zeros. (a) Is the normally constructive output (b) is the normally destructive output.

Figure 6-8 shows a repeat of the experiment shown in Figure 6-7. This time the push-pull configuration is being used. As we can see from the results the peak pulse level does not change after each successive "1" unlike for the non-inverting level thus, providing the potential for operation at higher bit rates.

6.4. Unbalancing the Mach Zehnder Interferometer using SOA current

Once fully recovered the SOAs carrier density will reach a state of equilibrium according to equation (1.17). Therefore, a change in the forward biasing current will not only change the gain available but also the refractive index of the SOA. With the MZI it is possible to measure the exact phase shift obtained as the current changes. By keeping a constant current supply to SOA1 and varying the current supply to SOA2 we can observe the resultant phase shift.

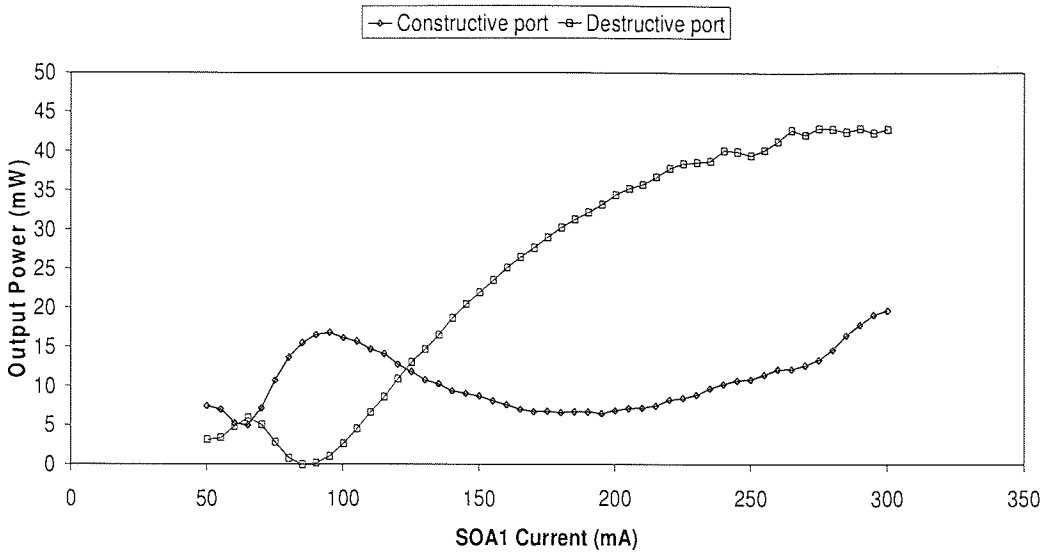


Figure 6-9 Output from both arms as the current is varied in one of the SOAs

Figure 6-9 shows the output from both arms of the MZI for a change in the SOA current. In this case there are no control pulses present and the clock consists of CW light. The current supply to SOA2 was fixed at 90mA whilst the current supply to SOA1 was varied from 40mA to 300mA. When the current supplied to both SOAs equals 90mA the phase shift and the gain seen in both arms are the same. As a result, perfect extinction between the two outputs is achieved and all the light exits through the constructive port. As the current supply to SOA1 is changed so does the proportion of light exiting both the constructive and destructive ports. This provides evidence that the refractive index of the SOA changes with gain. As a result of the additional effects of the variation of the gain, the results are best shown using the coefficients, corresponding to the transmission and reflection coefficients of the loop mirror, rather than the actual values. In the following, these will simply be referred to as the output coefficients.

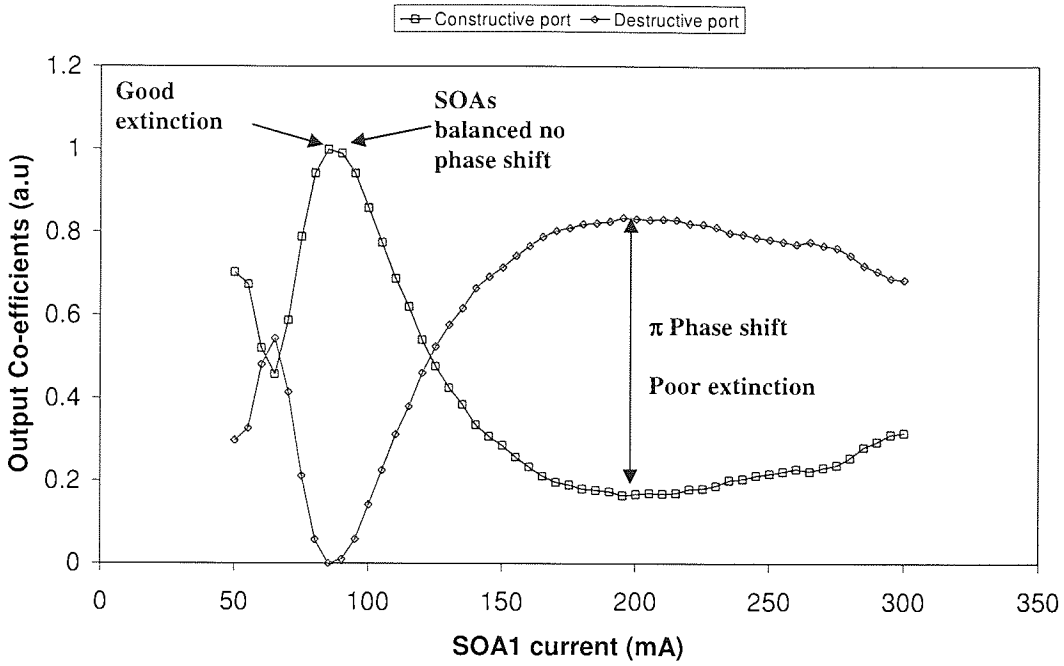


Figure 6-10 Coefficient of output power as a function of SOA current

Figure 6-10 shows the output coefficients as a function of the SOA current. The MZI is balanced when both the SOAs are set to 90mA. At this point there is no differential phase shift and all signal output is through the constructive port and little or no signal is evident at the destructive port. We can see that a (relative) π phase shift occurs at approximately 65mA and 200mA. A 2π phase shift is produced when the current is set to approximately 50mA. If we examine the extinction ratio for each value we can see that the extinction is at its highest when the SOAs have the same current. When the currents are different then the two SOAs do not provide the same level of gain; hence when the signals recombine in the second coupler they do not have the same power.

6.5. *Phase shifters characterisation*

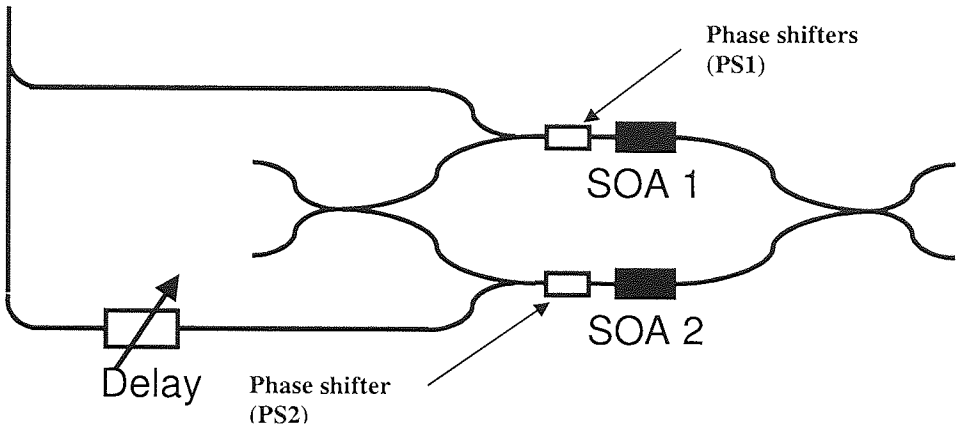


Figure 6-11 Mach-Zehnder interferometer with phase shifters included

We have seen in the previous section that we can use the SOA current to set the differential phase shift between each arm. However, for maximum extinction to take place the SOAs must produce the same gain. In the hybrid integrated MZI, voltage controlled phase shifters are included in each arm, see Figure 6-11. These are voltage controlled thermal devices, which change the length of each arm according to the applied voltage. The phase shifters are used for manual adjustment of the phase shift in each arm allowing the constructive and destructive ports to be manually switched over.

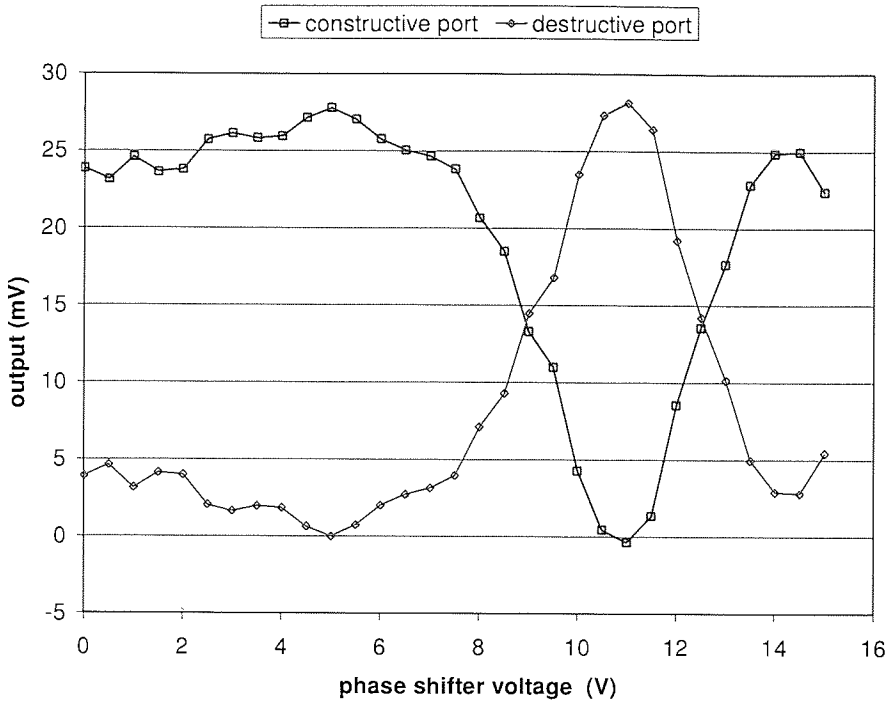


Figure 6-12 Constructive and destructive outputs for changes in voltage to PS1

Figure 6-12 shows the constructive and destructive outputs when PS2 has a constant voltage supply and the voltage to PS1 is changed. In these results no control pulse was present and just a 10Ghz clock was used. As we can see from the result the change in the voltage changed the phase shift through the arm and hence the differential phases shift between the arms. To enable setup of the interferometer we need to understand how the change in the phase shifters affects the phase shift generated through a control pulse.

As with the TOAD device, section 2.5, the output coefficients can be generated by recording the output powers on the constructive and destructive ports, whilst simultaneously injecting increasing amounts of control signal.

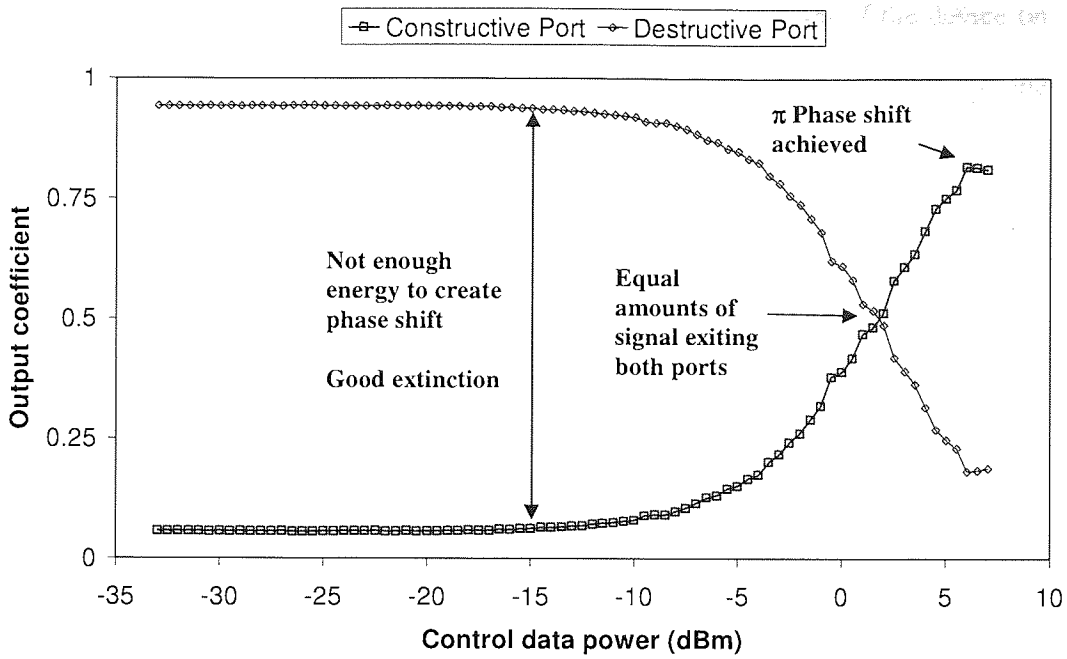


Figure 6-13 Switching coefficients for the Hybrid Integrated Mach-Zehnder interferometer

The Hybrid Integrated MZI output coefficients for the constructive and destructive ports can be found in Figure 6-13. As with the TOAD, Figure 2-9, when the control pulse energies are increased a differential phase shift is applied to the arms, which creates switching. In Figure 6-13 at control powers below approximately -15dBm the device is setup for maximum extinction, that is the maximum amount of the light is emitted from the constructive port and the light present at the destructive port is minimised. When the control power reaches approximately 2dBm equal amounts of light exit both the constructive and destructive ports. When the control pulse power equals 6dBm a full π differential phase shift is achieved. As described in the previous section because the arms are experiencing not only a differential phase shift but also a difference in gain then the switching results in poor extinction.

The main aim of the phase shifters is to determine the starting point of the device on the switching curve. We can determine this by recording the switching curves for one of the outputs against the different phase shift voltages.

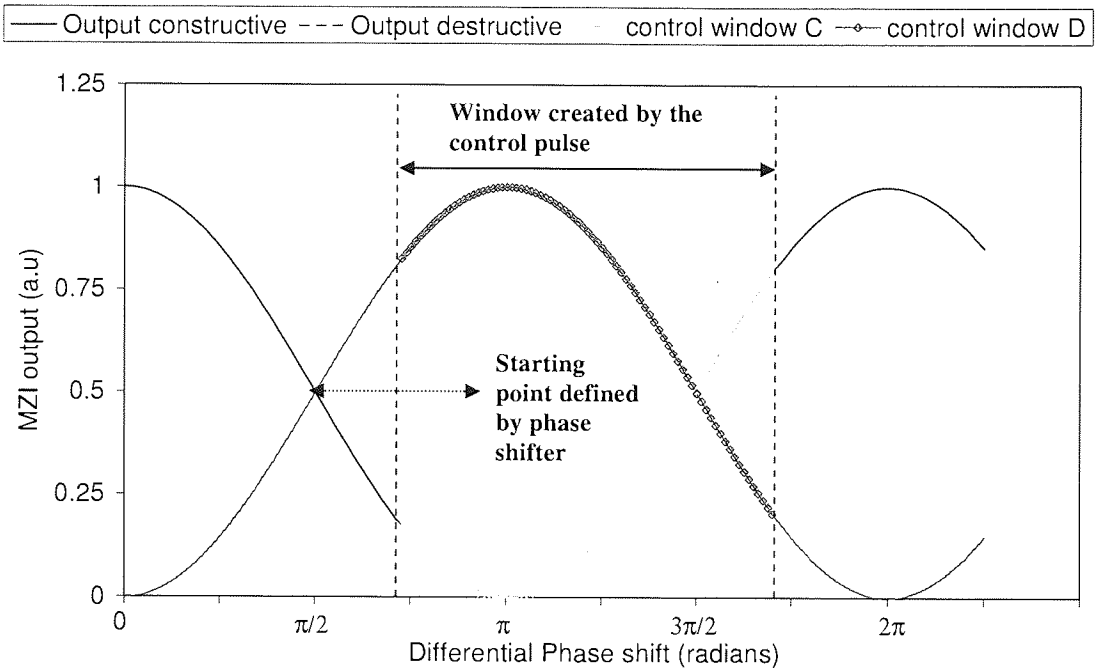


Figure 6-14 Theoretical chart demonstrating the link between the phase shifters and the differential phase shift generated by the control pulse

Figure 6-14 demonstrates the link between the phase shifter settings and the phase shift generated by the control pulse. If there were no control pulses present then the output of the arms would move up and down according to the differential phase shift caused by the phase shifters. With the addition of a control pulse we can add to the phase shift changing this location along the horizontal axis. Of course only a certain amount of phase shift can be applied through the control pulse therefore, a window is produced. We can see this effect in Figure 6-15 where various output port powers have been taken for control power as a function of the phase shifter voltages. When the phase shifter voltage changes so does the initial differential phase shift and

ultimately the initial output power. The reaction to a control pulse on the output power is determined by the starting differential phase shift.

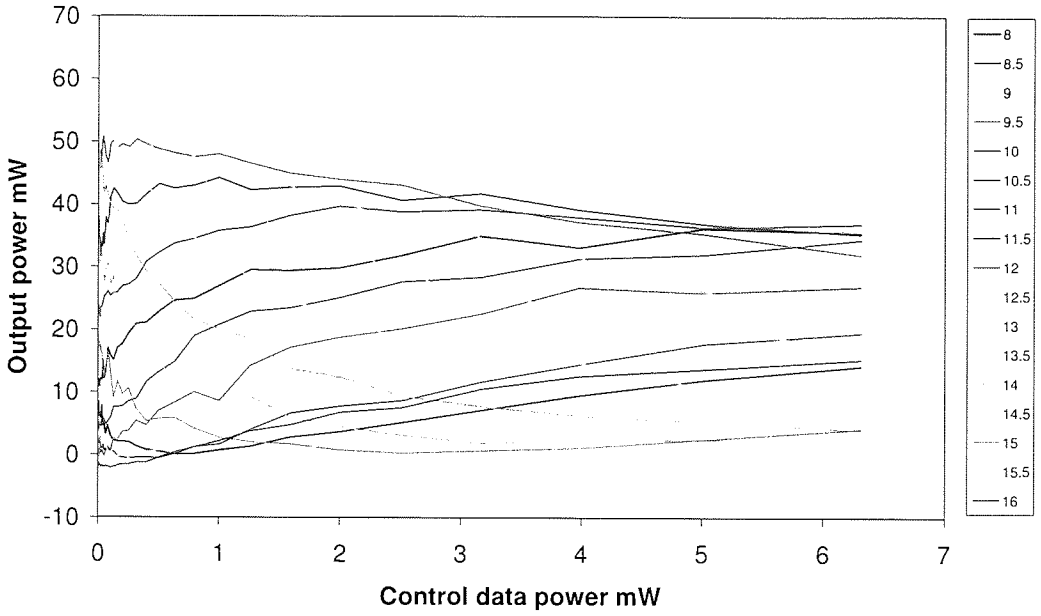


Figure 6-15 Output of one of the arms with various voltages applied to the phase shifters

6.6. Demonstration of non-inverting memory using hybrid integrated device

For a storage device to be commercially viable it has to be small and operate at high bit rates, as well as being cost effective. The hybrid integrated MZI is a compact package fitted onto one chip giving the potential to implement the scheme described above in an integrated device. Operation of such devices has been demonstrated at 40GHz using a form of the shift register [94]

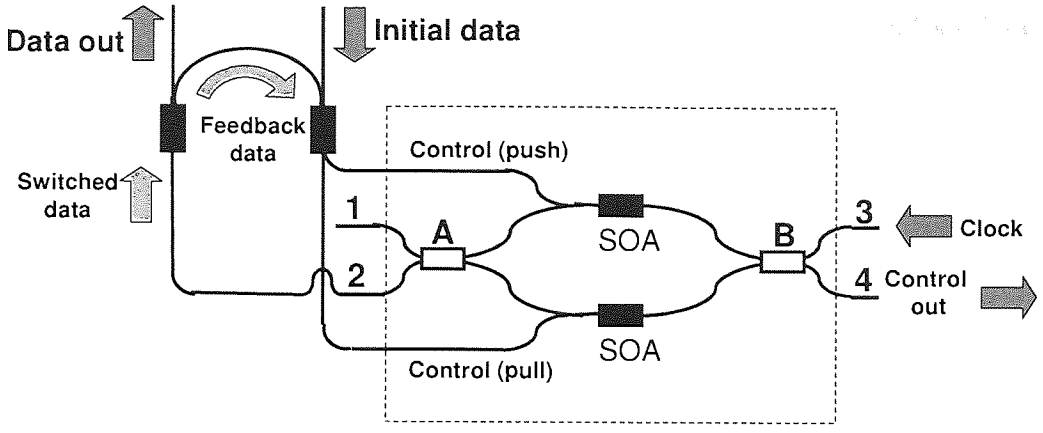


Figure 6-16 Schematic diagram of the non-inverting memory using a Mach-Zehnder interferometer

The MZ based memory device is shown schematically in Figure 6-16. In a similar way to the loop mirror, light injected into port 3 (Clock) is split at coupler B. The pulses propagate through both the top and the bottom arms until they enter coupler A and recombine interferometrically. With no relative phase shift between the two arms of the interferometer all the light will exit through port 1. As with the Sagnac loop mirror by introducing a relative π phase delay between the arms of the interferometer the signal will switch from port 1 to port 2.

In both the TOAD and the MZI configurations the recovery rate of the SOA determines the maximum operational bit rate of the device, a slow SOA recovery can lead to inter-symbol interference. Therefore, in this experiment a push-pull configuration was used utilising two SOAs, one in each arm of the interferometer.

The operation of the memory is the same as for the Sagnac loop mirror configuration described above. The packet is stored by injecting RZ data into the "initial data" port once only. These control pulses are then split and coupled into the arms of the interferometer and used to switch out the RZ clock pulses injected through input port 3. The switched clock pulses containing the data will then exit through output port 2.

Once again, extended storage can be achieved through the use of a feedback loop, which will feed the regenerated signal back into the MZI through the push-pull input ports. These will then switch out the next set of clock pulses and the cycle will continue until the feedback loop is disconnected.

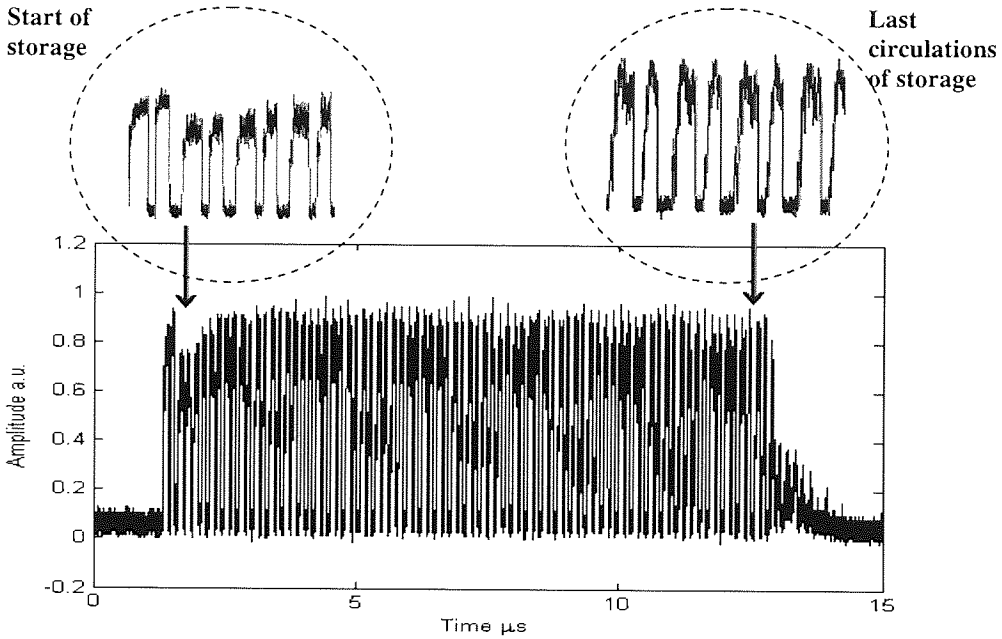


Figure 6-17 Oscilloscope trace showing operation of the Mach-Zehnder non-inverting memory

The results demonstrating preliminary proof of concept for the MZI configuration are shown in Figure 6-17, where a 10Gb/s data packet has been stored for 50 circulations. For ease of identification a simple packet was used consisting of a block of ones separated by a block of zeros. The real time oscilloscope trace shows successful storage of a data packet. The left insert show the initial input data packet and the first three circulations and the right insert showing the final four circulations (right insert), with the 10Gb/s data packet being successfully stored for over 10µs. These results show the feasibility of this configuration for integration and miniaturisation at higher data rates than the Sagnac loop configuration.

6.7. Discussion

In the previous chapters the TOAD based non-inverting optical memory has been the main subject of study. In this chapter the concept of using a hybrid integrated MZI, in replacement for the TOAD, has been introduced. The advantages and disadvantages of using the MZI in replacement for the TOAD have been discussed with the hybrid integrated MZI showing greater potential for commercial applications.

Through some experimental demonstrations relating to basic operation of the MZI we have demonstrated the advantages of the push-pull device using two SOAs located in each arm as opposed to the non push-pull configuration using a single SOA. Through the push-pull solution the operational bit rate has been made less dependent on the SOA recovery time, thus demonstrating the potential for higher bit rate operation.

The proof of principle for using the hybrid integrated MZI has been experimentally demonstrated at 10Gb/s using a basic pattern. The initial results demonstrated in this chapter provide proof of concept only. However, further research is required to demonstrate the operation further, thus confirming the MZI's potential in a non-inverting memory.

7. Conclusions and further work

7.1. Conclusion

This thesis has explored a potential solution to provide an all-optical memory. Two approaches have been investigated using a Terahertz Asymmetric Optical Demultiplexor (TOAD) based device and a Mach-Zehnder Interferometer (MZI) based device. Both configurations are regenerative where the data is refreshed after a period of time that allows for potential long-term storage. The concept of looping the output of a regenerator back into its input for regeneration, with the aim of creating long term memory storage, has been demonstrated. Although this technique has been demonstrated before, this is the first time this has been investigated and demonstrated with a non-inverting characteristic. By having the data swap to its complement, as previously reported, the access time is increased, reducing the performance of the memory. Thus, by having a solution that does not have this characteristic we can reduce the maximum access time by half.

The majority of research undertaken in this thesis has been focused around the non-inverting configuration using a TOAD. This configuration has been both experimentally and numerically investigated and demonstrated. For reasons of compact physical size and low switching energies the SOA was chosen as the non-linear element required for switching. Initial investigations were achieved using a simple numerical simulation followed by experimental demonstrations using a basic pattern. The storage of a basic pattern using the TOAD has been demonstrated for up to a time period of 1s.

Using the numerical model initial investigations were made into the operation of the non-inverting memory. One of the most notable effects was when the initial data power was changed. It was later confirmed experimentally, provided the initial data had enough power for storage, successive circulations increase or decrease the power of the stored data until a stable level is reached. It was also shown that changing the gain in the feedback changed the power of the stable level.

In addition to the change in the initial data powers, experimental demonstrations were made showing the devices ability to store and recover a signal with poor initial quality. This is only possible because the TOAD acts as a regenerator.

After confirming the operation and the potential of the non-inverting optical memory, the next stage was to use more complex data and measure the quality using a Bit Error Rate Test set (BERT). With the initial measurements of the SOA recovery and operation of the TOAD it quickly became clear that 10Gb/s operation was not possible with the SOA available, therefore, the bit rate was effectively reduced to 3.3Gb/s. Although the bit rate was reduced to a level lower than desired, the tests applied using the BERT would still be sufficient to demonstrate that the quality of the data would not be reduced with increased storage time.

With all the pulse preserving techniques the longer the data is stored the lower the quality of the exiting data. Therefore the degradation effects limit the maximum storage time. By using a pulse regenerative device the degradation effects, which limit the storage time of a pulse preserving memory device, are minimised making storage time effectively unlimited. It was important therefore to clarify that the data does not deteriorate after each circulation. By using a BERT it has been shown using a variety of techniques that the data does not deteriorate up to 1000 circulations. Three

techniques were used Bit Error Rate (BER) curves, Q-Values and BER intensity graphs. It was demonstrated that although there was an initial settling down time after this period no further degradation took place.

Although it has been demonstrated that this device works as a concept there are many issues that need to be addressed before this could become a potentially commercial product. Firstly the experimental device was built using discrete devices, which makes the device relatively large in physical size. Secondly the data rate used in this device does not match up to the potential 40GHz line rates that have been proposed for the next generation optical communication systems. One potential solution would be to use a hybrid-integrated device.

The later part of the thesis demonstrated the potential of using a hybrid integrated Mach-Zehnder Interferometer (MZI). Such a device has been demonstrated at 40Gb/s whilst having a small physical footprint [94]. Through experimental demonstration the operation of the Mach-Zehnder has been investigated, demonstrating how the push-pull system increases the potential operational bit rate whilst using a relatively slow SOA. Although detailed investigation has not been done, the proof of concept has been experimentally demonstrated showing the storage of a basic pattern for 10μs whilst showing the desired non-inverting characteristics.

7.2. Further work

It was the intention throughout this thesis to introduce the concept of a non-inverting all-optical memory, using both a TOAD and a Mach-Zehnder interferometer. Therefore, there are many possible extensions, which could be made to this research that would contribute to a potential commercial solution. The most promising direction would be to continue further investigations into the operation of the hybrid integrated Mach-Zehnder interferometer device. The results presented in this thesis are preliminary and only provide proof of concept. Before any full conclusions can be made confirming the viability for a Mach-Zehnder based non-inverting optical memory, investigations must be made into the quality of the data stored. Initially this must be done using basic data patterns and then progressing onto BER results. Initially these results may be made using 10Gb/s data progressing onto 40Gb/s. Throughout the research on the TOAD based configuration, one critical aspect became clear. Any noise in the system could potentially cause the data to be lost, in a device such as the proposed memory solutions a loop containing gain is present, hence the potential for noise to propagate around this loop whilst being amplified is high.

With the TOAD the SOA could only be operated up to a certain current level without the risk of the noise being prominent and causing errors. With the Mach-Zehnder interferometer Push-pull device there are two SOAs in the system potentially doubling the ASE produced. In addition with the TOAD setup, reflections were minimised through the installation of isolators where possible. As the Mach-Zehnder is an integrated unit such measures would be difficult to implement. Therefore, the operation of the non-inverting memory could potentially be limited by noise and reflections.

When using the TOAD the factor limiting the bit rate, in this research, was the SOA recovery time. It has been well documented that using assisted light injection can improve the recovery speed of the SOA [95, 96]. Investigations would need to be made to see if this is possible. Firstly would the recovery rate be increased enough to allow for higher bit rates. Using light injection might enable the bit rate to increase to 5Gb/s (although 10Gb/s has been shown to be potentially achievable) however the recovery still might be too slow for 10Gb/s operation. The second consideration would be the effect this would have on the extinction ratio of the switched output. The injection of light into the SOA would change the gain characteristics of the SOA. As we have seen in previous experiments the extinction ratio of the switched outputs may be disrupted enough to prevent successful storage.

Unlike the SOA, the response time of silica fibre is on the timescale of femtoseconds. Therefore the possibility for high operational bit rates maybe be achieved using Highly Non-Linear Fibre (HNLF) instead of an SOA, as the non-linear element. This could be a potential solution to enable bit rates of 40Gb/s and above.

With the current setup of the TOAD using 3.3Gb/s data, further work on varying the condition of the initial data could be undertaken. If the intention of the device is to operate as an input buffer then the signal received may have been transmitted for a long distance before it reaches the buffer. Further investigation could be made to measuring the dynamic range of the Q value of the initial data.

8. Appendices

8.1. *Appendix A: Publications*

- N.C. Johnson, J.A. Harrison, K.J. Blow, *All-optical regenerative memory using a semiconductor optical amplifier in a single loop mirror*, in *Photonics in Switching 2006*: Crete.

- N.C. Johnson, J.A. Harrison, K.J. Blow, *All-optical regenerative memory using a single loop mirror with feedback*, in *Nonlinear Photonics*. 2007, OSA: Quebec.

- N.C. Johnson, J.A. Harrison, K.J. Blow, *Demonstration and Characterisation of a non-inverting All-optical read/write regenerative memory*. Optics communications, 2008. **281**(17): p. 4464-4469.

- N.C. Johnson, J.A. Harrison, K.J. Blow, P.Harper, *Experimental demonstration of SOA based non-inverting optical memory*, in *Photonics in Switching 2008*. 2008: Sopporo, Japan.

- N.C Johnson, J A Harrison, K J Blow, *Symmetric operating point for increasing the extinction ratio of semiconductor based optical loop mirrors*. Journal of modern optics, 2008, vol55(17), p2777-2783.

8.2. Appendix B: Definitions and Symbols

3R	Regenerate, reshape, re-time
a	Fibre radius
α	Coupling co-efficient
A	Active region cross sectional area (SOA)
AC_W	Anticlockwise
$\varnothing$	Phase difference across the arms
A_{eff}	Affective area
AOM	Acoustic Optical Modulator
ASE	Amplified Spontanious Emmision
BER	Bit Error Rate
BERT	Bit Error Rate Test equipment
B_R	Bit rate period
c	Speed of light in a vaccum
CW	Continuous wave
C_W	Clockwise
dB	Decibels
dBm	Power calculated in dB with respect to 1mW
DPSK	Differential phase shift keying
DSF	Dispersion shifted fibres

e	Unit electric charge
EDFA	Erbium doped fibre amplifier
Ei1	Electrical field entering the coupler port1
Ei2	Electrical field entering the coupler port2
Eo1	Electrical field exiting the coupler output port1
Eo2	Electrical field exiting the coupler output port2
FP-SOA	Fabry perot semiconductor optical amplifer
FWHM	Full Width Half Max
FWM	Four wave mixing
g	Gain co-efficient
HNLF	Highly Non-linear Fibre
hv	Photon energy
I	Intensity
I_f	SOA forward biasing current
l	Device length (SOA)
$\mu\sigma$	Microseconds
MZI	Mach-Zehnder Interferometer
n	Refractive index of the fibre
N	SOA carrier density
n(E)	Intensity dependant refractive index

N_0	Carrier density when the SOA has fully recovered
n_1	Refractive index of the core
n_2	Refractive index of the cladding
NALM	Non linear amplified loop mirror
n_c	Refractive index co-efficient
N_{eh}	Thermal equalibrium
NOLM	Non linear optical loop mirror
NRZ	Non-return to zero
NT	Carrier density as transparancy
$Ø_c$	Critical angle
OEO	Optical electrical optical conversion
OFA	Optical fibre amplifiers
$Ø_i$	Angle of incidence
OOK	On off keying
P	Power
Pr	Power reflected
PRBS	Pseudo-Random Binary Sequence
Ps	Power signal
Ps	Picoseconds
Pt	Power transmitted

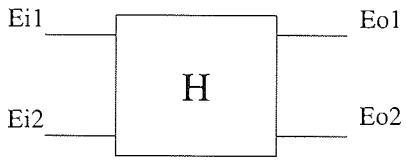
RAM	Random access memory
RZ	Return to zero
S_c	Storage Capacity
SLALOM	Semiconductor Laser Amplifier in a Loop Mirror
SMF	Single mode fibre
SNR	Signal to noise ratio
SOA	Semiconductor Optical Amplifier
SPM	Self phase modulation
TOAD	Terahertz Asymmetric Optical Demultiplexor
TW-SOA	Traveling wave semiconductor optical amplifer
VOA	Variable Optical Attenuator
XGM	Cross gain modulation
XPM	Cross phase modulation
Γ	Confinement factor (SOA)
λ	Wavelength
τ	Carrier lifetime (SOA)

8.3. Appendix C: Coupler theory

Coupler Theory

Coupler equation

The following is mathematical proof of the workings of the loop mirror



The above shows a 50:50 coupler as a system Ei1/2 represents the energy entering the coupler and the energy out is represented as Eo1/2 H is the response of the system.

$$\begin{bmatrix} Eo1 \\ Eo2 \end{bmatrix} = H \begin{bmatrix} Ei1 \\ Ei2 \end{bmatrix}$$

If α = coupling coefficient and $\varnothing$ represents the phase difference across the arms then

$$H = \begin{bmatrix} (\alpha)^{\frac{1}{2}} & (1-\alpha)^{\frac{1}{2}} e^{i\varnothing} \\ (1-\alpha)^{\frac{1}{2}} e^{i\varnothing} & (\alpha)^{\frac{1}{2}} \end{bmatrix}$$

Where $(\alpha)^{\frac{1}{2}}$ and $(1-\alpha)^{\frac{1}{2}}e^{i\varnothing}$ represents the signal coming out of the arms. The phase is only represented on one arm because this is the phase difference between the two arms. Therefore replacing H into the equation

$$\begin{bmatrix} Eo1 \\ Eo2 \end{bmatrix} = \begin{bmatrix} (\alpha)^{\frac{1}{2}} & (1-\alpha)^{\frac{1}{2}}e^{i\varnothing} \\ (1-\alpha)^{\frac{1}{2}}e^{i\varnothing} & (\alpha)^{\frac{1}{2}} \end{bmatrix} \cdot \begin{bmatrix} Ei1 \\ Ei2 \end{bmatrix}$$

This matrix can be solve to give

$$Eo1 = (\alpha)^{\frac{1}{2}} Ei1 + (1-\alpha)^{\frac{1}{2}} e^{i\varnothing} Ei2$$

$$Eo2 = (1-\alpha)^{\frac{1}{2}} e^{i\varnothing} Ei1 + (\alpha)^{\frac{1}{2}} Ei2$$

In the case of the loop mirror the Ei2 is Zero so we can simplify the equation suitably

$$Eo1 = (\alpha)^{\frac{1}{2}} Ei1$$

$$Eo2 = (1-\alpha)^{\frac{1}{2}} e^{i\varnothing} Ei1$$

Output differential phase shift across a single coupler required to satisfy conservation of energy

Taking the complex conjugate the when $Eo1 \Rightarrow |Eo1|^2$ the complex components are removed

$$|Eo1|^2 = \alpha |Ei1|^2$$

$$|Eo2|^2 = (1-\alpha)|Ei1|^2$$ <u>So(α+1-α)=1</u>

In general

$$H = \begin{bmatrix} a & b \\ b & a \end{bmatrix}$$

$$Po = |Eo|^2 = |H \cdot Ei|^2 = |H|^2 \cdot |Ei|^2 = Pi$$

Conservation of energy states that power in must equal power out therefore $|Eo|^2 = |Ei|^2$ so for this to be true then $|H|^2$ must equal 1

$$|H|^2 = H^T \cdot H^* = I = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

Hence

$$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} a & b \\ b & a \end{bmatrix} \begin{bmatrix} a* & b* \\ b* & a* \end{bmatrix} = \begin{bmatrix} a \cdot a* + b \cdot b* & a \cdot b* + b \cdot a* \\ b \cdot a* + a \cdot b* & b \cdot b* + a \cdot a* \end{bmatrix}$$

$$a \cdot a* + b \cdot b* = b \cdot b* + a \cdot a* = 1 \Rightarrow |a|^2 + |b|^2 = 1$$

$$a \cdot b* + b \cdot a* = 0$$

For information $Cos^2\theta + Sin^2\theta = 1$ therefore

$$|a| = Cos\theta \text{ and } |b| = Sin\theta$$

$$a = Cos\theta e^{i\theta_a} \text{ and } b = Sin\theta e^{i\theta_b}$$

$$Cos\theta e^{i\theta_a} \cdot Sin\theta e^{-i\theta_b} + Sin\theta e^{i\theta_b} \cdot Cos\theta e^{-i\theta_a} = 0$$

a . b* + b . a* = 0

$$Cos\theta \cdot Sin\theta (e^{i\theta_a} \cdot e^{-i\theta_b}) + Sin\theta \cdot Cos\theta (e^{i\theta_b} \cdot e^{-i\theta_a}) = 0$$

$$Cos\theta \cdot Sin\theta \left[e^{(i\theta_a - i\theta_b)} + e^{(-i\theta_a + i\theta_b)} \right] = 0$$

$$Cos\theta \cdot Sin\theta \left[e^{i(\theta_a - \theta_b)} + e^{-i(\theta_b - \theta_a)} \right] = 0$$

This can then be converted to

$$Cos\theta \cdot Sin\theta[2Cos(\theta a - \theta b)] = 0$$

Proof of this

$$e^{i\theta} = Cos\theta + iSin\theta$$

$$e^{i(\theta a - \theta b)} = Cos(\theta a - \theta b) + iSin(\theta a - \theta b)$$

$$e^{-i(\theta a - \theta b)} = Cos(\theta a - \theta b) + iSin-(\theta a - \theta b)$$

$$e^{-i(\theta a - \theta b)} = Cos(\theta a - \theta b) - iSin(\theta a - \theta b)$$

so

$$2Cos\theta \cdot Sin\theta \cdot Cos(\theta a - \theta b) = 0$$

For this to be true then

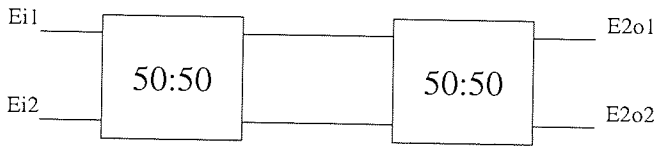
$$\Rightarrow Cos(\theta a - \theta b) = 0$$

$$(\theta a - \theta b) = (2n+1)\frac{\pi}{2}$$

Therefore the phase shift between the electric fields Ø on the output of the coupler required to satisfy conservation of energy must be = π/2

Interferometer Theory

We will now look at the interferometer configuration in this case the input to the second couplers are the outputs from the first



$$Eo1 = (\alpha)^{\frac{1}{2}} Ei1$$

$$Eo2 = (1-\alpha)^{\frac{1}{2}} e^{i\varnothing} Ei1$$

Therefore the outputs from the second coupler equal

$$\begin{bmatrix} E_2o1 \\ E_2o2 \end{bmatrix} = H_2 \begin{bmatrix} Eo1 \\ Eo2 \end{bmatrix} = \begin{bmatrix} (\alpha)^{\frac{1}{2}} & (1-\alpha)^{\frac{1}{2}} e^{i\varnothing} \\ (1-\alpha)^{\frac{1}{2}} e^{i\varnothing} & (\alpha)^{\frac{1}{2}} \end{bmatrix} \begin{bmatrix} (\alpha)^{\frac{1}{2}} Ei1 \\ (1-\alpha)^{\frac{1}{2}} e^{i\varnothing} Ei1 \end{bmatrix}$$

$$\begin{bmatrix} E_2o1 \\ E_2o2 \end{bmatrix} = \begin{bmatrix} \alpha Ei1 + (1-\alpha) e^{i2\varnothing} Ei1 \\ 2\alpha^{\frac{1}{2}} (1-\alpha)^{\frac{1}{2}} e^{i\varnothing} Ei1 \end{bmatrix} = \begin{bmatrix} [\alpha + (1-\alpha) e^{i2\varnothing}] Ei1 \\ 2[\alpha(1-\alpha)]^{\frac{1}{2}} e^{i\varnothing} Ei1 \end{bmatrix}$$

$$E_2o1 = \left[\alpha + (1-\alpha)e^{i2\varnothing}\right]Ei1$$

$$\left|E_2o1\right|^2 = \left|\left[\alpha + (1-\alpha)e^{i2\varnothing}\right]Ei1\right|^2$$

$$\left|E_2o1\right|^2 = \left[\alpha + (1-\alpha)e^{i2\varnothing}\right]Ei1 \cdot \left\{\left[\alpha + (1-\alpha)e^{i2\varnothing}\right]Ei1\right\}^*$$

$$\left|E_2o1\right|^2 = \left[\alpha + (1-\alpha)e^{i2\varnothing}\right]Ei1 \cdot \left[\alpha + (1-\alpha)e^{-i2\varnothing}\right]Ei1^*$$

$$\left|E_2o1\right|^2 = \left\{\alpha^2 + \alpha(1-\alpha)e^{-i2\varnothing} + \alpha(1-\alpha)e^{i2\varnothing} + (1-\alpha)^2\right\}Ei1 \cdot Ei1^*$$

$$\left|E_2o1\right|^2 = \left\{\alpha^2 + (1-\alpha)^2 + \alpha(1-\alpha)\left[e^{i2\varnothing} + e^{-i2\varnothing}\right]\right\}\left|Ei1\right|^2$$

remember that $e^{i\theta} = Cos\theta + iSin\theta$ so

$$e^{i2\theta} + e^{-i2\theta} = (Cos2\theta + iSin2\theta) + (Cos-2\theta + iSin-2\theta)$$

the sine's cancel each other out so what is left is the 2Cos2θ

$$\left|E_2o1\right|^2 = \left\{\alpha^2 + (1-\alpha)^2 + 2\alpha(1-\alpha)\left[Cos2\theta\right]\right\}\left|Ei1\right|^2$$

For E_2o2

$$E_2o2 = 2\left[\alpha(1-\alpha)\right]^{\frac{1}{2}} e^{i\varnothing} Ei1$$

$$\left|E_2o2\right|^2 = \left|2\left[\alpha(1-\alpha)\right]^{\frac{1}{2}} e^{i\varnothing} Ei1\right|^2$$

$$|E_2o2|^2 = 2[\alpha(1-\alpha)]^{\frac{1}{2}} e^{i\varnothing} Ei1 \cdot \left\{ 2[\alpha(1-\alpha)]^{\frac{1}{2}} e^{i\varnothing} Ei1 \right\}^*$$

$$|E_2o2|^2 = 2[\alpha(1-\alpha)]^{\frac{1}{2}} e^{i\varnothing} Ei1 \cdot \left\{ 2[\alpha(1-\alpha)]^{\frac{1}{2}} e^{-i\varnothing} Ei1 \right\}$$

$$|E_2o2|^2 = 4\alpha(1-\alpha) e^{i\varnothing} \cdot e^{-i\varnothing} |Ei1|^2$$

$$|E_2o2|^2 = 4\alpha(1-\alpha) e^{i(\varnothing-\varnothing)} |Ei1|^2$$

$$|E_2o2|^2 = 4\alpha(1-\alpha) |Ei1|^2$$

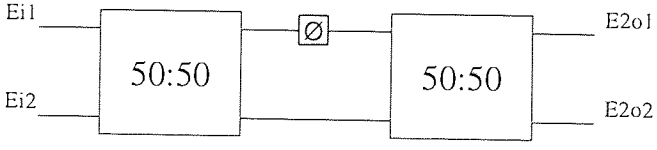
So if we add the values for α=0.5 and phase of $\theta=\pi/2$

$$|E_2o1|^2 = \left\{ \alpha^2 + (1-\alpha)^2 + 2\alpha(1-\alpha)[Cos2\theta] \right\} |Ei1|^2$$

$$|E_2o2|^2 = 4\alpha(1-\alpha) |Ei1|^2$$

$$|E_2o1|^2 = \{0.25 + 0.25 + 0.5 - 1\} |Ei1|^2 = 0$$

$$|E_2o2|^2 = 4 \cdot 0.5 \cdot 0.5 |Ei1|^2 = 1$$



For switching Matrix X can be modified to include a phase shift in one arm see figure xx

$$\begin{bmatrix} E_2o1 \\ E_2o2 \end{bmatrix} = H_2 \begin{bmatrix} Eo1 \\ Eo2 \end{bmatrix} = \begin{bmatrix} (\alpha)^{\frac{1}{2}} & (1-\alpha)^{\frac{1}{2}} e^{i\varnothing} \\ (1-\alpha)^{\frac{1}{2}} e^{i\varnothing} & (\alpha)^{\frac{1}{2}} \end{bmatrix} \begin{bmatrix} (\alpha)^{\frac{1}{2}} Ei1 \\ (1-\alpha)^{\frac{1}{2}} e^{i\varnothing_2} Ei1 \end{bmatrix}$$

Where θ_2 Represents the total phase shift on the input Eo2 the matrix can then be multiplied out to include

$$\begin{bmatrix} E_2o1 \\ E_2o2 \end{bmatrix} = \begin{bmatrix} \alpha Ei\,1 + (1-\alpha) e^{i\varnothing + \varnothing_2} Ei\,1 \\ \alpha^{\frac{1}{2}} (1-\alpha)^{\frac{1}{2}} e^{i\varnothing} Ei\,1 + \alpha^{\frac{1}{2}} (1-\alpha)^{\frac{1}{2}} e^{i\varnothing_2} Ei\,1 \end{bmatrix}$$

$$= \begin{bmatrix} \left[\alpha + (1-\alpha) e^{i\varnothing+\varnothing_2}\right] Ei1 \\ \alpha^{\frac{1}{2}} (1-\alpha)^{\frac{1}{2}} \left(e^{i\varnothing} + e^{i\varnothing_2}\right) Ei1 \end{bmatrix}$$

Therefore

$$E_2o1 = \left[\alpha + (1-\alpha) e^{i\varnothing+\varnothing_2}\right] Ei1$$

$$E_2o2 = \alpha^{\frac{1}{2}} (1-\alpha)^{\frac{1}{2}} \left(e^{i\varnothing} + e^{i\varnothing_2}\right) Ei1$$

$$\left|E_2o1\right|^2 = \left|\left[\alpha + (1-\alpha) e^{i\varnothing+\varnothing_2}\right] Ei1\right|^2$$

$$|E_2o1|^2 = \left|\left[\alpha + (1-\alpha)e^{i\varnothing+\varnothing_2}\right]Ei1\right| \cdot \left|\left[\alpha + (1-\alpha)e^{-i\varnothing+\varnothing_2}\right]Ei1\right|$$

$$|E_2o1|^2 = \left[\alpha^2 + \alpha(1-\alpha)e^{i\varnothing+\varnothing_2} + \alpha(1-\alpha)e^{-i\varnothing+\varnothing_2} + (1-\alpha)^2\right]Ei1^2$$

$$|E_2o1|^2 = \left[\alpha^2 + (1-\alpha)^2 + \alpha(1-\alpha)\left(e^{i\varnothing+\varnothing_2} + e^{-i\varnothing+\varnothing_2}\right)\right]Ei1^2$$

remember that $e^{i\theta} = Cos\theta + iSin\theta$ so

$$e^{i\theta} + e^{-i\theta} = (Cos\theta + iSin\theta) + (Cos-\theta + iSin-\theta)$$

the sine's cancel each other out so what is left is the 2Cosθ

$$|E_2o1|^2 = \left[\alpha^2 + (1-\alpha)^2 + 2\alpha(1-\alpha)(\mathrm{Cos}\theta + \theta_2)\right]Ei1^2$$

For the other arm

$$E_2o2 = \alpha^{\frac{1}{2}}(1-\alpha)^{\frac{1}{2}}\left(e^{i\varnothing} + e^{i\varnothing_2}\right)Ei1$$

$$|E_2o2|^2 = \left|\alpha^{\frac{1}{2}}(1-\alpha)^{\frac{1}{2}}\left(e^{i\varnothing} + e^{i\varnothing_2}\right)Ei1\right| \cdot \left|\alpha^{\frac{1}{2}}(1-\alpha)^{\frac{1}{2}}\left(e^{-i\varnothing} + e^{-i\varnothing_2}\right)Ei1\right|$$

$$|E_2o2|^2 = |\alpha(1-\alpha)|\left(e^{i\varnothing} + e^{i\varnothing_2}\right)\left(e^{-i\varnothing} + e^{-i\varnothing_2}\right)Ei1^2$$

$$|E_2o2|^2 = |\alpha(1-\alpha)|\left(e^{i\varnothing-\varnothing_2} + e^{i\varnothing_2-\varnothing} + 2\right)Ei1^2$$

$$|E_2o2|^2 = |\alpha(1-\alpha)|\{Cos(\varnothing_2-\varnothing) + iSin(\varnothing_2-\varnothing) + Cos(\varnothing-\varnothing_2) + Sin(\varnothing-\varnothing_2) + 2\}Ei1^2$$

$$|E_2o2|^2 = |\alpha(1-\alpha)|\{Cos(\varnothing_2-\varnothing) + Cos(\varnothing-\varnothing_2) + i[Sin(\varnothing_2-\varnothing) + Sin(\varnothing-\varnothing_2)] + 2\}Ei1^2$$

if

$$Cos(\varnothing_2 - \varnothing) + Cos(\varnothing - \varnothing_2) = 2Cos(\varnothing - \varnothing_2)$$

and

$$Sin(\varnothing_2 - \varnothing) + Sin(\varnothing - \varnothing_2) = 0$$

$$|E_2o2|^2 = |\alpha(1-\alpha)\{2Cos(\varnothing_2 - \varnothing) + 2\}Ei1^2$$

$$|E_2o2|^2 = |2\alpha(1-\alpha) + 2\alpha(1-\alpha)Cos(\varnothing_2 - \varnothing)|Ei1^2$$

To prove this if the coupling coefficient α=0.5 and the phase through the coupler $\varnothing=\pi/2$.

For no phase shift in the arm that is $\varnothing_2=\pi/2$

$$|E_2o1|^2 = [\alpha^2 + (1-\alpha)^2 + 2\alpha(1-\alpha)(\mathrm{Cos}\,\theta + \theta_2)]Ei1^2$$

$$|E_2o1|^2 = \left[0.25 + 0.25 + 0.5\left(\mathrm{Cos}\frac{\pi}{2} + \frac{\pi}{2}\right)\right]Ei1^2$$

$$|E_2o1|^2 = [0.25 + 0.25 - 0.5]Ei1^2 = 0$$

$$|E_2o2|^2 = |2\alpha(1-\alpha) + 2\alpha(1-\alpha)Cos(\varnothing_2 - \varnothing)|Ei1^2$$

$$|E_2o2|^2 = \left|0.5 + 0.5(Cos\left(\frac{\pi}{2} - \frac{\pi}{2}\right))\right|Ei1^2$$

$$|E_2o2|^2 = |0.5 + 0.5|Ei1^2 = Ei1^2$$

Therefore when no phase shift is present

$$|E_2o1|^2 = 0$$

$$|E_2o2|^2 = Ei1^2$$

If we include a π phase shift in one of the arms

$$|E_2o1|^2 = \left[0.25 + 0.25 + 0.5\left(\mathrm{Cos}\frac{\pi}{2} + \frac{3\pi}{2}\right)\right]Ei1^2$$

$$|E_2o1|^2 = [0.25 + 0.25 + 0.5(\mathrm{Cos}2\pi)]Ei1^2$$

$$|E_2o1|^2 = [0.25 + 0.25 + 0.5]Ei1^2 = Ei1^2$$

$$|E_2o2|^2 = \left|0.5 + 0.5(Cos\left(\frac{3\pi}{2} - \frac{\pi}{2}\right))\right|Ei1^2$$

$$|E_2o2|^2 = |0.5 + 0.5(Cos\pi)|Ei1^2$$

$$|E_2o2|^2 = |0.5 - 0.5|Ei1^2 = 0$$

Therefore when a phase π shift is present

$$|E_2o1|^2 = Ei1^2$$

$$|E_2o2|^2 = 0$$

So complete switching is achieved

8.4. *Appendix D: Storage of 10Gb/s data.*

Sampling oscilloscope pictures taken when attempting to store a 10GHz data packet of 01011101 using the TOAD based device. We can see after 6 cycles the data cannot be recovered.

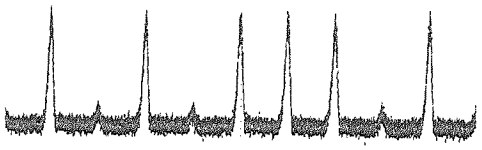


Figure 8-1 Initial data input of a 10Gb/s signal to be stored

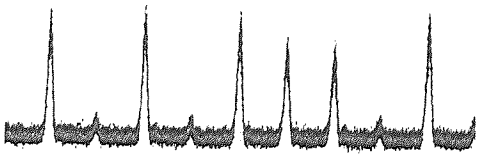


Figure 8-2 1st circulation of 10Gb/s data showing modulation caused by slow SOA recovery

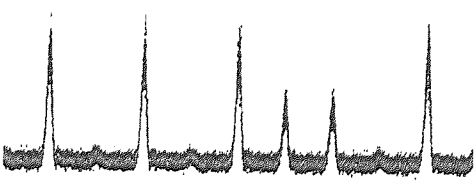


Figure 8-3 2nd circulation of 10Gb/s data showing further degrading of the signal

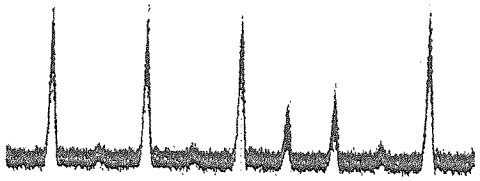


Figure 8-4 3rd circulation of 10Gb/s data quality of the data has reduced further

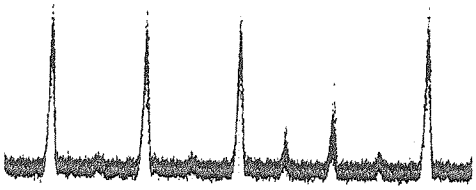


Figure 8-5 Further reduction in quality after 4 circulations of a 10Gb/s signal

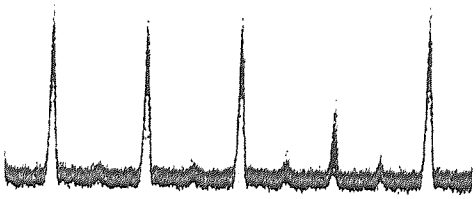


Figure 8-6 5th circulation using 10Gb/s data and the pulse affected by modulation has almost reduced to the same level as the zeros

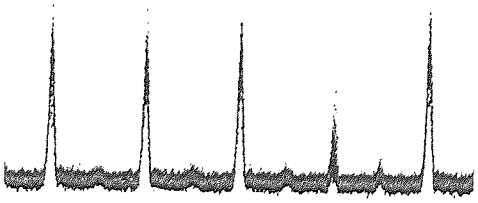


Figure 8-7 6th circulation using a 10Gb/s data and the data is completely lost through the continuous modulation effects

8.5. Appendix E: References

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